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3.2.2 Number of books and chapters in edited volumes/books published and papers published in national/ international conference proceedings per teacher during last five years

A.Y: 2019-20

Sl. No.	Name of the teacher	Title of the book/chapters published	Title of the paper	Title of the proceedings of the conference	Year of publication	ISBN/ISSN number of the proceeding	Whether at the time of publication Affiliating Institution Was sameYes/NO	Name of the publisher	PageNo
1	MandaSwapnareddy	-	Identifing Freshness of a Leaf Based on Colour Using Vector Quatization Method	3rd National Conference on Emerging Technologies in Computer Science and Engineering-2020	2019-20	978-81-945588-1-1	Yes	Santhiram Engineering College, Kurnool	1-9
2	Dr. Ashok Kumar K	-	Hardware realization of Bathymetry rover using Embedded C	First Online International Conference on "Smart Modernistic in Electronics and Communication" (ICSMEC)	2019-20	978-93-80831-43-5	Yes	Department of ECE, St.Martin's Engineering College, Secunderabad (www.smec.ac.in)	10-14
3	Dr. G.Ravindranath	-	A Prosthetic Arm Based On Electroencephalography By Signal Acquisition And Processing On Matlab	National Conference on Emerging Technologies in Energy Systems (NCETES-2020)	2019-20	-	Yes	Prasad V. Potluri Siddhartha Institute of Technology, Vijayawada, India	15-21
4	A V Murali Krishna	-	Identifing Freshness of a Leaf Based on Colour Using Vector Quatization Method	3rd National Conference on Emerging Technologies in Computer Science and Engineering-2020	2019-20	978-81-945588-1-1	Yes	Santhiram Engineering College, Kurnool	22-29

5	Dr. D. HanumanthaRao		Influence of drik[illegible] water and graphite powder concentration on electrical discharge machining of Ti-6Al-4V alloy	International Conference on Recent Adavances in Materials and Manufacturing	2019-20	d[illegible]rg/10.1 016/j.matpr. 2019.11.035	Yes	KLE Dr. M.S. Sheshgiri College of Engineering and Technology	30
6	Dr. P.Vasudeva Naidu	-	A Prosthetic Arm Based On Electroencephalography By Signal Acquisition And Processing On Matlab	National Conference on Emerging Technologies in Energy Systems (NCETES-2020)	2019-20	-	Yes	Prasad V. Potluri Siddhartha Institute of Technology, Vijayawada, India	31-37
7	B.IndiraPriyadarshini	-	A Comprehensive study on EEG signals for seizure detection Techniques	3rd International Conference on Intelligent Sustainable Systems(ICISS)	2019-20	978-1-7281-7089-3	Yes	IEEE Explorer	38-41
8	D.Nagaraju	-	Design and Simulation of a Multiband Slot Antenna for GPS/WIMAX/WLAN Systems	International Conference on Integrated Interdisciplinary Innovations in Engineering (ICIIIE-2020)	2019-20	doi:10.1088/ 1757-899X/1033/1 /012030	Yes	University Institute of Engineering and Technology, Panjob University, Chandigarh.	42-48
9	D.Nagaraju	-	Design and Simulation of a Compact 5.4 GHz H-Shaped Slot Antenna for Energy Combining	International Conference on Integrated Interdisciplinary Innovations in Engineering (ICIIIE)	2019-20	10.1088/175 7-899X/1033/1 /012031	Yes	University Institute of Engineering and Technology, Panjob University, Chandigarh.	49-55
10	V Karunakar Reddy	-	Hardware realization of Bathymetry rover using Embedded C	First Online International Conference on "Smart Modernistic in Electronics and Communication" (ICSMEC)	2019-20	978-93-80831-43-5	Yes	Department of ECE, St.Martin's Engineering College, Secunderabad (www.smec.ac.in)	56-60
11	ChilakalapudiHariPriyanka	-	Identifing Freshness of a Leaf Based on Colour Using Vector Quatization Method	3rd National Conference on Emerging Technologies in Computer Science and Engineering-2020	2019-20	978-81-945588-1-1	Yes	Santhiram Engineering College, Kurnool	61-69
12	Dr.M.Yuvaraj	-	Information Resource Planning for Health care system using Goal programming model	Continuity,Consistency and Innovation in Applied Sciences and Humanities (ICCIASH)	2019-20		Yes	St.Martin's Engineering College, Secunderabad (www.smec.ac.in)	70-84

13	B.IndiraPriyadarshini	-	Comparison of Wavelets for EEG Denoising	First Online International Conference on "Smart Modernistic in Electronics and Communication"	2019-20	978-93-80831-43-5	Yes	Department of ECE, St.Martin's Engineering College, Secunderabad (www.smec.ac.in)	85-89
14	B.IndiraPriyadarshini	-	Design And Implementation Of Dadda Multiplier For Fir Filters By Compressors	First Online International Conference on "Smart Modernistic in Electronics and Communication"	2019-20	978-93-80831-43-5	Yes	Department of ECE, St.Martin's Engineering College, Secunderabad (www.smec.ac.in)	90-97
15	B.IndiraPriyadarshini	-	Design And Implementation Of High Speed And Low Power Fir Used In Eeg Analysis	First Online International Conference on "Smart Modernistic in Electronics and Communication"	2019-20	978-93-80831-43-5	Yes	Department of ECE, St.Martin's Engineering College, Secunderabad (www.smec.ac.in)	98-103
16	Dr.N.Pavan Kumar	-	Investigation of magnetic behavior of a composite made of a soft and hard magnetic material	3rd International Conference on Condensed Matter and Applied Physics (ICC-2019)	2019-20	9.78074E+12	Yes	AIP Publishing	104-107
17	ArunaKumariKotha	-	Microwave Assisted Synthesis of Gold Nanoparticles with Phyla nodiflora (L.) Greene leaves extract	International conference on advanced light weight materials and structures	2019-20	978 81 92 7051 25	Yes	CMR technicalcampus,Kandlakoya	108-119
18	A. Abhishek Reddy	-	Operational Transconductance Amplifier with Improved Characteristics for Active Filters	First Online International Conference on "Smart Modernistic in Electronics and Communication"	2019-20	978-93-80831-43-5	Yes	St.Martins Engineering College & IOSR Journals	120-126
19	A. Abhishek Reddy	-	Spectrum Harvesting using Aggressive and Conservative Techniques in Congnitive Radio	First Online International Conference on "Smart Modernistic in Electronics and Communication"	2019-20	978-93-80831-43-5	Yes	St.Martins Engineering College & IOSR Journals	127-134
20	Dr.Y.Aparna	-	Design and synthesis of novel bis-1,2,3-triazol-1H-4-yl-substituted aryl benzimidazole2-thiols	Material Science for societal advancement organized by UGC	2019-20		Yes	Osmania University	135-141

21	P. Ravikumar Reddy	-	High Speed CmosDd Amplifiers At Low Static Current Consumption	First Online International Conference on "Smart Modernistic in Electronics and Communication"	2019-20	978-93-80831-43-5	Yes	St.Martins Engineering College & IOSR Journals	142-149
22	K. Shravan Kumar	-	IOT Based Meteorological System By Using Raspberry-Pi	First Online International Conference on "Smart Modernistic in Electronics and Communication"	2019-20	978-93-80831-43-5	Yes	St.Martins Engineering College & IOSR Journals	150-156
23	V Karunakar Reddy	-	Agricultural Field Motor Controlling Through IVR Service	First Online International Conference on "Smart Modernistic in Electronics and Communication"	2019-20	978-93-80831-43-5	Yes	St.Martins Engineering College & IOSR Journals	157-159
24	Kunda Praveen	-	Design and implementation of C.C.S.D.S. Data simulator in Alters VHDL	First Online International Conference on "Smart Modernistic in Electronics and Communication"	2019-20	978-93-80831-43-5	Yes	St.Martins Engineering College & IOSR Journals	160-170
25	Dr. Ashok Kumar K	-	Advanced Memory Management Unit for 3-D NoC	InternationaCoference on Electronics and Sustainable Communcation Systems	2019-20	978-1-7281-4108-4	Yes	IEEE Explore	171-178
26	Dr. Ashok Kumar K	-	Smart college chotbot using ML and python.	International Conference on Systems, Computation, Automation and Networking	2019-20	978-1-7281-6202-7	Yes	IEEE Explore	179-185
27	Mr. V. Karunakar Reddy	-	Advanced Memory Management Unit for 3-D NoC	InternationaCoference on Electronics and Sustainable Communcation Systems	2019-20	978-1-7281-6202-7	Yes	IEEE Explore	186-193
28	Dr. P. Hara Gopal Mani	-	Implementation of the Standard Floating Point DWT Using IEEE 754 Floating Point MAC	Presented at Intelligent Communication Technologies and Virtual Mobile Networks Conference (ICICV 2019)	2019-20	978-3-030-28364-3	Yes	Springer	194-207
29	Dr.N.S.RAO	-	Design and analysis of Koch Star shaped geometry with enclosing Ring multiband Patch Antenna for S and L	5th international conference on nano electronics circuits and Communication Systems(NCCS-2019) organised by IETE	2019-20	978-981-10-2999-8	Yes	Springer EES	208-212

			Band applications",	&ISVE .					
30	D.Nagaraju	-	Fast Turbo Codes Using Sub-Block Based Interleaver	Proceeding of Second International conference on Circuits, Controls and Communications	2019-20	978-1-5386-0615-5	Yes	IEEE Explore	213-214
31	Dr. Ashok Kumar K	-	Design of fpga based block cipher clefia for feistel network	9th National Conference on Recent Trends in Electronics and Communication Engineering	2019-20	-	Yes	Proceedings of 9 th NCRTEC-19	215-220
32	Mr. V. Karunakar Reddy	-	Design of fpga based block cipher clefia for feistel network	9th National Conference on Recent Trends in Electronics and Communication Engineering	2019-20	-	Yes	Proceedings of 9 th NCRTEC-19	221-226
33	Dr. Ashok Kumar K	-	High reliability and Low latency for Network on Chip	International Conference on Recent Advances in Computer Science and Engineering	2019-20	-	Yes	ICRACE-19	227-234
34	M.Naresh	-	Identity mapping using cluster-based certificate technique for vehicular Ad-Hoc networks	International Conference on Intelligent Computing and Control Systems (ICICCS 2019)	2019-20	978-1-5386-8113-8	Yes	IEEE Explorer	235-241
35	M.Naresh	-	Link prediction algorithm for efficient routing in VANETs	International Conference on Computing Methodologies and Communication (ICCMC 2019)	2019-20	978-1-5386-7808-4	Yes	IEEE Explorer	242-249
36	M.Naresh	-	Visiting center based portable emissary approach for data gathering in wireless sensor networks	International Conference on Computing Methodologies and Communication (ICCMC 2019)	2019-20	978-1-5386-7808-4	Yes	IEEE Explorer	250-258
37	Dr.PrakashRao	-	Implementation of the Standard Floating Point DWT Using IEEE 754 Floating Point MAC	Intelligent Communication Technologies and Virtual Mobile Networks	2019-20	978-3-030-28364-3	Yes	Springer link	259-274
38	B.IndiraPriyadarshini	-	Implementation of the standard floating point DWT using IEEE 754 Floating Point MAC	ICICV 2019, Springer.	2019-20	978-3-030-28364-3	Yes	Springer	275-290
39	Dr.NukalaSrinivasaRao	-	Broad Band Capacitive Coupling a Antenna for C-Band applications	4th International Conferecne	2019-20	978-981-15-2854-5	Yes	Springer EES	291-294

40	Dr.NukalaSrinivasaRao	-	Energy-Efficient Waste Management System Using Internet of Things	International Conference on Nanoelectronics, Circuits and Communication Systems	2019-20	978-981-15-2854-5	Yes	Springer EES	295-299
41	Dr.M.Yuvaraj	Engineering Mathematics-III	-	-	2019-20	978-81-946124-5-2	Yes	Bhavana International Publications (BHIP)	299-306
42	Dr. Yuvaraju	Operations Research	-	-	2019-20	978-81-946124-0-7	Yes	BHIP	307-315
43	DR.M.Ramesh	Engineering Mathematics-III	-	-	2019-20	978-81-946124-5-2	Yes	Bhavana International Publications(BHIP)	316-323
44	D.PurnaChandarRao	Engineering Mathematics-III	-	-	2019-20	978-81-946124-5-2	Yes	Bhavana International Publications (BHIP)	324-331
45	Dr.M.Yuvaraj	Fundamentals of Probability and Statistics for Engineers	-	-	2019-20	9781-946124-6-9	Yes	Bhavana International Publications (BHIP)	332-339
46	Dr.M.Yuvaraj	Mathematical foundations of computer science	-	-	2019-20	978-81-946124-4-5	Yes	Bhavana International Publications (BHIP)	340-346
47	R.Madhavi	Operations Research	-	-	2019-20	978-81-946124-0-7	Yes	Bhavana International Publications (BHIP)	347-355
48	Dr.P.Vijay pal reddy	Hybrid Approach for Gist Generation	-	-	2019-20	978-613-9-46471-5	Yes	Lambert Academic Publishing	356-359
49	Dr.P.Vijay pal reddy	Content word selection models for Gist Generation	-	-	2019-20	978-613-9-46436-4	Yes	Lambert Academic Publishing	360-363
50	Y.Aparna	Being Human: Ethics and Environment	A Review on Sustaiable development- Facts and Challenges	-	2019-20	978-93-87916-93-7	Yes	VL Media Solutions	364-377
51	Dr.NukalaSrinivasaRao	Springer EES	Broad Band Capacitive Coupling a Antenna for C-Band applications	4th International Conferecne	2019-20	978-981-15-2854-5	Yes	Springer EES	378-391

52	Dr.NukalaSrinivasaRao	Springer EES	Energy-Efficient Waste Management System Using Internet of Things	International Conference on Nanoelectronics, Circuits and Communication Systems	2019-20	978-981-15-2854-5	Yes	Springer EES	392-395
53	Dr. Ashok Kumar K	Recent Developments in Computing, Electronics and Mechanical Sciences	Book Chapter-Cloud Computing for IOT	-	2019-20	978-81-941281-9-9	Yes	Anvi Books & Publishers	396-400
54	Mr. V. Karunakar Reddy	Recent Developments in Computing, Electronics and Mechanical Sciences	Book Chapter-Cloud Computing for IOT	-	2019-20	978-81-941281-9-9	Yes	Anvi Books & Publishers	401-404
55	M.Naresh	Springer:Lecture Notes on Data Engineering and Comunication technologies Volume 15	Improved Vertical Handoff decision scheme in Hetrogeneouswirelss network based on SCS	International Confereance of computer network and communication Technologies (ICCNCT 2018)	2019-20	978-981-10-8681-6	Yes	Springer EES	408-421
56	Dr.NukalaSrinivasaRao	Springer EES	Design and analysis of Koch Star shaped geometry with enclosing Ring multiband Patch Antenna for S and L Band applications"	5th international conference on nano electronics circuits and Communication Systems(NCCS-2019) organised by IETE & ISVE .	2019-20	978-981-10-2999-8	Yes	Springer EES	422-426

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IDENTIFYING FRESHNESS OF A LEAF BASED ON COLOUR USING VECTOR QUANTIZATION METHOD

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***Abstract*- Quality of a leaf is influenced by its age and maturity. Edible leaves like spinach, fenugreek, curry leaves, etc., are mostly used in Indian Dishes, consumers depend on the sensory properties like appearance, colour, texture and aroma to assess the internal quality of the internal quality of the leaf. However, with the onset of automated food chains and IOT based food recognition applications, vegetables are identified by capturing their images and processing. IOT is effectively used to reduce waste, cost management and risks. For an instance, IoT facilitates food companies to ensure superior levels of traceability, food safety and, therefore accountability all through the farm-to-plate supplies chain operations. The IoT network in the food supply chain greatly helps in reducing waste, costs, and risks as well, in all stages of the procedure. In this paper a simple method is proposed to assess the quality of leafy vegetables based on its colour using vector quantization method. Cropped images are processed and fed to the algorithm to identify the number of colours in the algorithm.**

***Keywords*: k-means, IOT, colour identification, clustering, food monitoring**

I. INTRODUCTION

IOT in agriculture and food is still in early stages of development. Utilization of IOT in food chains and for food safety is increasing gradually. Food safety for perishable goods is of more concern [1]. To ensure food safety till it reaches the customer from the yield continuous food monitoring has to be done [5]. One of the highly used ingredients in Indian dishes is green leafy vegetables. Also, scientifically it is known as Spinciaoleracea Linn. (Family-Chenopodiaceae). The Spinach used as a food and has medicinal value also. Spinach bundled up with vitamins such as vitamin A, vitamin B, vitamin C and vitamin E and minerals like magnesium, manganese, iron, calcium and Folic acid. Spinach is great source of chlorophyll, which speedup digestion [7]. They are also highly perishable and have a very less shelf time as compared to other vegetables. There are varieties of green leaves that are edible and frequently used in Indian dishes like spinach, fenugreek leaves, coriander, curry leaves etc. spinach is used extensively in northern states of our country as well as southern states. There have been various algorithms used in recognizing leaves based on texture and outline characteristics [3]. Spinach leaves are a main source of calcium and are recommended as a regular diet for people with liver ailments. Spinach unlike fenugreek has a lesser shelf life and once the leaves start to lose their freshness they gradually lose their nutrition value. Freshness of a leaf is identified primarily by its colour [4]. When the leaves are placed in the shelf after harvesting they have a life span of one day without freezing and four days with freezing. Often, the leaves are kept in the fridge in super markets or at home. Monitoring perishable goods like spinach is essential in super markets to reduce loss and wastage. IOT can utilized to continuously monitor the freshness of the leaf and replace the product [2]. In this paper a solution is proposed to continuously monitor the product using a camera that captures pictures at regular intervals and directs to the central server. At the server the algorithm processes the images and sends a notification if the leaf is losing its freshness. A leaf is said to be fresh by looking at its colour, a bright green leaf is fresh, and a darker shade of green indicates an aged

leaf. A leaf with traces of brown colour can indicate spots or disease. Leaf that is yellowish could have less nutrition content and traces of black or dark brown could mean the leaf has started to decompose.

II. METHODOLOGY

A. Data Collected

Images of spinach leaves are collected from different sources using Samsung mobile camera. These images are primarily belonging to Spinach and hence images of a spinach leaf in different conditions are collected and fed to the algorithm. Leaves tend to change colour based on the environmental conditions and also the way in which they are stored. Also the time taken to store the leaf is very vital. The following common conditions are considered:

1. When the leaf is freshly plucked by hand.

2. When the leaf is plucked and maintained in cool temperatures for a day or two to retain freshness.

3. When the leaf was plucked after it aged on the plant itself

4. When the leaf has aged and also damaged without proper storage.

Images of leaves with bright green, dark green, yellowish and yellowish leaves with spots are used. Some of the images are presented below

Fig.1 Examples of the spinach leaves used in dataset

B. Procedure

The image is captured using a pinhole camera that is fixed inside the fridge or in a place where the leaves can be viewed properly. Images are captured at regular intervals and sent to a central server. The algorithm resides at the server that processes the images. The image is first cropped and only the leaf without the background is fed to the algorithm. The algorithm extracts the colours from the leaf and displays the percentage of each colour. Based on the amount of colour the server sends a notification to the client. The colours are identified using clustering K means algorithm is used to cluster the colours.

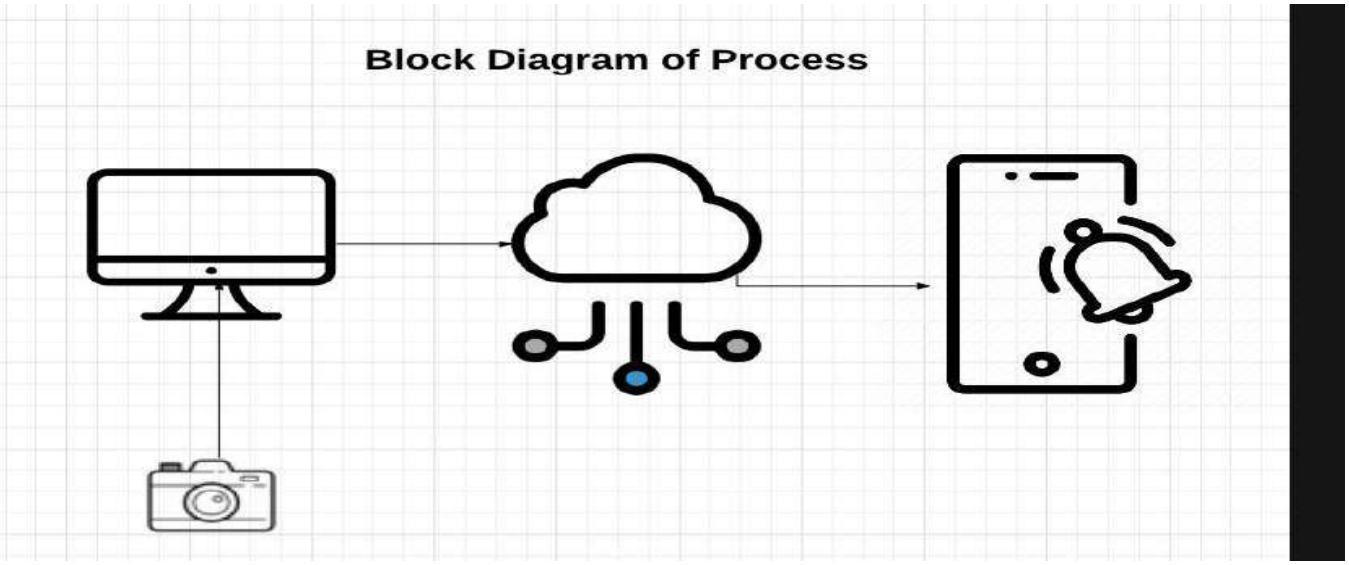


Fig. 4 A simple architecture depicting the process

The pre-processed and cropped images are fed to the algorithm that performs the following tasks:

1. Extract the RGB values of the image as hexadecimal numbers.

2. The image is then resized to a fixed height and width for uniformity.

3. The image is fed to the k-means clustering algorithm with the number of clusters as n. In our case the number of clusters depicts the number of colours. The clusters are formed using the following formula

$$J(V) = \sum_{i=1}^{c} \sum_{j=1}^{c_i} \left(\|x_i - v_j\| \right)^2$$

4. The hexadecimal values of the colours are then again converted back to RGB values and plotted on a Pie chart with the percentage of each colour.

The flow chart presented below depicts the process adopted to identify the colour of the leaf.

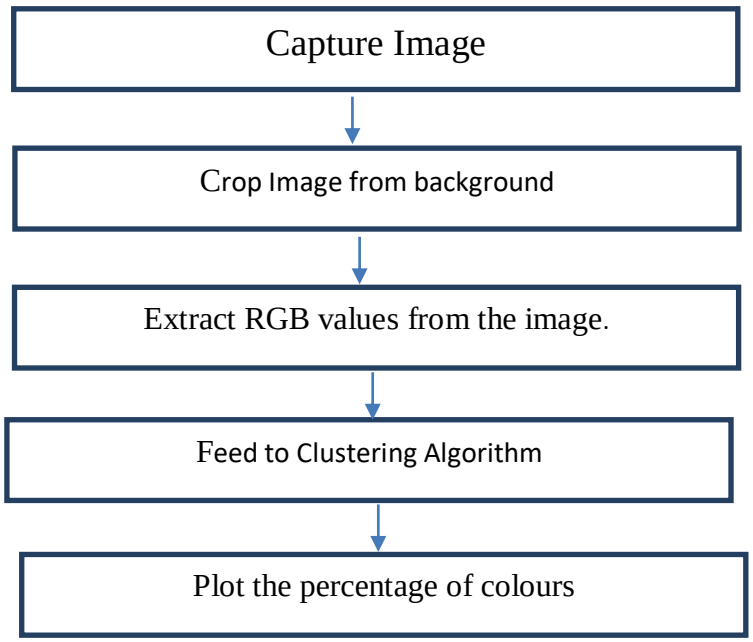


Fig. 2 Flow chart of the proposed solution

C. K means Clustering algorithm

k-means clustering is a method used for vector quantization, originating from signal processing which is popular among different cluster analysis methods in data mining[6]. k-means clustering aims to partition n observations into k clusters in which each observation belongs to the cluster with the nearest mean, serving as a prototype of the cluster. This results in a partitioning of the data space into Voronoi cells. k-Means minimizes within-cluster variances (squared Euclidean distances), but not regular Euclidean distances, which would be the more difficult Weber problem: the mean optimizes squared errors, whereas only the geometric median minimizes Euclidean distances. Better Euclidean solutions can for example be found using k-medians and k-medoids.

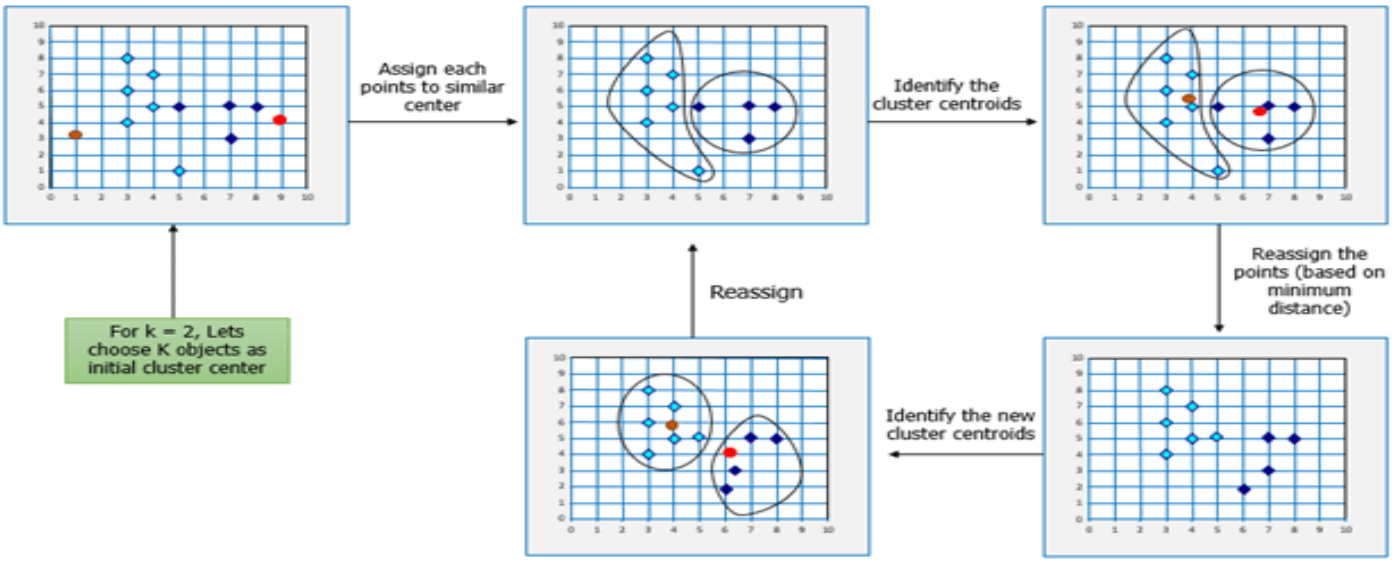
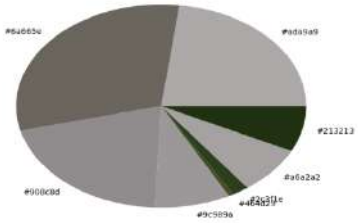
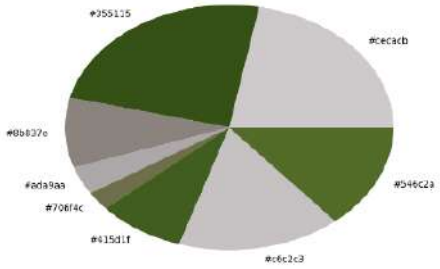


Fig. 3 A simple working model of K-means clustering

III EXPERIMENTAL RESULTS

Pre-processed images of the leaves were fed as input to the k-means clustering algorithm. The output of the algorithm is plotted using a pie chart in order to get a clear percentage of colours in the leaf. The results are presented as follows:





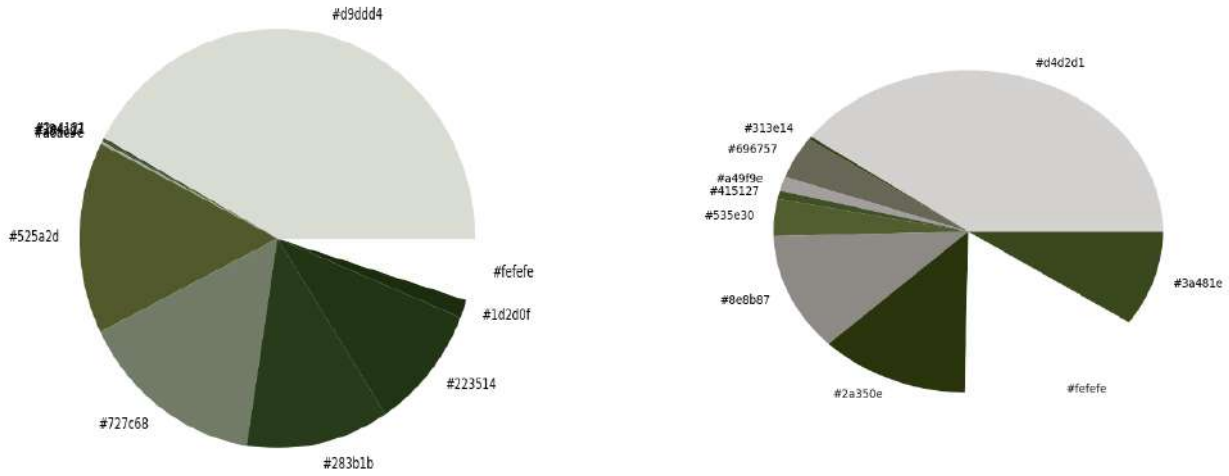


Fig 5: Results showing the colours extracted from four different leaves depicted in the previous section namely a,b,c and d.

IV CONCLUSION:

The approach proposed in this paper to identify the amount of colour present in an image of a leaf can be used to determine the freshness of a leaf. The application of this model is in food chain units where freshness of the food ,must be identified and retained. Automation of identification of the freshness using small pinhole camera with a microcontroller can be used to avoid food wastage. The percentage of different shades on the leaf is successfully extracted. Further, more work can be done to extract the amount of colour from images and predict if the leaf will decompose in a few days using machine learning algorithms. Also, notification can be sent to the store manager. More features of the leaf and its environment can be captured and predictions can be made.

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[1] E. A. Frison, I. F. Smith, T. Johns, J. Cherfas, and P. B. Eyzaguirre, "Agricultural Biodiversity, Nutrition, and Health: Making a Difference to Hunger and Nutrition in the Developing World," Food Nutr. Bull., vol. 27, no. 2, pp. 167–179, Jun. 2006.

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Processing and Information Technology, 2007, pp.

[4] Sigit Adinugroho, Yuita Arum Sari. "Leaves Classification Using Neural Network Based on Ensemble Features" in 2018 5th International Conference on Electrical and Electronics Engineering

[5] Yamine Bouzembrak, MarcelKlüche, AnandGavai and Hans J.P.Marvin. "Internet of

ABOUT SREC

Santhiram Engineering College (SREC) is sponsored by M/s Sri Shirdi Sai Educational Academy, Nandyal. SREC is established under the able guidance of Dr. M. SANTHIRAMUDU, Chairman in the year 2007 with a noble motto "Education for peace and progress". SREC is approved by AICTE, New Delhi: Recognized by UGC under 2(f) and 12 (B): Permanently Affiliated to JNTUA, Anathapuramu: Certified to an ISO 9001:2015. The college is ranked as one of the Best Engineering Colleges of JNTUA. Ananthapuramu.

SREC is situated on NH-40, 12 KM away from Nandyal, Kurnool Dist. Andhra Pradesh. It is a learning abode for 1600+ Students. The Campus is pollution free and its serene environment is ideally suited for academic activities. Our goal is to produce Engineers and Managers who can contribute to the progress of the Nation and the World through excellent Scientific, Technical Innovations and Research Activities.

COLLEGE ACHIEVEMENTS

- SREC received **BEST FASTEST GROWING ENGINEERING COLLEGE IN AP** Award in 2014 from **Dr. Smt. NAJMA HEPTULLA,** Ministry of Minority Affairs, New Delhi.
- The **BEST ENGINEERING COLLEGE** in India with **"AA"** Grade Ranked by Career 3600 Magazine.
- **Dr. M. V. SUBRAMANYAM,** Principal, received a National **PATENT CERTIFICATE** for his Research work in 2015.
- SREC Received **2 GOLD MEDALS** from JNTUA, Ananthapuramu and **8 PRATHIBA AWARDS** from the Govt. of A.P.
- Received **10 PMKVY Skill Development Centers.**
- Recognized under **GOLD CATEGORY in AICTE - CII Survey**
- Recognized **NPTEL Online Exam Center by IIT, Chennai,**
- Received **MICROSOFT CAMPUS AGREEMENT**
- Received nearly **Rs.20,00,000/- worth AICTE/IE/UGC Research Projects**
- More than **500 RESEARCH ARTICLES** published in reputed publications
- Signed **MOU** with **LINCOLN UNIVERSITY, Malaysia** for bilateral R&D activities.
- Signed **MOU** with **NUCLEUS VISION (Eleven 01 Labs)** to promote Block chain Technology across Indian college students.
- Our student won the **GOLD MEDAL** in the **3rd HEROES TAEKWONDO INTERNATIONAL CHAMPIONSHIP, Thailand in 2017.**
- Secured 2nd prize in **AICTE CHHATRA VISWAKARMA AWARD, 2018**

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Hardware realization of Bathymetry rover using Embedded C

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Abstract: Bathymetry is a process of finding water bodies depth; it is widely employed method in most of the unexplored areas of oceans and lakes. Estimating Depth using bathymetry with incorporation of velocity of sound in underground water, which depends on pressure, temperature and salinity of water body. Need for the Rover is properly justified, because of the prevailing climatologically condition on high altitudes of Himalayas. On such altitudes with temperature of glacial lakes are mostly below zero degree Celsius, hence performing bathymetry by human inspection on floating boats are very hazardous to human life.

This main purpose of this paper is to Measure water depths in lakes by means of sonar or digital transducer for calculation of depths in lakes. We use GPS (global positioning system) for tracking out the location. Arduino is used for controlling system which acts as a micro controller for working of motor, measuring the depth, identifying the location and transmission purpose. At last we use latitude and longitude to point out way in maps. State-of-the-art robotic embedded sonar vehicles are too expensive and heavy. Robotic system provides less-cost, high-accuracy bathymetric surveys of lakes, rivers and oceans is proposed. It is able to identify the exact position of rover during transmission and reception of sonar pulse. It has ability to derive the bathymetry of glacial lakes thereby controlling from the longer distance.

Keywords: Arduino; Bathymetry; GPS; Transducer.

I.INTRODUCTION

The Bathymetry rover can monitor the location of the rover and also helping to monitor the rove and displaying the depth of the lakes, river and sea. It gives mint to mint updates related to rover location in the Google maps. Arduino Uno is the major device in this system and Sever helps to store the data and display output. Bathymetry data gives information related to Shape of underwater terrain and depths, has a range of use. Nautical charts [1] formed based on the information received from Bathymetry and it is useful for mariners like a road map guide to motorists to safe and effective maritime transportations. Climate change in the environment can be learning from the bathymetry charts. These charts can alert ongoing and sea level rises, potential beach erosion and land sinking. Hydrodynamic models are created by using bathymetric data. The key element for biological oceanography [2] is bathymetry. Researchers use high resolution bathymetry to find fish and other sea food.

In this paper we constructed and designed a model which will provide vehicle location and security information to user by displaying on location in the web page by using Google Maps.

In this paper we discussed interfacing of GPS and Arduino, finding the latitude and longitude of rover location and sent to Arduino. We discussed how Sensor helps to give the river depth. It sends the latitude and longitude data and sensors data in the form bit streams via GPRS. This data is read by the server and published in Google map for this total process program is implemented in Arduino and server part in PHP language.

II. LITERATURE

The 7th International Geographic Congress presented a commission on the sub-oceanic nomenclature in Berlin 1989. It is only responsible to publish the conventional bathymetric chart. Another commission convened in Wiesbaden (April 15-16, 1903), with prince Albert-1 of Monaco is the chair person and also adopted the characteristic determined in a memorandum by J. Thoulet. The second version published between 1912 -1931 surrounded by the contour line which is representing altering of nomenclature and terrestrial relief. The utilization of sonic and ultrasonic devices are enhanced the amount heavily. The bathometry charts were initiated in 1903 by an international group geographers and oceanographers, under leadership of Prince Albert-1 of Monaco. During this time there is huge interest in the study of real time nature thereby identifying the set of group. The set of maps describes importance of the structure of ocean floor. GEBCO is maintaining in digital form as GEBCO Digital Atlas. European Marine Observation and Data Network (EMODnet) is an intelligent project which is

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funded by European govt., to bring both marine and data into interoperable, continuous and freely accessible data sets for the entire maritime basins in European waters. As part of this the EMODnet Bathymetry portal presents the bathymetry data set in the form of Digital Terrain Models (DTM) for specified basins of the maritime. The DTMs produces central DTM which is integrated and collated bathymetric data sets. If high resolution DTMs not available at that time Bathymetry information is collected from GEBCO-30 arc Second grid. In association with the GEBCOs global Bathymetric and EMODnet Hydrographic team is including bathymetry data-set from the DTMs given to EMODnet Bathymetry portal. The Baltic Sea Bathymetry Data base (BSBD) is effective the solution of an effort to create and generate a bathymetric grid for the Baltic Sea region which is using data from Baltic sea countries hydrographic offices under Baltic sea hydro graphic commission. Southwest Indian Ocean bathymetric compilation is also data set that it cover the area 4°S-40°S; 20°E-45°E. The major objective of this multinational project is to collate, assemble, publish and archive entire environment available bathymetric data set from all sources through the Indian Ocean and construct a new bathymetric map and grid of Indian Ocean using data-set from the entire open sources.

If we look around we will find ourselves to surround by computing system. Nowadays embedded systems can find all the fields like mobile phones, digital cameras, portable video games, camcorders, smart watches, calculators, washing machines, fax machines, transmission control unit, anti lock brakes, automobile industries, automated teller machines, cash registers, alarm systems, and many more. Embedded systems are used in all fields making the life easy, simpler and secure.

III. PROPOSED SYSTEM

Bathymetry is the study of under water depth of river, lake or Ocean. It can track the location of the rover and also helps in monitoring the rover and displaying the depth of water. The proposed model block diagram is as shown in below figure 1

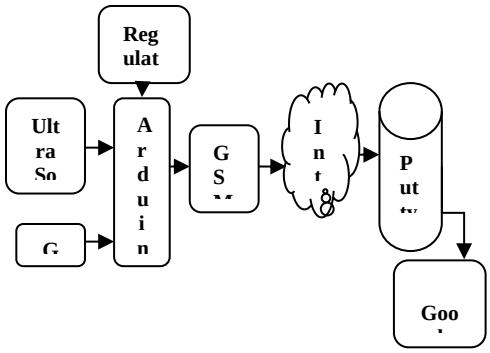

Fig 1 proposed block diagram

Ultra Sonic Sensor [3] is generates short bursts of voice and listens for this sound to echo off of objects. The frequency of the voice is very high for human being to hear (ultrasonic 40 kHz). It provides accurate, non contact distance from .02 meters -3 meters and it is easy to interface controller. Sensors will work by sending ultrasonic rupture and giving output data it corresponds to the time required for the rupture echo signal to sensor by calculating the echo signal width we can easily identify the target distance. The ping))) sensor can't measure the exact distance if the object is more than the sensor range 3 meters, if the reflected angle is $\theta<45^{\circ}$ and if the object is very small then it is difficult to get the accurate distance of the object. Along this a soft skin animals or if the objects have irregular or stuffed surface are not reflect the proper echo signals so that it is difficult to get the accurate distance. Ping))) sensors are temperature sensitivity if the temperature range is 0 to 70°C is significant in the magnitude of 11-12 percent.

C_{AIR}= 331.5 + (T_C x 0.6) m/s [4]

Global Position System (GPS) is provides time and location information in all environmental conditions, in or one the earth. The GPS System provides critical positioning capability to Civil, military and commercial user around the earth. The U S Department of Defence (D o D) is developed GPS system in 1995. The GPS module REB-1315S4 is connected to the Arduino it continuously gives information related to the longitude, altitude, latitude and relative speed also. The frequency range of the REB-1315S4 is L1 band 1575.42 MHz, it provides C.A Code and it can operate on different temperature conditions in the range between -35 to +85℃ the default bud rate of the REB-1315S4 is 9600 bits per second. In order to operate REB-1315S4 we need 3.3V DC power supply we need the power supply must be added by bypass capacitor 10µf and 1µf it is used to reduce the Noise from power supply and will increases the Power stability.

Global System for Mobile Communication (GSM) [5] is a group of ETSI standards indicating that infrastructure related to digital Cellular system. More than 85 countries are following the ETSI standards. The GSM [6] will send and receive text messages and we can also do the same for voice calls we are using SIM card. SIM800 is a wireless module and Ultra compact. It is complete dual band GSM/GPRS [7] solution SMT. SIM800A provides GSM (800MHz)/ GPRS (1800MHz) for messages, data, fax and voice with low power consumption and form factor. With small size 2.4cm X 2.4 cm X 3cm and weight of 3.4gm. It

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is controlled by using AT commands and the temperature sustainability range is -40 - 85℃. The GSM need power between 700-1000mA it is getting from external power supply. To make a call we are using AT command like ATD + mobile number with country code then press Enter similarly to disconnect the call use command ATH and Enter. Select COM port to burn the program from Laptop into Arduino board. Next power supply provided to the GSM modem for programming we use only T_X and R_X these pins are pin1 and pin2 in Arduino Uno then we have to burn the program in Board. The GSM T_X and R_X pins are connected to Arduino Uno R_X and T_X pins.

The Arduino Uno [8] is a controller based board the ATmega328. It has 16 digital input/output pins (in which 6 are used as PWM outputs), six are analog inputs, one USB connector, a power jack, ICSP header, a 16 MHz Ceramic resonator and r eset

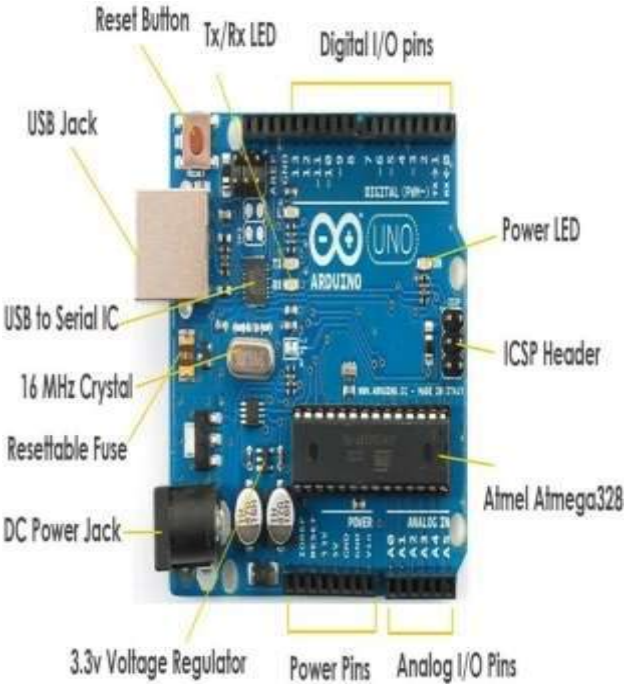

Fig 2 Arduino Uno

button. Compare to other preceding boards it won't have FTDI USB-serial driver chip. In built it is programmed as USB-Serial converter. It is having powerful reset circuit. Power supply to the board is given by using USB port. The power supply may receive from Battery or AC-DC adapter [9]. By default board will select power source. It can operate external power supply up to 6-20 Volts. The memory storage of ATmega328 has 32KB in this 0.5KB for boot loader. Along this it have 1KB of E^2PROM and 2KB OF SRAM. It is also compatible for UART Transistor – Transistor logic serial communication. It supports SPI and I^2C Communication. The Arduino Integrated Development Environment (IDE) have editor for writing programs, a text console, a message area and toolbar. It connects to Arduino Uno and Hardware to upload programs and communicating them. Writing a program in Arduino software is called Sketch. Sketches written in editor and saved with extension file .ino. The toolbar icons allow programmer to verify and upload program, open, create and save.

Hyper text Preprocessor is a scripting language in server side to design Web development. PHP code is embedded in to hyper text markup language (HTML/HTML5), it can be used in addition with web frame works and web content management system. PHP interpreter is used to process the PHP code. The web server combines the results of executed PHP code and interpreted data it may be in any form information with generated web page. PHP program may executed by using command line interface and it is used in standalone graphic applications. In PHP integer range will store depending on the platform either 32-bit/ 64-bit similar to C language. Similarly floating point numbers will store based on platform based. Standard problems are solved by using Standard PHP Library (SPL).

PuTTY is open source terminal emulator, serial console and is free network file transfer application. It supports different network communication protocols. Originally PuTTY application is meant for Microsoft windows but it is used in Linux and other operating systems. PuTTY was designed by British programmer Simon Tatham. PuTTY supports Single Sign on through the Generic Security Service Application program. PuTTY integrated with Command line Secure Copy Protocol and SSH File Transfer Protocol are called "PSCP" and "PSFTP". PuTTY does not allow Session Buttons directly.

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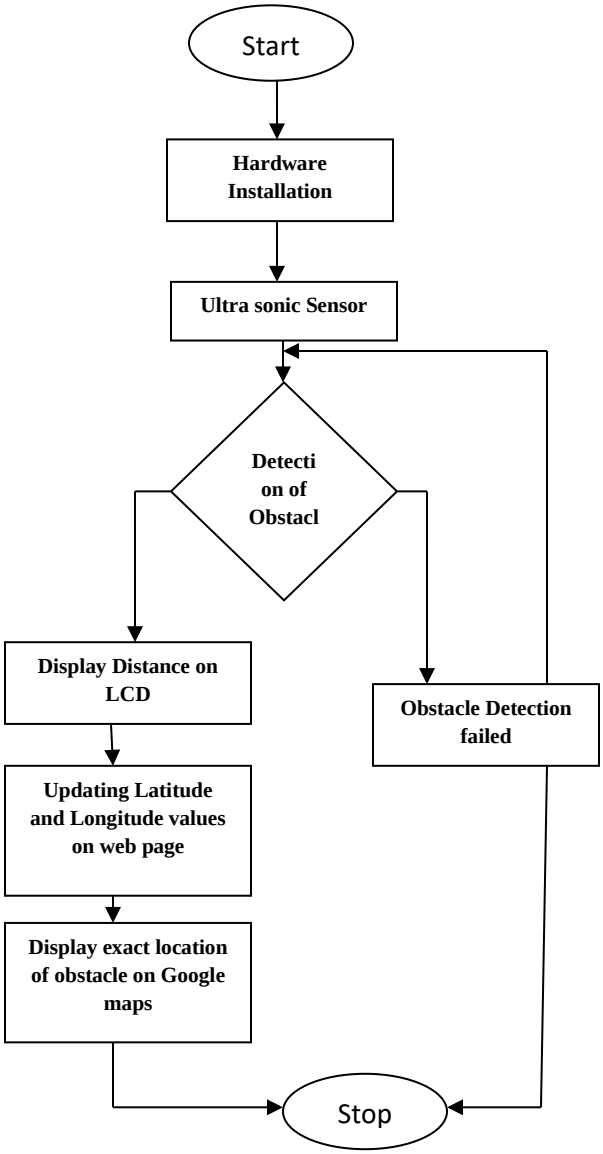
IV. PROJECT FLOW CHART



V. RESULTS

When the system is powered on the LCD will Display a welcome string "BATHYMETRY ROVER". The total kit is powered on and a sensor starts working and does respective works. Shown in figure 3.

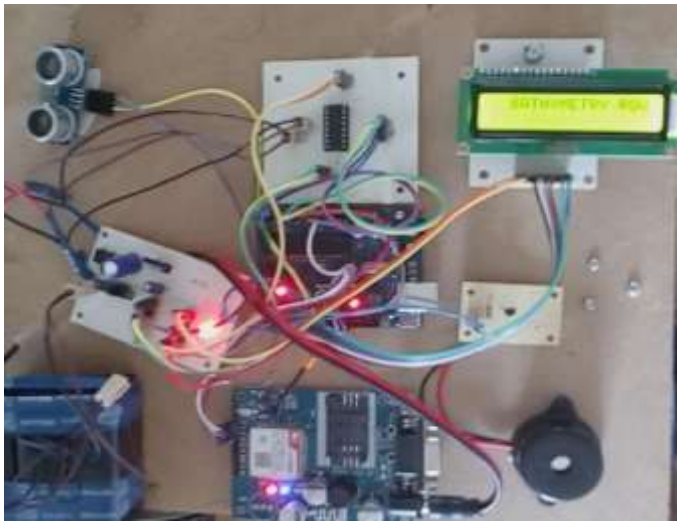


Fig 3 Bathymetry rover

HARDWARE INSTALATION

The information obtained from sensor is computed in Arduino for further processing and then the Arduino drives the DC motor according to the inputs. GPS get initialized when kit is turned on. It is shown in fig 4.

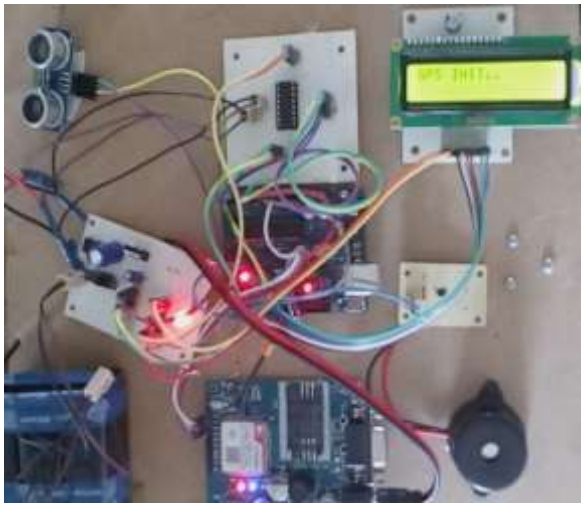


Fig 4 GPS initialization

DISPLAYING THE DISTANCE

When the sensor detects obstacles then the distance of obstacles displayed on the LCD and updates the distance in the server. It is shown in fig 5.

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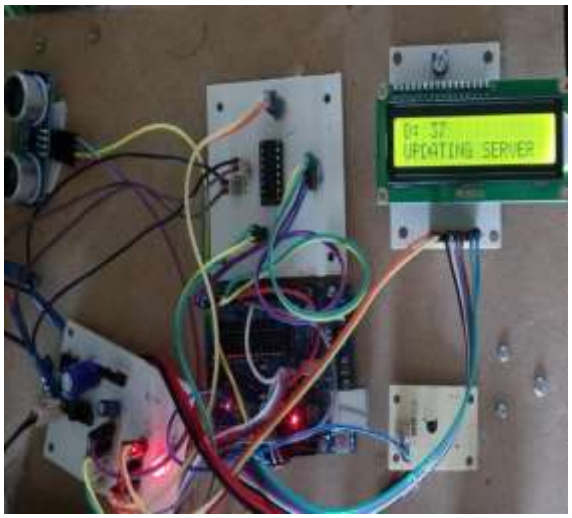

Fig 5 Displaying the Distance

UPDATING LATITUDE AND LONGITUDINAL VALUES ON WEB PAGE

Fig 6 Displaying latitude and longitude

Updating the latitude and longitudinal values which are given by GSM on web page it was created on server using PuTTY and also the pin location is displayed on Google Map and Shown in above image.

VI. CONCLUSION & FUTURE SCOPE

The proposed system is playing an important role in real time tracking and monitoring the rover and finding the water depths in lakes, sea and rivers. Knowledge of the Bathymetry has progressed quickly due to using advanced technologies like Acoustic, RADAR and optics. Maximum acoustic sounds are required to validate gravimetric Bathymetry in remote regions in the world.

FUTURE SCOPE

The Bathymetry rover system can be further improved by using multi beam sonar it is having greater resolution with greater productivity.

By the help of Airborne LIDAR Bathymetry (ALB) we can survey costal and land waters in single approach.

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DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

Certificate of Participation

This is to certify that Mr. /Ms. /Prof. /Dr. **G.Ravindranath** of **Matrusri Engineering College** has presented a paper titled **"A PROSTHETIC ARM BASED ON ELECTROENCEPHALOGRAPHY BY SIGNAL ACQUISITION AND PROCESSING ON MATLAB"** at **National Conference on Emerging Technologies in Energy Systems (NCETES-2020)** conducted in virtual mode by Department of Electrical and Electronics Engineering, Prasad V. Potluri Siddhartha Institute of Technology, Vijayawada, India held on 11th September 2020.

Dr. M.V.Ramesh	Dr. M. Venu Gopala Rao	Dr. K.Sivaji Babu
Co-ordinator	Co-Chairman	Principal

A PROSTHETIC ARM BASED ON ELECTROENCEPHALOGRAPHY BY SIGNAL ACQUISITION AND PROCESSING ON MATLAB

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Abstract— This paper presents the prosthetic arm based on electroencephalography by signal acquisition and processing. Around the world, there are 5-6 million people with partial hand amputation due to traumatic accidents, various health issues and wars. Recent advancements show prosthetic arms are purely mechanical and tedious. In order to solve this problem, Brain-Computer Interface (BCI)-based control strategies were introduced into robot control. The methods adopted should take into consideration the nature of the application, for example, Electroencephalography (EEG) signal is ideal for our application due to its convenient approach. Particularly, for EEG-based BCI systems, a set of sensors are needed to acquire the EEG signals from different brain areas. The Fast Fourier Transform algorithm is adopted for feature extraction of the EEG signals and python is used to save the data in .txt file. The .txt file is imported into MATLAB and data analysis is done by signal processing and analysis tool. Next, Signal classification is done and then the signal is carried to end-effector.

Keywords— Electroencephalography**, Brain-Computer Interface (BCI),** Steady state visual evoked potential (SSVEP), Fast Fourier Transform (FFT).

I. INTRODUCTION

The advancement of technologies in this era has great impacts on human life. Now, people are able to travel faster and communicate in a more convenient way than in the past. Assistive computers and machines provide conventional input devices such as a keyboard, a mouse, or a joystick to be operated by the users. These devices are, however, difficult to be used by elderly or disabled individuals. For this reason, special interfaces such as sip-and-puff systems, single switches, and eye-tracking systems have been proposed [1]. Nevertheless, these specials interfaces do not work for people suffering from severe neuromuscular diseases who cannot convey their intentions or operations to computers or machines with these interfaces. Consequently, even autonomous electric wheelchairs are unable to transport disabled people to their desired locations. Hence, there exists a growing demand and necessity for developing an alternative interface that can be used by the severely disabled population for communication with autonomous systems.

Brain-computer interface (BCI) system has been developed to address this challenge. BCIs are systems that can bypass conventional channels of communication [2]. A brain-computer interface (BCI) is a software and hardware system for establishing direct communication between human and computer, which enables people to send commands to the external world through brain activities, without depending on brain's normal output pathway of peripheral nerves and muscles activities [3]. BCI system is also useful to improve precision of control for vehicles and robots in hostile environments such as space, to let people live in intelligent e-homes, to integrate new electronics body enhancements, and to play and communicate in novel ways [4]. There are a vast group of control signals available for BCI systems. These signals can be generated at will by people, thus enabling BCI systems to interpret their intentions for command and control purposes. Particularly, in EEG-based BCI systems, the commonly used control signals are such as slow cortical potentials (SCP), event-related synchronization and desynchronization (ERS/ERD), event-related potentials (ERP), and visual evoked potentials (VEPs) [5]. The focus of this thesis is on steady-state visual evoked potential (SSVEP). In fact, when stimulated by a repetitive flicker of frequency 6 Hz and above, some sinusoidal oscillatory waveforms with the frequency same as the stimulus or its harmonics would be observed from the scalp of a person [6]-[8].

In this paper, a SSVEP-based BCI system for Robot Arm control is proposed. The system consists of a 16-channel EEG recording system for EEG measurement. Visual stimuli are developed on a laptop LCD screen for eliciting SSVEPs. Meanwhile, MATLAB is used as the main tool for signal processing of EEG signals and command recognition. The Fast Fourier Transform algorithm is adopted for feature extraction of the EEG signals. Signals are acquired by using a Bluetooth device EmotivEPOC + which is a 16-channels electrode, placed on the scalp and python is used to save the data in .txt file. The .txt file is imported into MATLAB and data analysis is done by signal processing and analysis tool. Frequency domain algorithm tool for generating the frequency response of the data and plotting Magnitude and phase diagram. Prior to controlling the movement of Robot Arm. Finally, the subjects are instructed to move the Robot Arm in specific directions and the performance of the system in real-time is observed and analysed.

II. Brain Computer Interface (BCI)

Generally, a typical BCI system comprises of five main consecutive stages, namely signal acquisition, signal pre-

processing or signal enhancement, feature extraction, classification, and the control interface. The signal acquisition stage captures the brain signals and may also perform noise reduction and artefact processing. The aim of pre-processing block is to bring the signals into a suitable form for further processing purposes. The discriminative information in the recorded brain signals are identified and extracted during the stage of feature extraction. Once measured, the signal is mapped onto a vector containing effective and discriminant features from the observed signals, upon which classification can be done. Feature extraction has always been a challenging task in BCI system because brain signals are mixed with other signals originated from a finite set of brain activities that overlap in both time and space. The classification block classifies the signals based on the constructed feature vectors. Hence, the choice of good discriminative features is essential to achieve effective pattern recognition so as to correctly decipher the user's intentions. Finally, control interface translates the classified signals into meaningful commands for any device connected, such as a wheelchair, Robot Arm or a computer.

A. Electroencephalography (EEG)

EEG is the recording of underlying human brain activity produced by the summation of electrical potentials generated by a large population of neurons which propagated through the skull. EEG is, as compared to MEG or fMRI, widely available, compact, inexpensive, usable at bedside, and offers a reasonable trade-off between temporal and spatial resolution [24]. The major drawback of EEG, however, is the low SNR due to the poor-quality signals that have to cross the scalp, skull, and many other layers before reaching the recording electrodes. In addition, EEG is greatly distorted by background noise generated either inside the brain or externally over the scalp. EEG often appears as an alternating type of electrical activity comprise of various frequencies with typical amplitude ranging from 2 to 100 µV. The early studies are more towards investigation of EEG for diagnosis of neurological disorders and cognitive neuroscience studies. As the EEG normally appears as random wave with various rhythms, quantitative measurement of EEG signal frequencies produces a convenient way to classify the signals. According to the frequency ranges that they occupy, EEG is categorized into several groups. As discussed in the above paragraphs, EEG is recorded by using electrodes. The placement of electrodes over the scalp is commonly based on the International 10-20 system which has been standardized by the American Electroencephalographic Society [6]. The system is based upon measurements of four standard points on the scalp, which is nasion, inion, left and right preauricular point the transverse and median planes divide the skull from these points. The electrode locations are determined by marking these planes at the intervals of 10% and 20% as shown in Figure.2. By following the standard procedure of 10-20 system, the electrode locations are reproducible on different subjects.
The EEG signal is measured as the potential difference over time between signal or active electrode and reference electrode, where the reference electrode will be the same for all channels.

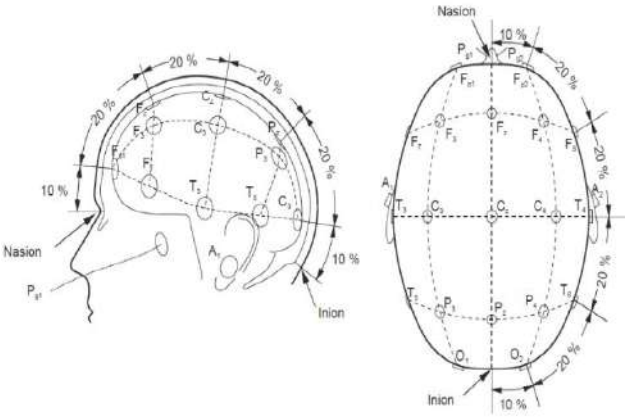

Figure 1: The International 10-20 electrode placement system

There is no standard position for common reference electrodes but normally an inactive position which provides a fairly constant electrical potential will be chosen. Midline position such as Cz and Fpz are sometimes used because they do not amplify the signal in any particular hemisphere. Multi-channel configurations can comprise up to 128 or 256 active electrodes. These electrodes are made up of silver chloride (AgCl). A good electrode application should create an electrical contact with ideal impedance of below 5 kΩ to record an accurate signal.

B. The SSVEP-Based Controlling System

SSVEP are usually elicited through cathode-ray tube (CRT) monitors, light-emitting diodes (LEDs), or liquid crystal display (LCD). Experimental results proved that the spectrum of LED flicker was very simple which includes only the fundamental frequency and its harmonics. It was found that there were many high frequency components related to the fresh frequency in the CRT spectrum low frequency components in the LCD flickers except for the fundamental frequency and its harmonics.
There are several factors that contribute to the quality of the elicited SSVEP. One experiment which investigates the influence of stimuli color on SSVEP-based BCI wheelchair control had been conducted by Singla *et al.* Four different stimuli colors were compared and experimental results showed that SSVEP response with violet stimuli are better than that with green, red, and blue stimuli besides, the patterns of the stimuli also affect the quality of the recorded signal. The commonly used patterns are such as letters, rectangles, checkerboards, or arrows which alternate between two colors or patterns at specific intervals.

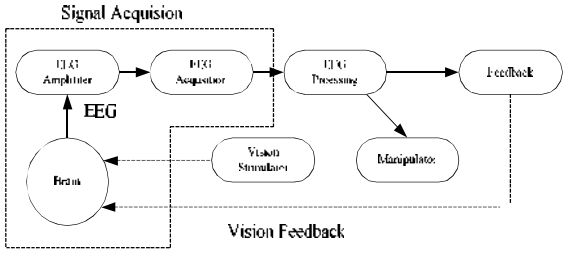

Figure 2: SSVEP based controlling system

III. IMPLEMENTATION

3.1 Hardware implementation

The hardware system was composed is 14 channel(2 reference channels) Emotiv EPOC+ signal acquisition device, Prosthetic arm, Arduino UNO/MEGA, Power Supply and Voltage Regulators.

EMOTIV EPOC+, this is the device used to acquire brain waves. Electrodes are placed on scalp. It is a wireless device, raw signals are saved in .txt file wirelessly using a Bluetooth device and a software, Emotiv Research Edition SDK v2.0.0.20 Installer which came along with the hardware package.

PROSTHETIC ARM, create an operative low-cost 3D printed prosthetic arm there are copious designs and making challenges. We aim to develop an apparent mechanical model of the arm and electrical system drives which determines the functionality resemblance of the device impersonating the human arm. The goal is to develop a prosthesis that has the ability to benefits people with missing hands. We aim to build an affordable prosthetic which is marginally available for amputees.
The modularity of the arm: Amputation can happen anywhere along the arm and is different in every case. We aim to design an ideal design that supports connection to a stump positioned anywhere along the arm. Scalability and Mathematical Model: The model should be so designed in order to have control over the degrees of freedom of the arm. The electrical motors should facilitate the free functioning of the arm. The arm should be strong enough to withhold the weights and any external stress and help in providing balance to the amputee.

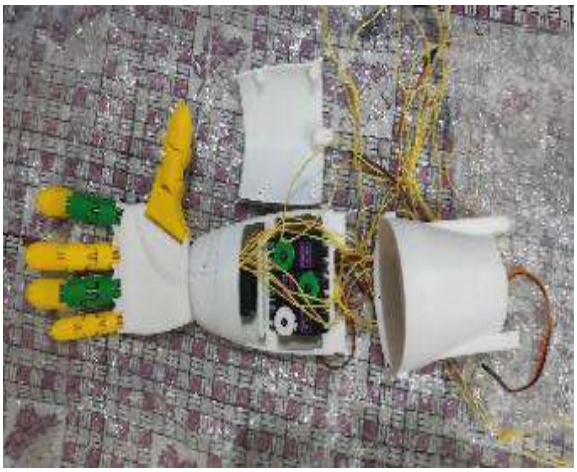

Fig.3. Fingers are controlled by tendons actuated through servo motors placed in the forearm

Arduino Uno is a microcontroller board based on the ATmega328P It has 14 digital input/output pins (of which 6 can be used as PWM outputs), 6 analog inputs, a 16 MHz quartz crystal, a USB connection, a power jack, an ICSP header and a reset button. It contains everything needed to support the microcontroller; simply connect it to a computer with a USB cable or power it with AC-to-DC adapter or battery to get started. The Arduino Uno can be programmed with the IDE (Arduino Software (IDE)).

3.2. Software Implementation

The software used for collecting the raw data from Emotiv PRO software and Emotiv Research Edition SDK v2.0.0.20 Installer for the process of signal pre-processing is MATLAB.

***Data Pre-Processing*:**

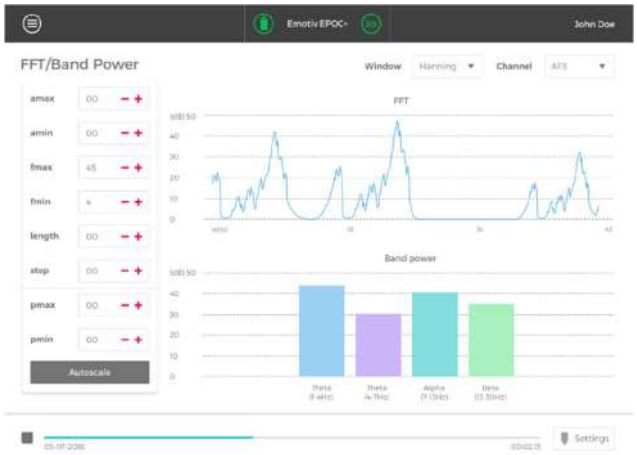

Fig. 4: EMOTIVPRO software

In Bandpass Filtering of raw EEG Signals, frequencies which do not fall within the alpha and beta bands are eliminated because they do not reflect visual processing in occipital region. This is achieved by constructing a 4th order Butterworth Infinite-Impulse Response (IIR) bandpass filter with a passband of 6 Hz to 30 Hz using the Signal Processing Toolbox in MATLAB. The main reason for selecting an IIR filters over Finite-Impulse Response (FIR) filters is due to the advantages of IIR filters which provide sharp cut-off with a much lower filter order and thus, low computational requirements as compared to FIR filters. Each electrode is connected to one input of a differential amplifier (one amplifier per pair of electrodes); a common system reference electrode is connected to the other input of each differential amplifier. Most EEG systems these days, however, are digital, and the amplified signal is digitized via an analog-to-digital converter, after being passed through an anti-aliasing filter. Analog-to-digital sampling typically occurs at 256–512 Hz in clinical scalp EEG; sampling rates of up to 20 kHz are used in some research applications. During the recording, a series of activation procedures may be used. The digital EEG signal is stored electronically and can be filtered for display. Typical settings for the high-pass filter and a low-pass filter are 0.5–1 Hz and 35–70 Hz respectively. The high-pass filter typically filters out slow artifact, such as electro galvanic signals and movement artifact, whereas the low-pass filter filters out high-frequency artifacts, such as electromyography signals. An additional notch filter is typically used to remove artefact caused by electrical power lines (60 Hz in the United States and 50 Hz in many other countries).

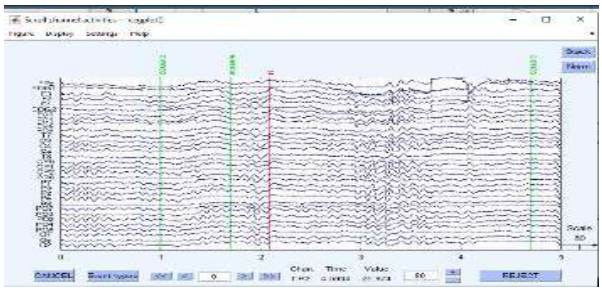

Fig.5. Raw EEG signal on Time Vs Amplitude curve

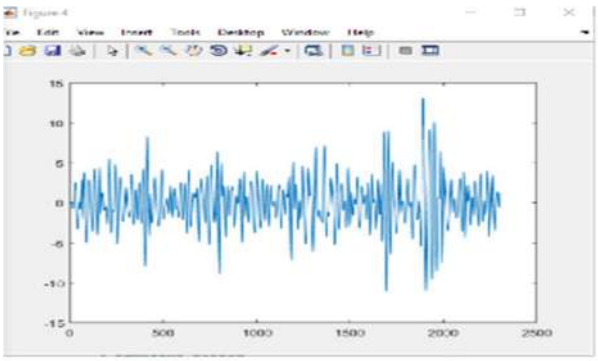

Fig.6. Filtered EEG signal on Time Vs Amplitude curve

Feature Extraction

For SSVEP-based BCI system, a method to extract the valid frequency in a relative short time is the core problem. As discussed previously, SSVEP response has the same fundamental frequency as the stimulus. Therefore, methods to determine the power spectrum in frequency domain can be employed to extract the meaningful EEG signal features. The power spectrum methods analyze the recorded EEG signals with the fast Fourier transform (FFT) algorithm of which the power for each frequency used in the BCI system is computed. In fact, Fourier transform is the most common method for examining the activity at different frequencies due to its low computational efforts, despite other feature extraction techniques such as wavelet transform (WT) are able to provide better time-frequency representation for the non-linear EEG signals. Zhang et al. had developed a CWT-based SSVEP classification method for BCI system. Although the experiment results showed that the implementation of wavelet transform provided precise measurements of how the frequency content of an EEG waveform changes over time, the method is not often used as it required higher computational effort but least necessity.

Signal Classification

Threshold frequency

In this work, the data classification is done by using threshold frequency, which is a relatively old classification technique developed by Vapnik and has shown to perform efficiently in several real-world problems, including BCI. Basically, SVM is a binary classifier that can separate two classes by using an optimal hyperplane which maximize the separating margin between the two classes.

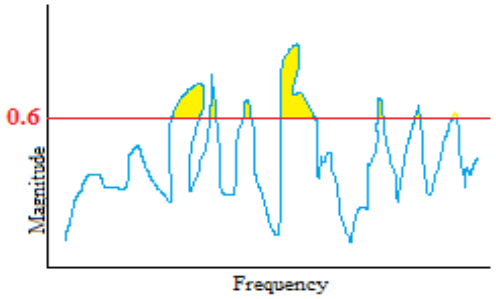

Figure 7: Classification by setting the Threshold Frequency

In this context, after signal pre-processing and feature extraction of the raw EEG data obtained, we are using machine learning for signal classification and training of the model. There are different classifiers like Multilayer Perceptron (MLPNN), Support Vector Machines (SVM), K-Nearest Neighbors (KNN) etc., which can be used for signal classification.

Multi-layered Perceptron Neural Network (MLPNN

Here we are implementing Multilayer Perceptron Neural Network (MLPNN) classifier. The architecture of MLPNN may contain two or more layers. A simple two-layer ANN consists only of an input layer containing the input variables to the problem and output layer containing the solution of the problem. This type of networks is a satisfactory approximator for linear problems. However, for approximating nonlinear systems, additional intermediate (hidden) processing layers are employed to handle the problem's nonlinearity and complexity. Although it depends on complexity of the function or the process being modelled, one hidden layer may be sufficient to map an arbitrary function to any degree of accuracy.

The determination of appropriate number of hidden layers is one of the most critical tasks in neural network design. The most popular approach to finding the optimal number of hidden layers is by trial and error. In the present study, MLPNN consisted of one input layer, one hidden layer with 21 nodes and one output layer. Training algorithms are an integral part of ANN model development. A good training algorithm will shorten the training time, while achieving a better accuracy. Therefore, training process is an important characteristic of the ANNs, whereby representative examples of the knowledge are iteratively presented to the network, so that it can integrate this knowledge within its structure. There are a number of training algorithms used to train a MLPNN and a frequently used one is called the backpropagation training algorithm which is based on searching an error surface using gradient descent for points with minimum error, is relatively easy to implement.

In this method, we use lifting-based discrete wavelet transform (LBDWT) coefficients of EEG signals as an input to classification system and obtain required discrete outputs. We provide faster wavelet decomposition in multi-channel EEG without any special hardware, by using LBDWT in a multi-channel EEG.

We can divide four-channel EEG recordings into sub-bands frequencies by using LBDWT. Since four-frequency band, which are alpha (D4), beta (D3), theta (D5) and delta (A5) is sufficient for the EEG signal processing, these wavelet sub-band frequencies (delta (1—4 Hz), theta (4—8 Hz), alpha (8—13 Hz), beta (13—30 Hz)) are applied to MLPNN input. Then we take the average of the four channels and give these wavelet coefficients (D3—D5 and A5) of EEG signals as an input to ANN. The MLPNN was designed with LBDWT coefficients (D3—D5 and A5) of EEG signal in the input layer; and the output layer consisted of one node representing whether movement of the prosthetic arm was detected or not. A value of "0" is assigned when the experimental investigation indicates no hand movement and "1" for a movement in hand.

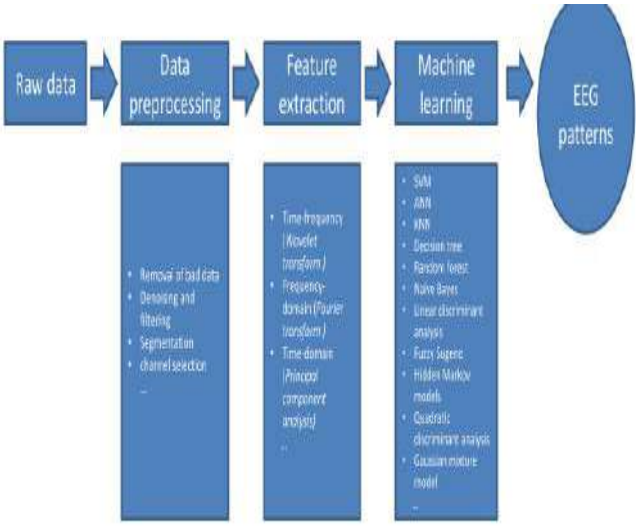

Fig.8. Flow chart EEG pattern

IV. RESULTS

We aim to develop a real-time SSVEP-based BCI system for command and control of prosthetic hand. For effective SSVEP response, which is dependent on color and size of flickers and distance (form observer to subject), the dominating one is color. 3 different colors red, violet and black are used to check out the optimal color which gave approximate frequency to the frequency of flickers.

Our objectives in this part work includes:

- Development of visual stimuli that give the best SSVEP response by using high timing precision software such as Psychophysics Toolbox from MATLAB
- Development and implementation of feature extraction and classification algorithms for real-time EEG signals processing and command recognition

Test conducted:

- Offline test- signals are taken, converted to .csv file then analyzed in MATLAB and transmitted to Arduino

Analysis of Different Brain Signals

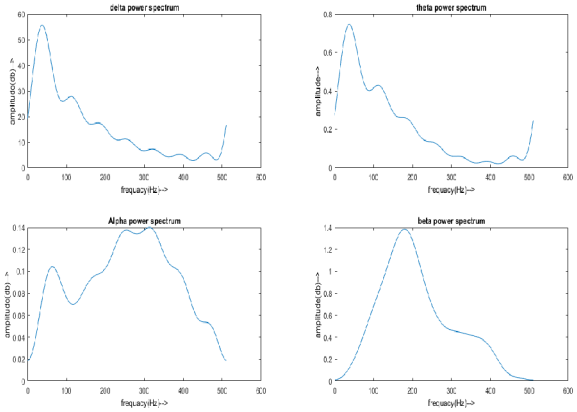

Fig.9. Brain Signals

Analysis of Different Alpha, Beta, Theta, Delta Signals in both Time and Frequency Domains

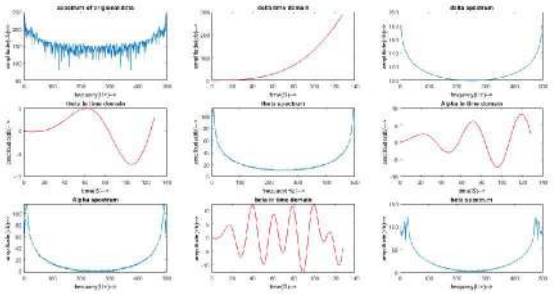

Fig.10. Alpha, Beta, Theta, Delta Signals

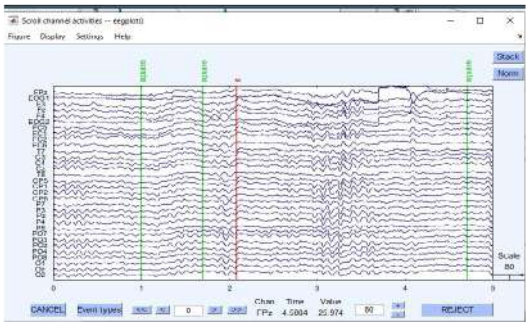

Fig.11.Raw EEG Signals with 32 Channel in EEGLAB

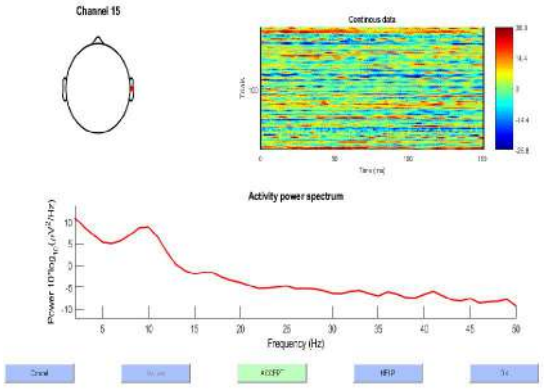

Fig.12 Individual Channel Response

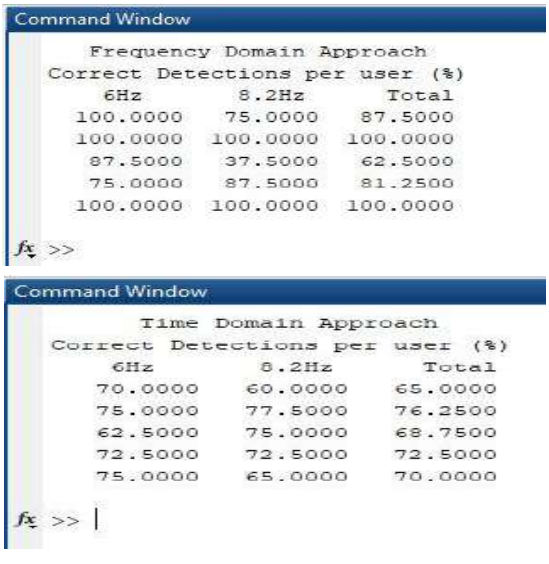

Fig.13.Matlab Command window for time and frequency domain

V. CONCLUSIONS

The paper discussed development and tested advanced prosthetic designs such as sophisticated EEG control algorithms, integrated pressure feedback and other advanced bio-mechatronic concepts and designs. With future growth of the 3D printing industry advanced printers and materials will allow students to develop more 'commercial-like' prosthetic devices – robust and durable systems that could benefit a wide range of peoples with a missing limb. With ongoing research improvements will hopefully lead to a system that is more durable and offers improved dexterity and control. Perhaps a future design will someday benefit amputees and improve the quality of people's lives.

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IDENTIFYING FRESHNESS OF A LEAF BASED ON COLOUR USING VECTOR QUANTIZATION METHOD

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***Abstract*- Quality of a leaf is influenced by its age and maturity. Edible leaves like spinach, fenugreek, curry leaves, etc., are mostly used in Indian Dishes, consumers depend on the sensory properties like appearance, colour, texture and aroma to assess the internal quality of the internal quality of the leaf. However, with the onset of automated food chains and IOT based food recognition applications, vegetables are identified by capturing their images and processing. IOT is effectively used to reduce waste, cost management and risks. For an instance, IoT facilitates food companies to ensure superior levels of traceability, food safety and, therefore accountability all through the farm-to-plate supplies chain operations. The IoT network in the food supply chain greatly helps in reducing waste, costs, and risks as well, in all stages of the procedure. In this paper a simple method is proposed to assess the quality of leafy vegetables based on its colour using vector quantization method. Cropped images are processed and fed to the algorithm to identify the number of colours in the algorithm.**

***Keywords*: k-means, IOT, colour identification, clustering, food monitoring**

I. INTRODUCTION

IOT in agriculture and food is still in early stages of development. Utilization of IOT in food chains and for food safety is increasing gradually. Food safety for perishable goods is of more concern [1]. To ensure food safety till it reaches the customer from the yield continuous food monitoring has to be done [5]. One of the highly used ingredients in Indian dishes is green leafy vegetables. Also, scientifically it is known as Spinciaoleracea Linn. (Family-Chenopodiaceae). The Spinach used as a food and has medicinal value also. Spinach bundled up with vitamins such as vitamin A, vitamin B, vitamin C and vitamin E and minerals like magnesium, manganese, iron, calcium and Folic acid. Spinach is great source of chlorophyll, which speedup digestion [7]. They are also highly perishable and have a very less shelf time as compared to other vegetables. There are varieties of green leaves that are edible and frequently used in Indian dishes like spinach, fenugreek leaves, coriander, curry leaves etc. spinach is used extensively in northern states of our country as well as southern states. There have been various algorithms used in recognizing leaves based on texture and outline characteristics [3]. Spinach leaves are a main source of calcium and are recommended as a regular diet for people with liver ailments. Spinach unlike fenugreek has a lesser shelf life and once the leaves start to lose their freshness they gradually lose their nutrition value. Freshness of a leaf is identified primarily by its colour [4]. When the leaves are placed in the shelf after harvesting they have a life span of one day without freezing and four days with freezing. Often, the leaves are kept in the fridge in super markets or at home. Monitoring perishable goods like spinach is essential in super markets to reduce loss and wastage. IOT can utilized to continuously monitor the freshness of the leaf and replace the product [2]. In this paper a solution is proposed to continuously monitor the product using a camera that captures pictures at regular intervals and directs to the central server. At the server the algorithm processes the images and sends a notification if the leaf is losing its freshness. A leaf is said to be fresh by looking at its colour, a bright green leaf is fresh, and a darker shade of green indicates an aged

leaf. A leaf with traces of brown colour can indicate spots or disease. Leaf that is yellowish could have less nutrition content and traces of black or dark brown could mean the leaf has started to decompose.

II. METHODOLOGY

A. Data Collected

Images of spinach leaves are collected from different sources using Samsung mobile camera. These images are primarily belonging to Spinach and hence images of a spinach leaf in different conditions are collected and fed to the algorithm. Leaves tend to change colour based on the environmental conditions and also the way in which they are stored. Also the time taken to store the leaf is very vital. The following common conditions are considered:

1. When the leaf is freshly plucked by hand.

2. When the leaf is plucked and maintained in cool temperatures for a day or two to retain freshness.

3. When the leaf was plucked after it aged on the plant itself

4. When the leaf has aged and also damaged without proper storage.

Images of leaves with bright green, dark green, yellowish and yellowish leaves with spots are used. Some of the images are presented below

Fig.1 Examples of the spinach leaves used in dataset

B. Procedure

The image is captured using a pinhole camera that is fixed inside the fridge or in a place where the leaves can be viewed properly. Images are captured at regular intervals and sent to a central server. The algorithm resides at the server that processes the images. The image is first cropped and only the leaf without the background is fed to the algorithm. The algorithm extracts the colours from the leaf and displays the percentage of each colour. Based on the amount of colour the server sends a notification to the client. The colours are identified using clustering K means algorithm is used to cluster the colours.

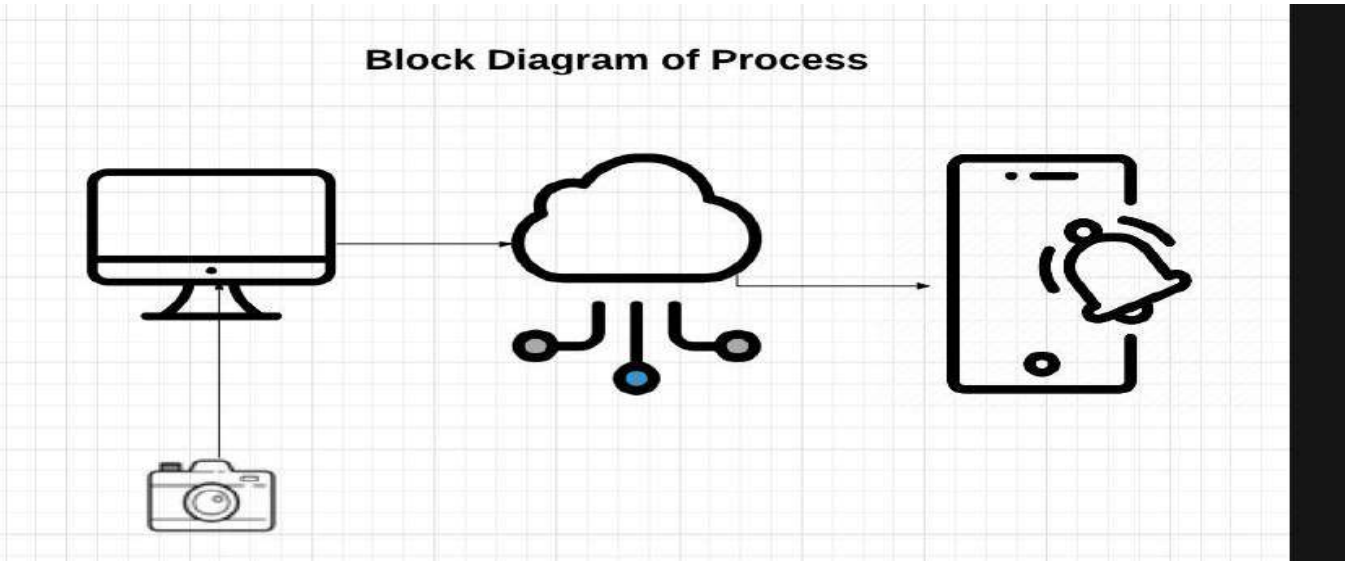


Fig. 4 A simple architecture depicting the process

The pre-processed and cropped images are fed to the algorithm that performs the following tasks:

1. Extract the RGB values of the image as hexadecimal numbers.

2. The image is then resized to a fixed height and width for uniformity.

3. The image is fed to the k-means clustering algorithm with the number of clusters as n. In our case the number of clusters depicts the number of colours. The clusters are formed using the following formula

$$J(V) = \sum_{i=1}^{c} \sum_{j=1}^{c_i} \left(\|x_i - v_j\| \right)^2$$

4. The hexadecimal values of the colours are then again converted back to RGB values and plotted on a Pie chart with the percentage of each colour.

The flow chart presented below depicts the process adopted to identify the colour of the leaf.

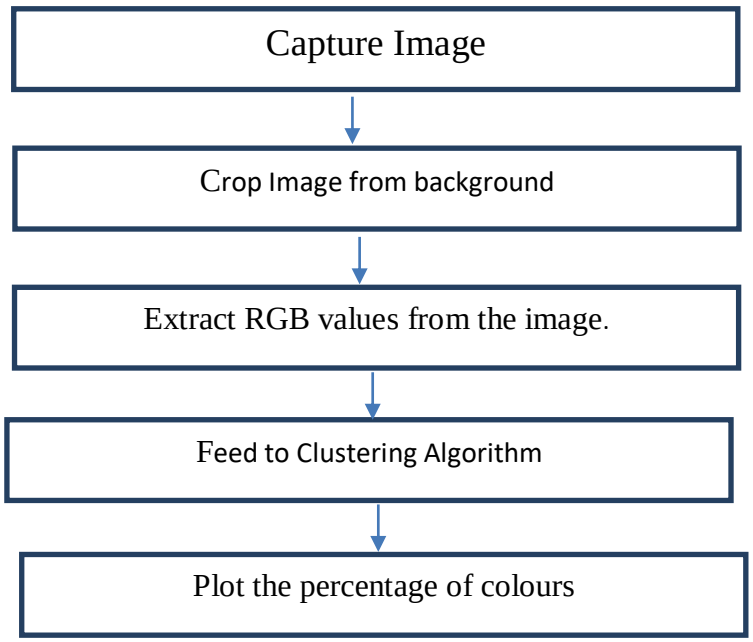


Fig. 2 Flow chart of the proposed solution

C. K means Clustering algorithm

k-means clustering is a method used for vector quantization, originating from signal processing which is popular among different cluster analysis methods in data mining[6]. k-means clustering aims to partition n observations into k clusters in which each observation belongs to the cluster with the nearest mean, serving as a prototype of the cluster. This results in a partitioning of the data space into Voronoi cells. k-Means minimizes within-cluster variances (squared Euclidean distances), but not regular Euclidean distances, which would be the more difficult Weber problem: the mean optimizes squared errors, whereas only the geometric median minimizes Euclidean distances. Better Euclidean solutions can for example be found using k-medians and k-medoids.

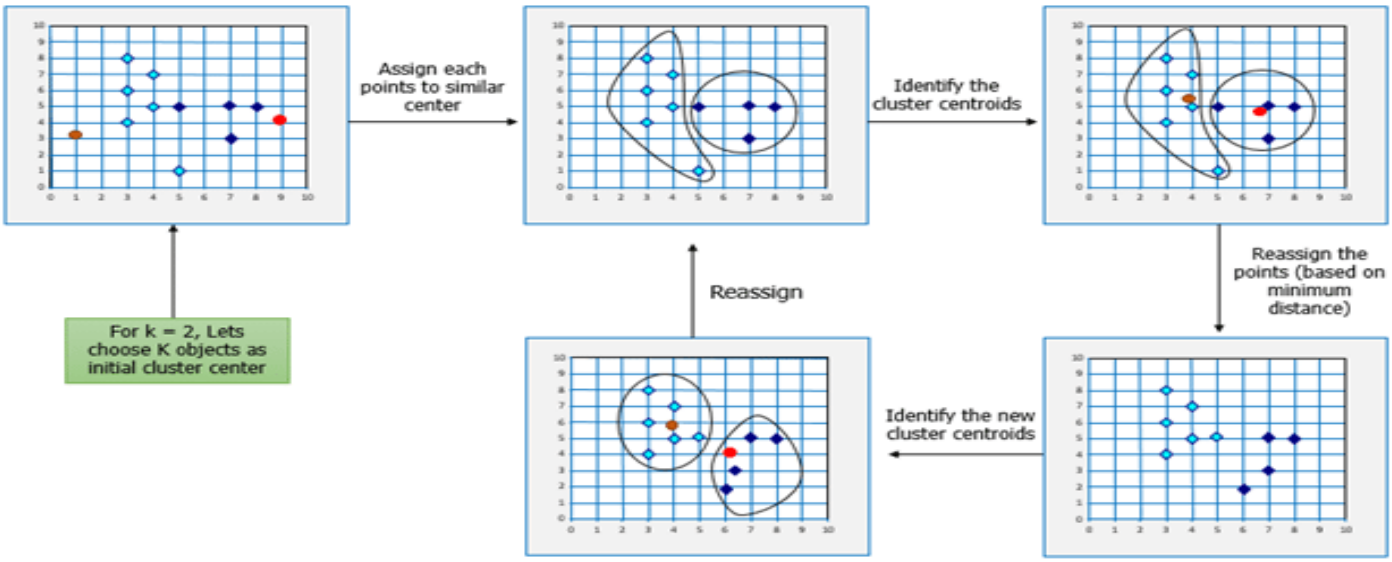
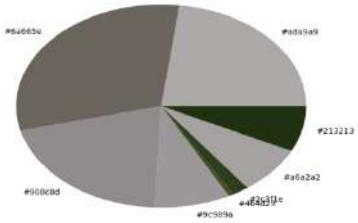
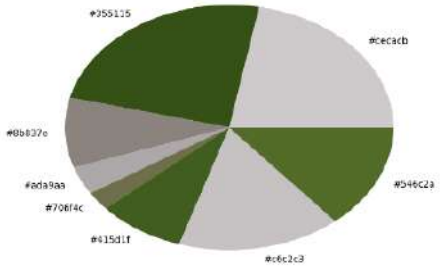


Fig. 3 A simple working model of K-means clustering

III EXPERIMENTAL RESULTS

Pre-processed images of the leaves were fed as input to the k-means clustering algorithm. The output of the algorithm is plotted using a pie chart in order to get a clear percentage of colours in the leaf. The results are presented as follows:





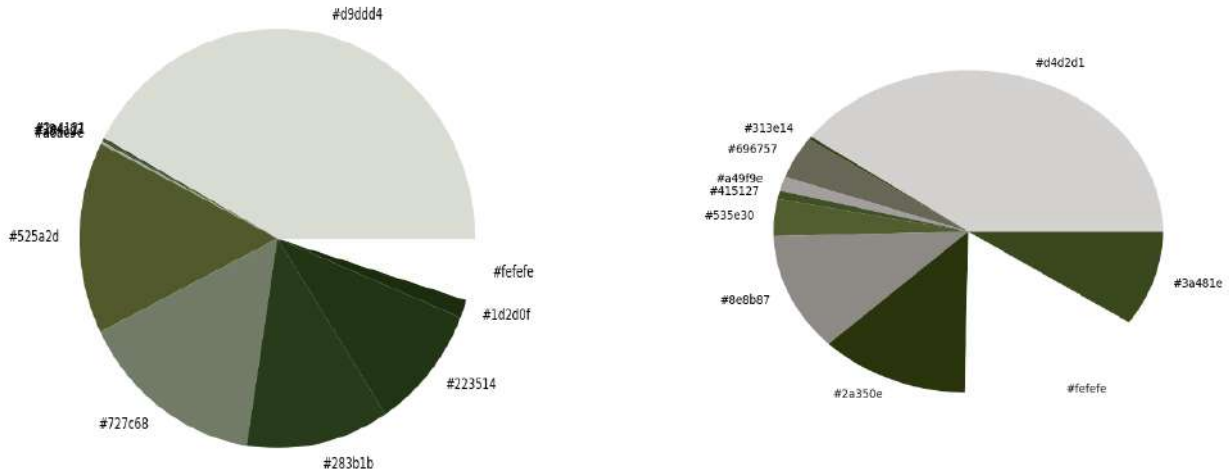


Fig 5: Results showing the colours extracted from four different leaves depicted in the previous section namely a,b,c and d.

IV CONCLUSION:

The approach proposed in this paper to identify the amount of colour present in an image of a leaf can be used to determine the freshness of a leaf. The application of this model is in food chain units where freshness of the food ,must be identified and retained. Automation of identification of the freshness using small pinhole camera with a microcontroller can be used to avoid food wastage. The percentage of different shades on the leaf is successfully extracted. Further, more work can be done to extract the amount of colour from images and predict if the leaf will decompose in a few days using machine learning algorithms. Also, notification can be sent to the store manager. More features of the leaf and its environment can be captured and predictions can be made.

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DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

Certificate of Participation

This is to certify that Mr. /Ms. /Prof. /Dr. **Vasudeva Naidu** of **Matrusri Engineering College** has presented a paper titled **"A PROSTHETIC ARM BASED ON ELECTROENCEPHALOGRAPHY BY SIGNAL ACQUISITION AND PROCESSING ON MATLAB"** at **National Conference on Emerging Technologies in Energy Systems (NCETES-2020)** conducted in virtual mode by Department of Electrical and Electronics Engineering, Prasad V. Potluri Siddhartha Institute of Technology, Vijayawada, India held on 11th September 2020.

Dr. M.V.Ramesh	Dr. M. Venu Gopala Rao	Dr. K.Sivaji Babu
Co-ordinator	Co-Chairman	Principal

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A PROSTHETIC ARM BASED ON ELECTROENCEPHALOGRAPHY BY SIGNAL ACQUISITION AND PROCESSING ON MATLAB

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Abstract— This paper presents the prosthetic arm based on electroencephalography by signal acquisition and processing. Around the world, there are 5-6 million people with partial hand amputation due to traumatic accidents, various health issues and wars. Recent advancements show prosthetic arms are purely mechanical and tedious. In order to solve this problem, Brain-Computer Interface (BCI)-based control strategies were introduced into robot control. The methods adopted should take into consideration the nature of the application, for example, Electroencephalography (EEG) signal is ideal for our application due to its convenient approach. Particularly, for EEG-based BCI systems, a set of sensors are needed to acquire the EEG signals from different brain areas. The Fast Fourier Transform algorithm is adopted for feature extraction of the EEG signals and python is used to save the data in .txt file. The .txt file is imported into MATLAB and data analysis is done by signal processing and analysis tool. Next, Signal classification is done and then the signal is carried to end-effector.

Keywords— Electroencephalography**, Brain-Computer Interface (BCI),** Steady state visual evoked potential (SSVEP), Fast Fourier Transform (FFT).

I. INTRODUCTION

The advancement of technologies in this era has great impacts on human life. Now, people are able to travel faster and communicate in a more convenient way than in the past. Assistive computers and machines provide conventional input devices such as a keyboard, a mouse, or a joystick to be operated by the users. These devices are, however, difficult to be used by elderly or disabled individuals. For this reason, special interfaces such as sip-and-puff systems, single switches, and eye-tracking systems have been proposed [1]. Nevertheless, these specials interfaces do not work for people suffering from severe neuromuscular diseases who cannot convey their intentions or operations to computers or machines with these interfaces. Consequently, even autonomous electric wheelchairs are unable to transport disabled people to their desired locations. Hence, there exists a growing demand and necessity for developing an alternative interface that can be used by the severely disabled population for communication with autonomous systems.

Brain-computer interface (BCI) system has been developed to address this challenge. BCIs are systems that can bypass conventional channels of communication [2]. A brain-computer interface (BCI) is a software and hardware system for establishing direct communication between human and computer, which enables people to send commands to the external world through brain activities, without depending on brain's normal output pathway of peripheral nerves and muscles activities [3]. BCI system is also useful to improve precision of control for vehicles and robots in hostile environments such as space, to let people live in intelligent e-homes, to integrate new electronics body enhancements, and to play and communicate in novel ways [4]. There are a vast group of control signals available for BCI systems. These signals can be generated at will by people, thus enabling BCI systems to interpret their intentions for command and control purposes. Particularly, in EEG-based BCI systems, the commonly used control signals are such as slow cortical potentials (SCP), event-related synchronization and desynchronization (ERS/ERD), event-related potentials (ERP), and visual evoked potentials (VEPs) [5]. The focus of this thesis is on steady-state visual evoked potential (SSVEP). In fact, when stimulated by a repetitive flicker of frequency 6 Hz and above, some sinusoidal oscillatory waveforms with the frequency same as the stimulus or its harmonics would be observed from the scalp of a person [6]-[8].

In this paper, a SSVEP-based BCI system for Robot Arm control is proposed. The system consists of a 16-channel EEG recording system for EEG measurement. Visual stimuli are developed on a laptop LCD screen for eliciting SSVEPs. Meanwhile, MATLAB is used as the main tool for signal processing of EEG signals and command recognition. The Fast Fourier Transform algorithm is adopted for feature extraction of the EEG signals. Signals are acquired by using a Bluetooth device EmotivEPOC + which is a 16-channels electrode, placed on the scalp and python is used to save the data in .txt file. The .txt file is imported into MATLAB and data analysis is done by signal processing and analysis tool. Frequency domain algorithm tool for generating the frequency response of the data and plotting Magnitude and phase diagram. Prior to controlling the movement of Robot Arm. Finally, the subjects are instructed to move the Robot Arm in specific directions and the performance of the system in real-time is observed and analysed.

II. Brain Computer Interface (BCI)

Generally, a typical BCI system comprises of five main consecutive stages, namely signal acquisition, signal pre-

processing or signal enhancement, feature extraction, classification, and the control interface. The signal acquisition stage captures the brain signals and may also perform noise reduction and artefact processing. The aim of pre-processing block is to bring the signals into a suitable form for further processing purposes. The discriminative information in the recorded brain signals are identified and extracted during the stage of feature extraction. Once measured, the signal is mapped onto a vector containing effective and discriminant features from the observed signals, upon which classification can be done. Feature extraction has always been a challenging task in BCI system because brain signals are mixed with other signals originated from a finite set of brain activities that overlap in both time and space. The classification block classifies the signals based on the constructed feature vectors. Hence, the choice of good discriminative features is essential to achieve effective pattern recognition so as to correctly decipher the user's intentions. Finally, control interface translates the classified signals into meaningful commands for any device connected, such as a wheelchair, Robot Arm or a computer.

A. Electroencephalography (EEG)

EEG is the recording of underlying human brain activity produced by the summation of electrical potentials generated by a large population of neurons which propagated through the skull. EEG is, as compared to MEG or fMRI, widely available, compact, inexpensive, usable at bedside, and offers a reasonable trade-off between temporal and spatial resolution [24]. The major drawback of EEG, however, is the low SNR due to the poor-quality signals that have to cross the scalp, skull, and many other layers before reaching the recording electrodes. In addition, EEG is greatly distorted by background noise generated either inside the brain or externally over the scalp. EEG often appears as an alternating type of electrical activity comprise of various frequencies with typical amplitude ranging from 2 to 100 µV. The early studies are more towards investigation of EEG for diagnosis of neurological disorders and cognitive neuroscience studies. As the EEG normally appears as random wave with various rhythms, quantitative measurement of EEG signal frequencies produces a convenient way to classify the signals. According to the frequency ranges that they occupy, EEG is categorized into several groups. As discussed in the above paragraphs, EEG is recorded by using electrodes. The placement of electrodes over the scalp is commonly based on the International 10-20 system which has been standardized by the American Electroencephalographic Society [6]. The system is based upon measurements of four standard points on the scalp, which is nasion, inion, left and right preauricular point the transverse and median planes divide the skull from these points. The electrode locations are determined by marking these planes at the intervals of 10% and 20% as shown in Figure.2. By following the standard procedure of 10-20 system, the electrode locations are reproducible on different subjects.
The EEG signal is measured as the potential difference over time between signal or active electrode and reference electrode, where the reference electrode will be the same for all channels.

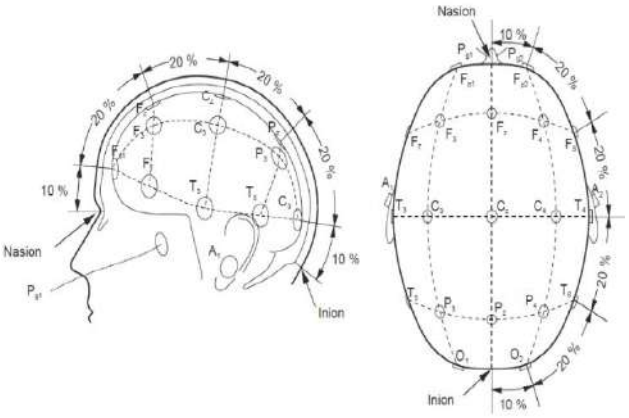

Figure 1: The International 10-20 electrode placement system

There is no standard position for common reference electrodes but normally an inactive position which provides a fairly constant electrical potential will be chosen. Midline position such as Cz and Fpz are sometimes used because they do not amplify the signal in any particular hemisphere. Multi-channel configurations can comprise up to 128 or 256 active electrodes. These electrodes are made up of silver chloride (AgCl). A good electrode application should create an electrical contact with ideal impedance of below 5 kΩ to record an accurate signal.

B. The SSVEP-Based Controlling System

SSVEP are usually elicited through cathode-ray tube (CRT) monitors, light-emitting diodes (LEDs), or liquid crystal display (LCD). Experimental results proved that the spectrum of LED flicker was very simple which includes only the fundamental frequency and its harmonics. It was found that there were many high frequency components related to the fresh frequency in the CRT spectrum low frequency components in the LCD flickers except for the fundamental frequency and its harmonics.
There are several factors that contribute to the quality of the elicited SSVEP. One experiment which investigates the influence of stimuli color on SSVEP-based BCI wheelchair control had been conducted by Singla *et al.* Four different stimuli colors were compared and experimental results showed that SSVEP response with violet stimuli are better than that with green, red, and blue stimuli besides, the patterns of the stimuli also affect the quality of the recorded signal. The commonly used patterns are such as letters, rectangles, checkerboards, or arrows which alternate between two colors or patterns at specific intervals.

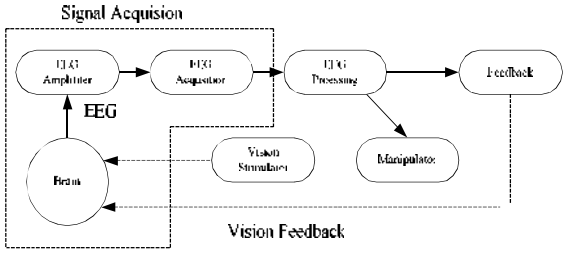

Figure 2: SSVEP based controlling system

III. IMPLEMENTATION

3.1 Hardware implementation

The hardware system was composed is 14 channel(2 reference channels) Emotiv EPOC+ signal acquisition device, Prosthetic arm, Arduino UNO/MEGA, Power Supply and Voltage Regulators.

EMOTIV EPOC+, this is the device used to acquire brain waves. Electrodes are placed on scalp. It is a wireless device, raw signals are saved in .txt file wirelessly using a Bluetooth device and a software, Emotiv Research Edition SDK v2.0.0.20 Installer which came along with the hardware package.

PROSTHETIC ARM, create an operative low-cost 3D printed prosthetic arm there are copious designs and making challenges. We aim to develop an apparent mechanical model of the arm and electrical system drives which determines the functionality resemblance of the device impersonating the human arm. The goal is to develop a prosthesis that has the ability to benefits people with missing hands. We aim to build an affordable prosthetic which is marginally available for amputees.
The modularity of the arm: Amputation can happen anywhere along the arm and is different in every case. We aim to design an ideal design that supports connection to a stump positioned anywhere along the arm. Scalability and Mathematical Model: The model should be so designed in order to have control over the degrees of freedom of the arm. The electrical motors should facilitate the free functioning of the arm. The arm should be strong enough to withhold the weights and any external stress and help in providing balance to the amputee.

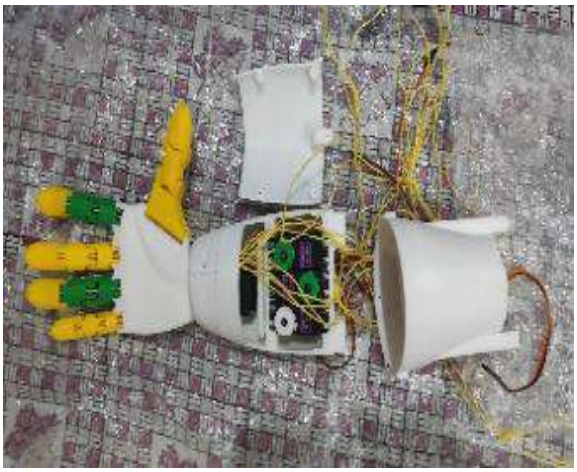

Fig.3. Fingers are controlled by tendons actuated through servo motors placed in the forearm

Arduino Uno is a microcontroller board based on the ATmega328P It has 14 digital input/output pins (of which 6 can be used as PWM outputs), 6 analog inputs, a 16 MHz quartz crystal, a USB connection, a power jack, an ICSP header and a reset button. It contains everything needed to support the microcontroller; simply connect it to a computer with a USB cable or power it with AC-to-DC adapter or battery to get started. The Arduino Uno can be programmed with the IDE (Arduino Software (IDE)).

3.2. Software Implementation

The software used for collecting the raw data from Emotiv PRO software and Emotiv Research Edition SDK v2.0.0.20 Installer for the process of signal pre-processing is MATLAB.

***Data Pre-Processing*:**

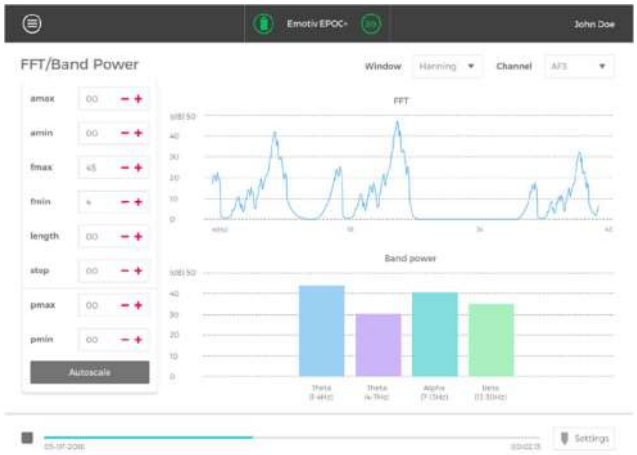

Fig. 4: EMOTIVPRO software

In Bandpass Filtering of raw EEG Signals, frequencies which do not fall within the alpha and beta bands are eliminated because they do not reflect visual processing in occipital region. This is achieved by constructing a 4th order Butterworth Infinite-Impulse Response (IIR) bandpass filter with a passband of 6 Hz to 30 Hz using the Signal Processing Toolbox in MATLAB. The main reason for selecting an IIR filters over Finite-Impulse Response (FIR) filters is due to the advantages of IIR filters which provide sharp cut-off with a much lower filter order and thus, low computational requirements as compared to FIR filters. Each electrode is connected to one input of a differential amplifier (one amplifier per pair of electrodes); a common system reference electrode is connected to the other input of each differential amplifier. Most EEG systems these days, however, are digital, and the amplified signal is digitized via an analog-to-digital converter, after being passed through an anti-aliasing filter. Analog-to-digital sampling typically occurs at 256–512 Hz in clinical scalp EEG; sampling rates of up to 20 kHz are used in some research applications. During the recording, a series of activation procedures may be used. The digital EEG signal is stored electronically and can be filtered for display. Typical settings for the high-pass filter and a low-pass filter are 0.5–1 Hz and 35–70 Hz respectively. The high-pass filter typically filters out slow artifact, such as electro galvanic signals and movement artifact, whereas the low-pass filter filters out high-frequency artifacts, such as electromyography signals. An additional notch filter is typically used to remove artefact caused by electrical power lines (60 Hz in the United States and 50 Hz in many other countries).

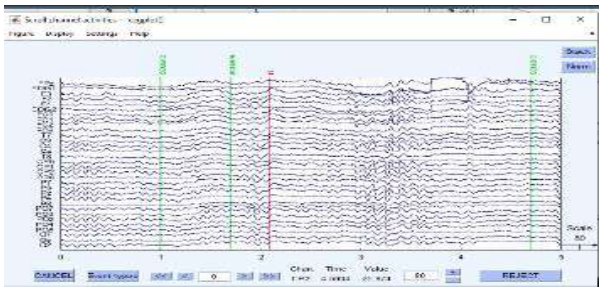

Fig.5. Raw EEG signal on Time Vs Amplitude curve

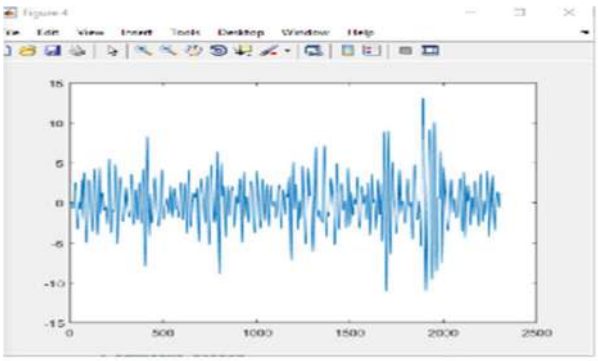

Fig.6. Filtered EEG signal on Time Vs Amplitude curve

Feature Extraction

For SSVEP-based BCI system, a method to extract the valid frequency in a relative short time is the core problem. As discussed previously, SSVEP response has the same fundamental frequency as the stimulus. Therefore, methods to determine the power spectrum in frequency domain can be employed to extract the meaningful EEG signal features. The power spectrum methods analyze the recorded EEG signals with the fast Fourier transform (FFT) algorithm of which the power for each frequency used in the BCI system is computed. In fact, Fourier transform is the most common method for examining the activity at different frequencies due to its low computational efforts, despite other feature extraction techniques such as wavelet transform (WT) are able to provide better time-frequency representation for the non-linear EEG signals. Zhang et al. had developed a CWT-based SSVEP classification method for BCI system. Although the experiment results showed that the implementation of wavelet transform provided precise measurements of how the frequency content of an EEG waveform changes over time, the method is not often used as it required higher computational effort but least necessity.

Signal Classification

Threshold frequency

In this work, the data classification is done by using threshold frequency, which is a relatively old classification technique developed by Vapnik and has shown to perform efficiently in several real-world problems, including BCI. Basically, SVM is a binary classifier that can separate two classes by using an optimal hyperplane which maximize the separating margin between the two classes.

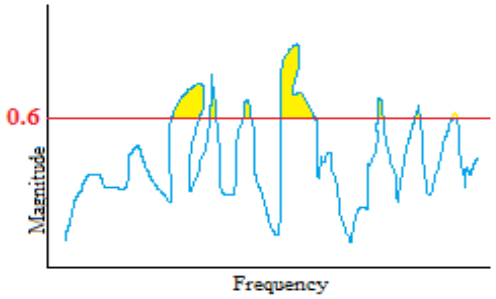

Figure 7: Classification by setting the Threshold Frequency

In this context, after signal pre-processing and feature extraction of the raw EEG data obtained, we are using machine learning for signal classification and training of the model. There are different classifiers like Multilayer Perceptron (MLPNN), Support Vector Machines (SVM), K-Nearest Neighbors (KNN) etc., which can be used for signal classification.

Multi-layered Perceptron Neural Network (MLPNN

Here we are implementing Multilayer Perceptron Neural Network (MLPNN) classifier. The architecture of MLPNN may contain two or more layers. A simple two-layer ANN consists only of an input layer containing the input variables to the problem and output layer containing the solution of the problem. This type of networks is a satisfactory approximator for linear problems. However, for approximating nonlinear systems, additional intermediate (hidden) processing layers are employed to handle the problem's nonlinearity and complexity. Although it depends on complexity of the function or the process being modelled, one hidden layer may be sufficient to map an arbitrary function to any degree of accuracy.

The determination of appropriate number of hidden layers is one of the most critical tasks in neural network design. The most popular approach to finding the optimal number of hidden layers is by trial and error. In the present study, MLPNN consisted of one input layer, one hidden layer with 21 nodes and one output layer. Training algorithms are an integral part of ANN model development. A good training algorithm will shorten the training time, while achieving a better accuracy. Therefore, training process is an important characteristic of the ANNs, whereby representative examples of the knowledge are iteratively presented to the network, so that it can integrate this knowledge within its structure. There are a number of training algorithms used to train a MLPNN and a frequently used one is called the backpropagation training algorithm which is based on searching an error surface using gradient descent for points with minimum error, is relatively easy to implement.

In this method, we use lifting-based discrete wavelet transform (LBDWT) coefficients of EEG signals as an input to classification system and obtain required discrete outputs. We provide faster wavelet decomposition in multi-channel EEG without any special hardware, by using LBDWT in a multi-channel EEG.

We can divide four-channel EEG recordings into sub-bands frequencies by using LBDWT. Since four-frequency band, which are alpha (D4), beta (D3), theta (D5) and delta (A5) is sufficient for the EEG signal processing, these wavelet sub-band frequencies (delta (1—4 Hz), theta (4—8 Hz), alpha (8—13 Hz), beta (13—30 Hz)) are applied to MLPNN input. Then we take the average of the four channels and give these wavelet coefficients (D3—D5 and A5) of EEG signals as an input to ANN. The MLPNN was designed with LBDWT coefficients (D3—D5 and A5) of EEG signal in the input layer; and the output layer consisted of one node representing whether movement of the prosthetic arm was detected or not. A value of "0" is assigned when the experimental investigation indicates no hand movement and "1" for a movement in hand.

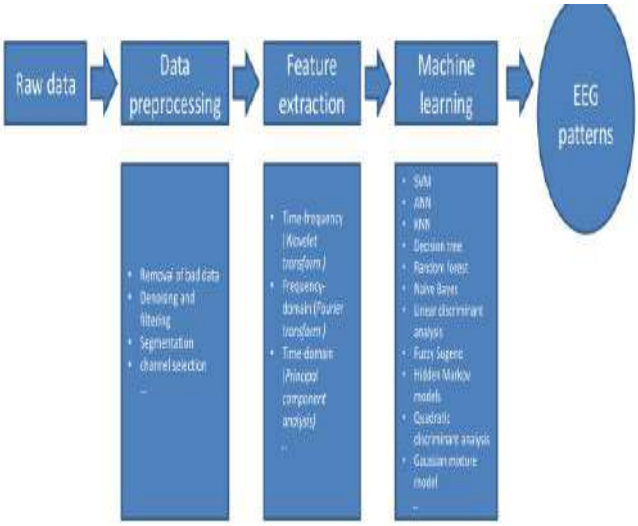

Fig.8. Flow chart EEG pattern

IV. RESULTS

We aim to develop a real-time SSVEP-based BCI system for command and control of prosthetic hand. For effective SSVEP response, which is dependent on color and size of flickers and distance (form observer to subject), the dominating one is color. 3 different colors red, violet and black are used to check out the optimal color which gave approximate frequency to the frequency of flickers.

Our objectives in this part work includes:

- Development of visual stimuli that give the best SSVEP response by using high timing precision software such as Psychophysics Toolbox from MATLAB
- Development and implementation of feature extraction and classification algorithms for real-time EEG signals processing and command recognition

Test conducted:

- Offline test- signals are taken, converted to .csv file then analyzed in MATLAB and transmitted to Arduino

Analysis of Different Brain Signals

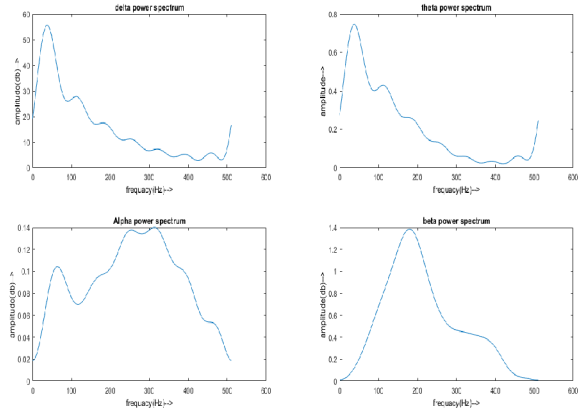

Fig.9. Brain Signals

Analysis of Different Alpha, Beta, Theta, Delta Signals in both Time and Frequency Domains

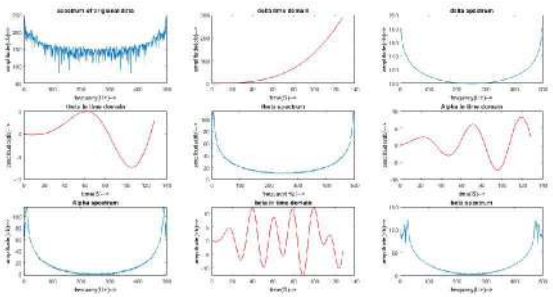

Fig.10. Alpha, Beta, Theta, Delta Signals

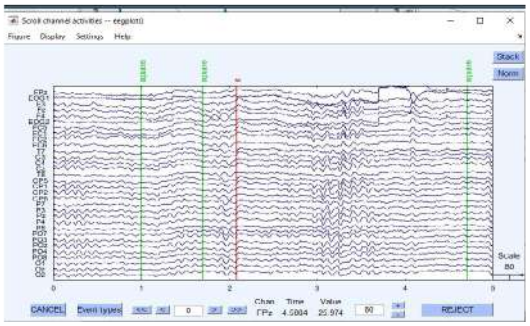

Fig.11.Raw EEG Signals with 32 Channel in EEGLAB

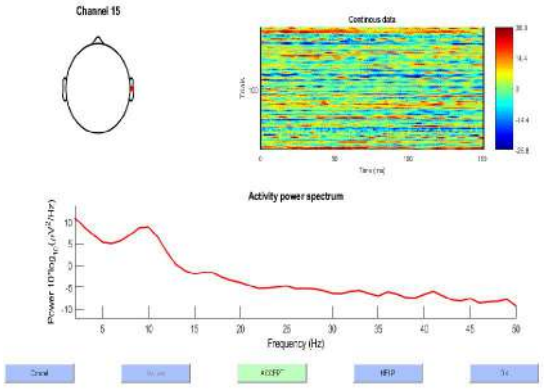

Fig.12 Individual Channel Response

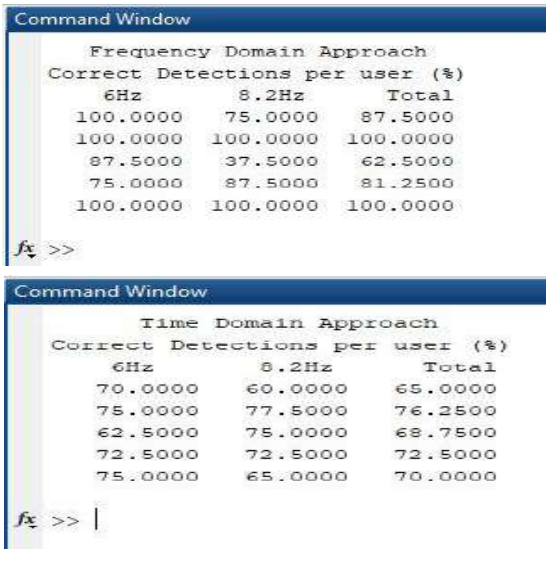

Fig.13.Matlab Command window for time and frequency domain

V. CONCLUSIONS

The paper discussed development and tested advanced prosthetic designs such as sophisticated EEG control algorithms, integrated pressure feedback and other advanced bio-mechatronic concepts and designs. With future growth of the 3D printing industry advanced printers and materials will allow students to develop more 'commercial-like' prosthetic devices – robust and durable systems that could benefit a wide range of peoples with a missing limb. With ongoing research improvements will hopefully lead to a system that is more durable and offers improved dexterity and control. Perhaps a future design will someday benefit amputees and improve the quality of people's lives.

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A Comprehensive Study on EEG Signals for Seizure Detection Techniques

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Abstract. **Convulsions is a medical condition that affect the nervous system of human body. In medical language it is called as seizures. It is not a disease but it is a disorder, it usually occurs in the human brain of all the age groups irrespective of their age, starting from child age group to adults. It is usually caused by sudden change in the brain or a sudden electrical activity that occurs in the brain. Based on the duration, Convulsions are classified into different types, they are local convulsions, focal convulsion, generalized tonic clonic convulsions and partial convulsions. Convulsions will usually occur in the trauma patients [Road traffic accidents] and Post-operative i.e., brain surgery patients, alcoholic [drunker], stress life style conditions and Hypocalcaemia patients [Low calcium levels]. This detection is possible by analyzing the electroencephalogram (EEG) signals. Confluent advantages of all product functions (PFs) are once again transmitted in the high-performance genetic algorithm (GA)-technique to the same division model. Average classification accuracy of the GA-SVM technique is approximately more than 89.01% in all attempts.**

Keywords—EEG signals, LMD,GA-SVM, FPGA

I. INTRODUCTION

A Convulsion is a nervous system ailment [1] [2]. It is usually diagnosed by using EEG [3][4][5] are also called as Electroencephalogram, which is a process of scanning the brain by keeping electrodes around the head and it is also called as nerve conduction studies, abnormalities in the brain can be detected by these NCS Studies. These brain abnormalities can be diagnosed by a Neurologist..

According to frequency spectrum, we have 5 internal bands on Electromagnetic diaphragm Information: $\mathfrak{X}$ (0-5HZ), ϕ (3-7Hz), α (6-16Hz), β (14-29Hz) and γ (28-58Hz). To determine brain information, the above signal range of information is more suitable than the EEG signal. These above signal information will play an important role in the detection of internal nerve system, which is well compared to the conventional method.

In 20th century, researches are performed with the advanced proposed model, Signals method is used to easily identify and diagnose the problem in the early stage in Convulsion [6] [7] have divided into bi-directional ways they are: interictal fault finding and convulsion seizures analysis. It is the process in which all diagnosis of Convulsions in EEG signals, all the diagnosis was categorized under four methods.

Experimental results those references have related that both dynamics techniques are used to identify perfect values of EEG signal information. Experimental sections are used to determine actual behavior, and the also used to find out the all the parameters of proposed method, and the mixed presentation of this technique yields in a more important issues in separating the simple interictal and in the proposed method information.

Local mean dissolution, [8] [9] it is used to breakdown EEG signal information into a period of magnitude and frequency changing Techniques. By the application of Local mean dissolution signal, magnitude and frequency change methods .In that information was breakdown into a set of product functions (PF's), every information will be validated by all the parameters of the basic processing of the frequency variation technique. The process of local mean dissolution is similar to that of Electromagnetic diaphragm, and two of them are similar to the model of iteratively resolving internal components from the first to the last frequency changes. Therefore, its cost indicating that local mean dissolution has last simulation complexity and maximum processing speed when related to Electromagnetic diaphragm.

According to this review, it is a powerful elegant technique for resolving the proposed signal information. In this proposed technique, it is elaborated in detail. Initially, Local mean dissolution is used to convert raw medical signals into large PFs. [10]

It needs to be increased in the mirror enhancing method. It is allowed to decrease the small effect signal information before Local mean dissolution is going to be adopted. Therefore, the minimum advantages of the starting 5 Product functions along with the proposed, including the p-value bottom than 0.001 information has been identified and gave a mixture advantages, where it changes to transform into the excellent analyzer, i.e., GA-technique for standard measurement.

The remaining sections are ordered like. II part explain about EEG.

In this paper, it contains part I- Introduction, Part II- Related work, Part III- Comparison and performance and Part IV. Conclusion, future scope.

II. RELATED WORKS

In this paper they are introducing about Convulsions Ailment [11] EEG dataset is divided into five different subsets (A-E) that are labeled as Z, O, N, F and S. Each subset having hundred slots EEG slot with every information having twenty three. Six seconds period**.** In these first and second Sets are gathered extra cranially and saved from five healthy volunteers with Conventional Ten-Twenty electrode arrangement method with eyes set & reset**.** Subsets C&D are recorded from the brain (C) when the patients are in out of convulsions and epileptogenic zones (D). Subset E is only consists seizure information related to seizure attacks. These all EEG subsets are digitalized at converting at a 154.52 Hertz with the help of 12-bit ADC using resolution parameter.

A) LMD-Local Mean Decomposition

LMD technique is identified to separate the product functions (PF's) by the standard EEG information by smoothen the source information. In this separation, amplitude modulation will take place which results using envelope estimation [12] [13] by considering the arbitrary signal x (t). Find out internal all extremal nodes n, then the i^{th} internal mean value m_i of two adjacent extremal nodes information are determined by

$$m_i = \frac{(n_i + n_i + 1)}{2}$$

The local magnitude a_i of two adjacent extrema is given as

$$a_i = \frac{(n_i - n_i + 1)}{2}$$

Subtract the local mean function $m_{11}(t)$ from the original signal x(t) $h(t)=x(t)-m_{11}(t)$

$h_{11}(t)$ is divided with $a_{11}(t)$, then we will get demodulated component $s_{11}(t)$

$$s_{11}(t)=h(t)/a_{11}(t)$$

After n times demodulation of the EGG signal we are getting the n(t). The recursive equation is given as

$h_{11}(t)=x(t)-m_{11}(t)$,
$h_{12}(t)=s_{11}(t)- m_{12}(t).h_1n(t)=s_1(n-1)(t)-m_1.n(t)$

After multiplication of find out all internal values $a_{11}(t)...a1n(t)$ with integrated envelope is

$$a_1(t)=a_{11}(t)a_{12}(t)....a_1n(t)$$

Fractional dimension (FD): FD=log (lm (k))/log (1/k)
Renvy entropy (RE): RE=-sum (p_k, log p_k)
Hurst exponent (HE): Parameter which can be used regularly for calculating internal data nodes, expectations, the range of far dependence for time savings**.** Classifications of these are based on their accuracy BPNN-feed forward neural network, KNN-data mining field, LDN-versatile technique, SVM-machine learning technique, GA-SVM-advanced technique of SVM

$$Sensitivity(SEN) = \frac{TP}{TP+FN} X100\%$$

$$Specificity(SEP) = \frac{TN}{TN+FP} X100\%$$

$$Accuracy(ACC) = \frac{TP+TN}{TP+TN+FN} X100\%$$

B) GA-SVM

This is mainly focused on classification & feature extraction. Feature extraction of EGG signals mainly in time Slot or may be in frequency Slot or wavelet based Slot**.** Based upon 2016 paper SVM having more accuracy then remaining other classification due to that reason we are moving with SVM technology further SVM is an artificial neural network for automatic classification to get more accuracy**.** Wavelet transform is more familiar of EGG information to generate the AI System**.** In previous paper we are getting more accuracy from SVM technology [14] which was high (i.e. 97% for Convulsions)**.**

The division of methods is categorized on their calculated advantages. Division of methods -SVM, ANN, LDA. Recently lot of techniques is in valuable to identify the seizure Ailment. Some of the works listed below.

Elhosary: Proposed a hardware structure for seizure detection application by developing a SVM training, feature extraction and classification process WANG et al: A hardware design for seizure detection was proposed [7].

Manish et al: Also utilized the same classifier along with some advanced method to decay the EEG signal information into noted bands. And fractal dimensions for seizure selection. This LS-SVM classifier reduced the computational complexities than SVM classifier [8].

Feng et al: Utilized Daubechies DWT for extracting the time-frequency Slot features which reflected the characteristics of non-stationary signals. They also utilized the same SVM classifier for classification. [12].

Rout et al: in this Technique problem identification way, by combining the vibrational model decay (VMD), Hilbert transform (HT), and by the techniques of faults reduced methods. [14].

III. COMPARISON AND PERFORMANCE

1. LMD method: The below flow chart shows LMD method. The following flow chart will gives the entire process of signal flowing.

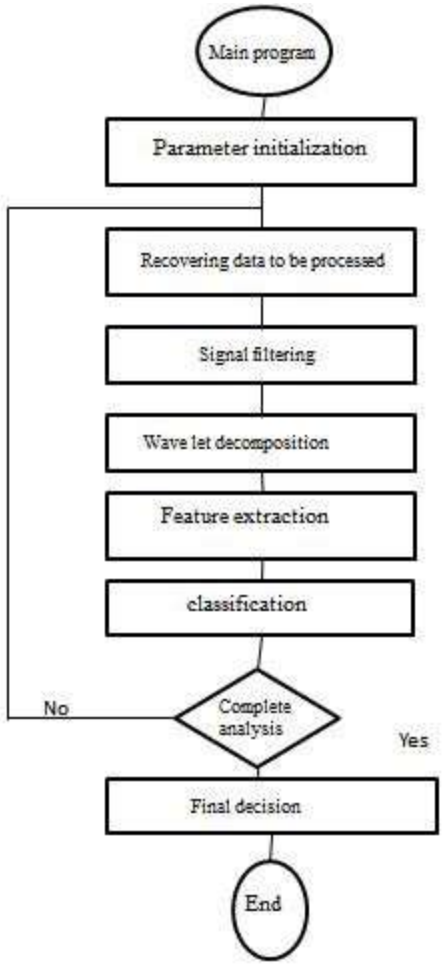

Figure 1: Flow chart of LMD method

The flow chart as shown in figure 1 begins with diagnosis data, first we need to give the information about to diagnosis. Based on the parameter values, given data will compared with data sheet which are saved primarily. After comparison the entire data is going to filter under wavelet decomposition. After decomposition, it will extract features of the result data. After extraction then it is classified .If the classification is done according to the analysis then it will be the final decision, or else it will compare with loaded EEG signal information once again.

2. GA-SVM: It abbreviates genetic algorithm optimized support vector machine (GA-SVM). It is a technique used to reduce the EEG signal information by using a standard data sheet.

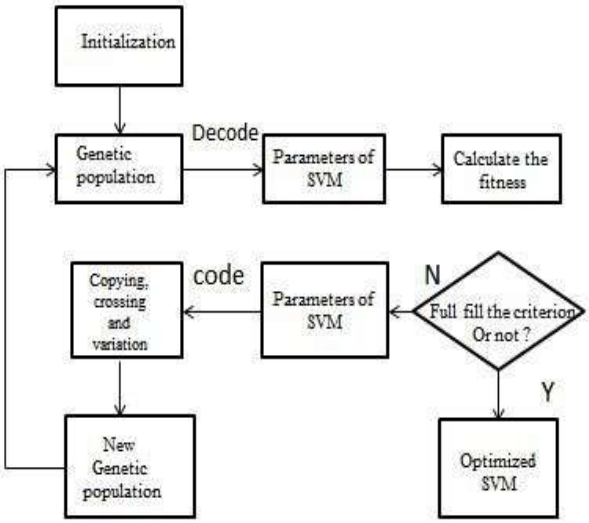

Figure 2: Principle Diagram of GA-SVM

The diagram shown in figure 2 depicts the operation of GA-SVM. First, it is initialized with data and then it is processed with genetic population to load data for further processes. After the process, it gets converted to code. By using decoding techniques, after decoding the result is compared with SVM data, which is already saved with software. After comparing, it calculates parameter values. If it is accurate then process is going to end. If it is not accurate, then it will once again under go process and validates the data with the given information and with the new data generation.

Table 1: Comparison table

S.NO	Used resource	LMD (In %)	GA-SVM Method (In %)
1.	LUT as a logic	0.15	0.18
2.	LUT as Memory	0.1	0.2
3.	Core of the ARM Processor	50	40

Table 1 shows the comparison table of LMD with GA-SVM method; we can say that GA-SVM based method is best in all cases.

IV . CONCLUSION AND FUTURE SCOPE

In this proposed model mainly new seizure identification model using LMD. Because EEs are changes with any other parameters and not in constant signals, SVM model is

introduced to decay the main EEG signals in to a series of PFs. In this paper LMD extracts almost nine parameters from first five PFs. Practical results shows that the decayed PFs are mainly useful in identifying many types of EEG information. The proposed method GA-SVM is highly stable and manages all common medical information.

The proposed method may use for identifying other Ailments and arranged in automated seizure identification simulation based on the proposed algorithm.

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Design and Simulation of a Multiband Slot Antenna for GPS/WLAN/WiMAX Systems Using CST

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Design and Simulation of a Multiband Slot Antenna for GPS/WLAN/WiMAX Systems Using CST

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Abstract. Design of a four band i.e. multiband slot antenna incorporating Global Positioning System, Wireless Local Area Networks (for IEEE 802.11 b&g and IEEE 802.11a) and Worldwide Interoperability for Microwave Access is presented in this paper. The antenna is designed for frequency of 1.57GHz for GPS, 2.5GHz for IEEE 802.11 b&g WLAN, 3.5GHz for WiMAX and 5.3GHz for IEEE 802.11a WLAN system. The antenna configuration comprises of a rectangular slot with triangular cuts at the corners to achieve impedance matching. It is designed and simulated using CST Studio Suite. The simulated antenna is fabricated on the economical substrate i.e FR-4 using standard photolithography process and tested in vector network analyzer (Anritsu- MS2027C). The designed antenna shows exceptional results in terms of return loss, voltage standing wave ration (VSWR),radiation pattern and bandwidth. Results conclude that the designed antenna is well suited for various applications as mentioned.

1. INTRODUCTION

In the domain of wireless communication, antennas play a requisite role in transmission and reception of EM (Electromagnetic) signals, and there are different types of antennas with different properties. With a lot of improvements in different wireless communication standards, it is required to integrate various wireless communication systems such as GPS, WiMAX and WLAN standards into one wireless device. Because of this, various antennas have been studied, e.g., the multiband patch antenna having different polarization states in [1], the dual-band monopole antenna for the WiMAX systems in [2] and the dual-band loop antenna for the 2.45/5.2/5.8 GHz bands in [3]. Slot antennas of compact size, wider bandwidth, and simple integration with other devices are better equipment for the design of multiband antennas. Different designs of multiband antennas have been proposed in the previous years, [4-22].

This paper presents the design of a multiband slot antenna for GPS/WiMAX/WLAN [7, 9, and 16] systems. The designed multiband antenna is simulated using the Computer Simulation Technology (CST) microwave studio. For verification of the simulation results, the antenna is fabricated using photolithography process and tested using Vector Network Analyzer (VNA).The

obtained results like reflection coefficient or S11 curve, radiation pattern, VSWR and bandwidth are presented in the paper.

2. ANTENNA DESIGN

The designed slot antennas with four bands is illustrated in Figure.1, which consists of a rectangular slot dimensions L1 × W1 = 48 × 18 mm2 with triangular cuts on four corners of the slot to achieve better impedance matching. The rectangular slot with triangular cuts is included with a M-shaped stub and two C-shaped stubs on the right and left sides of the slot. A T-shaped microstrip feed patch is used to feed the rectangular slot . A feed line of width Wf = 1.76mm is used to achieve an impedance of 50Ω. The antenna is designed using FR-4 substrate with a relative permittivity of ∈ _r = 4.4, a thickness of about 0.8mm and a loss tangent of 0.025.This material is known to retain its high mechanical and electrical strength and also available at low cost. The antenna is fabricated using photolithography process and tested using vector network analyzer.

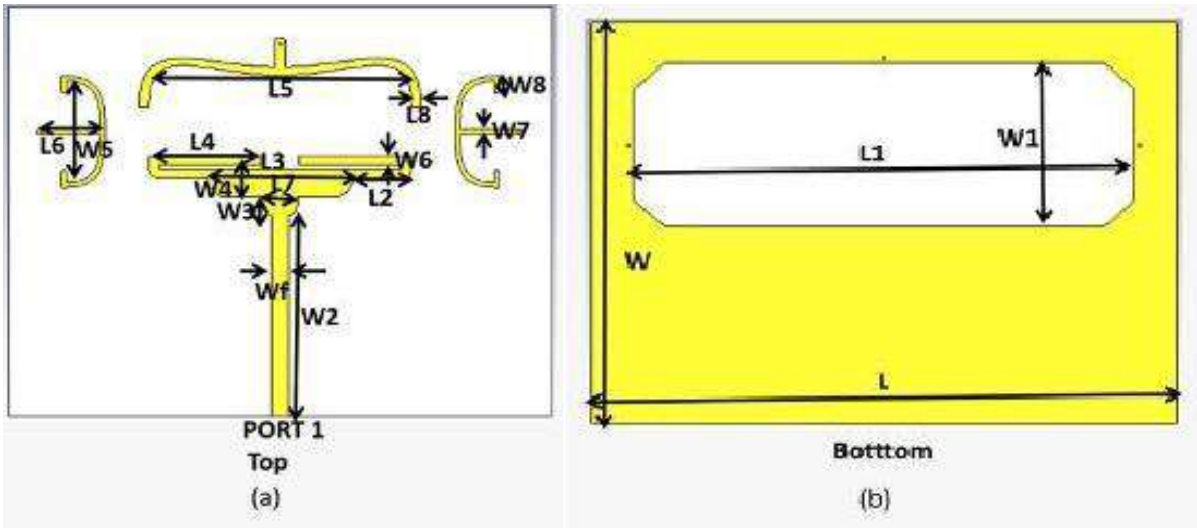

Fig.1. Designed Antenna (a) top view; (b) bottom view

The rectangular slot with chamfered edges with W-shaped stub with bending generates band 1 at about 1.57GHz. The two C-shaped stubs generate band 2 at about 2.5GHz for IEEE 802.11 b&g standard. Due to the coupling of the T-shaped feed patch and W-shaped stub generates band 3 at about 3.5GHz for WiMAX applications. The T-shaped feed patch in the higher mode generates band 4 at 5.3GHz for IEEE standard 802.11a WLAN. The concluding dimensions of the designed multiband antenna are illustrated in Table 1.

Table 1: Dimensions of the antenna (in mm)

L	**L_1**	**L_2**	**L_3**	**L_4**	**L_5**
56	48	6	15	12.5	29
L_6	**L_7**	**L_8**	**W**	**W_1**	**W2**
5.5	3.6	1	44	18	21.6
W_3	**W_4**	**W_5**	**W6**	**W_7**	**W_8**
2	2	12	1	0.5	1.3
h	**W_f**				
0.8	1.76				

3. RESULTS

The designed antenna with a rectangular slot of dimensions 48 × 18 mm2 is shown in the Fig1. The antenna is designed and simulated in CST studio suite and the antenna should maintain the input-output relationship between ports which is described by return loss curve or S11 curve. S11 represents how much power is reflected from the antenna. For a better antenna performance, S11 should always be less than -10dB. Fig.2 depicts the S11 curve for the four bands.

Voltage standing wave ratio (VSWR) is a quantity that tells how best the impedance of antenna is matched. Smaller the VSWR, better the impedance matched. For better performance, VSWR reading should be near to 1. Fig.3 depicts the VSWR curve for the four bands of the antenna.

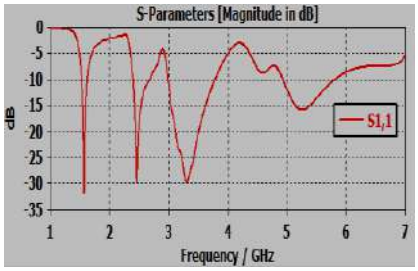

Fig.2. Return loss curve for four bands

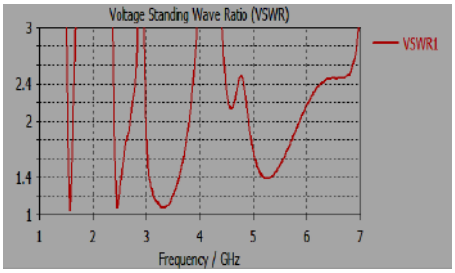

Fig.3. VSWR plot for four bands

The designed antenna shows an uniform radiation pattern which is one of the advantageous properties of the antenna.

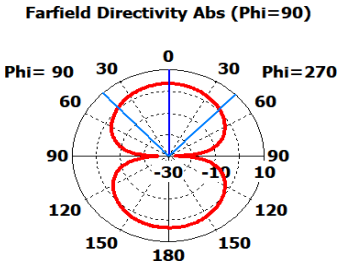

Fig.4. 2D Radiation Pattern (RP) for WLAN GPS band at 1.57GHz

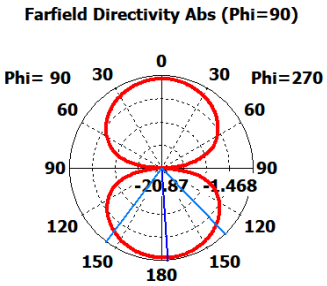

Fig.5. 2D Radiation Pattern for (IEEE 802.11 b&g) at 2.5GHz

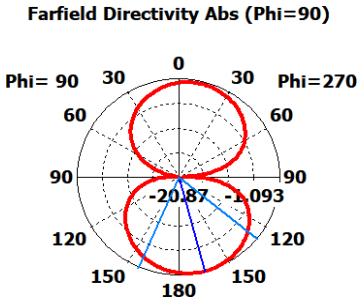

Fig.6. 2D Radiation Pattern for WLAN WiMAX at 3.5GHz 5.3GHz

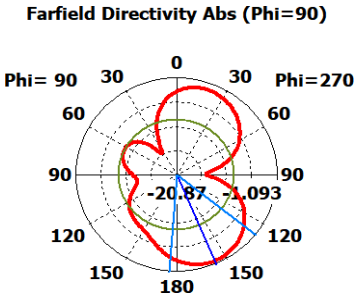

Fig.7. 2D Radiation Pattern for (IEEE 802.11a) at

Figures 4,5,6 and 7 represents the 2D radiation patterns of GPS, WLAN IEEE 802.11 b&g, WiMAX, and WLAN IEEE 802.11a respectively. It is observed that the radiation patterns are in the form of 8, which represents better radiation pattern.

The antenna is fabricated using photolithographic process.Fig.8 represents the fabricated antenna. After the fabrication antenna is tested using vector analyzer. Fig.9 represents the testing of the antenna in vector network analyzer

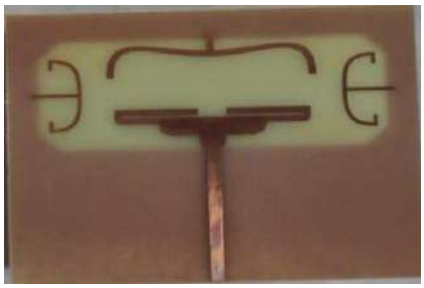

Fig.8. Fabricated antenna

Fig.9. Testing in VNA

Fig.10 and Fig.11 represents the S11 and VSWR curves respectively of the fabricated antenna in vector network analyzer.

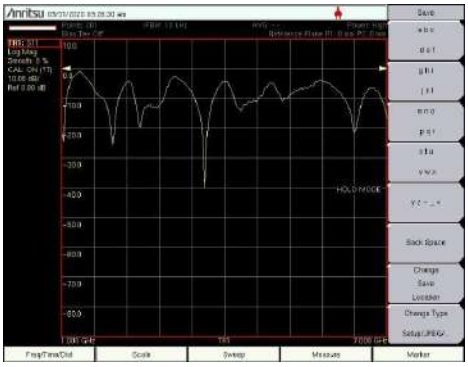

Fig.10. S_{11} curve in VNA

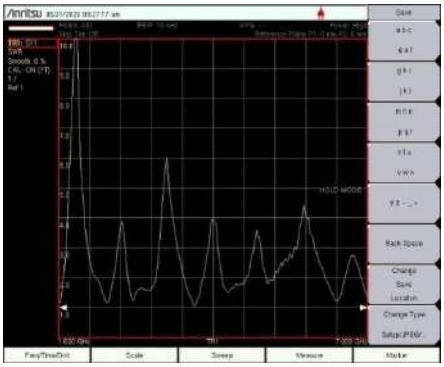

Fig.11. VSWR curve in VNA

Simulated vs Measured results of the antenna i.e. S11 and VSWR are shown in Fig.12 and Fig.13.

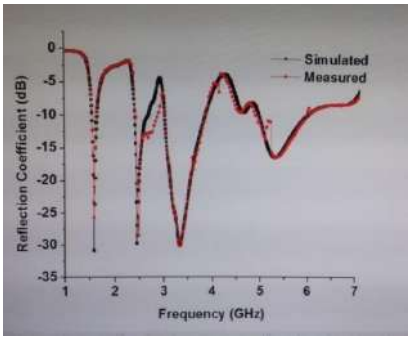

Fig.12. Simulated vs Measured S_{11}

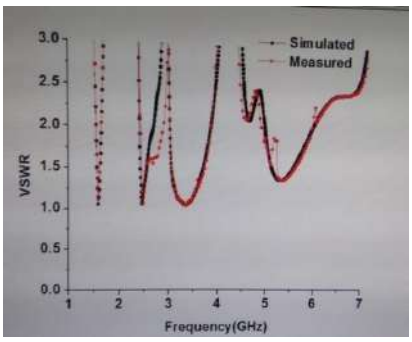

Fig.13. Simulated vs Measured VSWR

Tables 2,3,4 and 5 describes the Simulated vs Measured results for GPS, WLAN at 2.5GHz,WiMAX and WLAN at 5.3GHz.There is an improvement in the measured return loss S11 at 1.57GHz,3.5GHz,5.3GHz as compared to Simulated Return loss S11.

Table 2: Simulated vs measured results for GPS at1.57GHz

Parameter	Simulated	Measured
VSWR	1.0611	1.069
S-parameter	-31.591	-29.65

Table 3: Simulated vs measured results for WLAN IEEE 802.11 b&g at 2.5GHz

Parameter	Simulated	Measured
VSWR	1.097	1.093
S-parameter	-29.382	-20.00

Table 4: Simulated vs measured results for WiMAX at 3.5GHz

Parameter	Simulated	Measured
VSWR	1.0682	1.0633
S-parameter	-29.455	-39.95

Table 5: Simulated vs Measured results for IEEE 802.11a WLAN at 5.3GHz

Parameter	Simulated	Measured
VSWR	1.3849	1.3722
S-parameter	-15.865	-21.22

4. CONCLUSION

In this paper, a multiband slot antenna for GPS at 1.57GHz, IEEE 802.11 b & g WLAN at 2.5GHz, WiMAX at 3.5GHz and IEEE 802.11a WLAN at 5.3GHz is designed and simulated using CST microwave studio software and achieved very low return loss and excellent voltage standing wave ratio. The antenna has been observed to provide better impedance matching, exceptional VSWR readings, S11 parameters and uniform radiation pattern. Hence, as per the characteristics observed above, the antenna can be used for many applications such as GPS/ WiMAX and WLAN systems as it resonates at multiple bands of frequencies.

5. FUTURE SCOPE

The antenna can also be extended to resonate at some more frequencies for various applications. With the increase in the number of frequencies, impedance gets mismatched, to reduce the impedance mismatch various feeding techniques can be adopted.

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Design and Simulation of a Compact 5.4GHz H-shaped Slot Antenna for RF Energy Harvesting Systems

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Design and Simulation of a Compact 5.4GHz H-shaped Slot Antenna for RF Energy Harvesting Systems

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Abstract. in this paper, a compact H-shaped slot antenna is proposed. The antenna contains one H-shape slot which is fed through microstrip line, an open circuited stub is connected for proper impedance matching. The H- shaped slot is used for bandwidth enhancement. The antenna is designed to radiate at 5.4 GHz with a bandwidth of 1.6GHz. The antenna has an omni-directional pattern across the frequency band. The gain of the antenna is 4.35dBi at 5.4GHz. Since, the proposed antenna satisfies all the characteristics of energy harvesting systems, it can be used for energy harvesting systems, at 5.4GHz 4G-LTE band. CST microwave studio was used for designing the proposed antenna. An excellent agreement is achieved between simulated and measured results..

1. INTRODUCTION

In recent years the Radio Frequency energy harvesting has been attracting an increasing deal of attention in order to provide power to the electronic devices, including Wireless Sensor Networks. This paper focuses on ambient RF energy available in the ambient environment. One of the best methods for harvesting the Radio Frequency (RF) energy is to use a rectenna. A rectenna is also called as rectifying antenna which consists of receiving antenna, filters and rectifiers. The receiving antenna is presented in this paper.

For energy harvesting systems the antenna should have high gain, high directivity, omnidirectional radiation pattern, large bandwidth and high efficiency. To meet the requirements, various methods have been proposed. Several investigations concentrate on the receiving antenna where it collects input power as much as possible. If the input power received by antenna is maximum then the energy harvested will be also maximum. Several researchers have been using multiband antenna for harvesting from different frequency bands [1, 12, 14], antennas with high gain can also be used for RF energy harvesting [2, 9], combination of Electro Magnetic wave and solar cell is used for energy harvesting [3, 7, 8], and rectenna arrays [4, 6, 9]. In the paper [5, 13], semicircular slot antenna for rectenna was presented. A compact 5.4 GHz antenna for energy harvesting is proposed in this paper. This compact feature can be used in rectenna array design to combine higher microwave power at 4G-LTE band.

2. H-SHAPE SLOT ANTENNA DESIGN ANTENNA DESIGN

Traditional microstrip-fed rectangular slot antenna with a magnetic wall at the slot centre is depicted in Fig.1 (a). The proposed antenna design has an H-shape slot fed by a microstrip feed line and open-circuited stub to adjust impedance matching is depicted in Fig.1(c). The antenna is designed in CST microwave studio. In designing the antenna FR-4 substrate with a dielectric constant (εr) of 4.4 with thickness of 0.8 mm is used. The antenna is compact for using H-shape slot. The H-shape slot increases the bandwidth (BW) of the antenna. The resonance frequency of the slot is calculated from equation (1), where 'c' is the speed of the light and 'εeff' is the effective dielectric constant. The dimension of the designed antenna is 92 x 73.5 mm2. Fig.1(c) and Fig.1 (b) shows the layout and fabricated prototype of the designed antenna respectively; all the structural parameters of the antenna are embellished in Fig.1.

$$= c/(slot\ length * \sqrt{\varepsilon_{eff}}) \qquad (1)$$

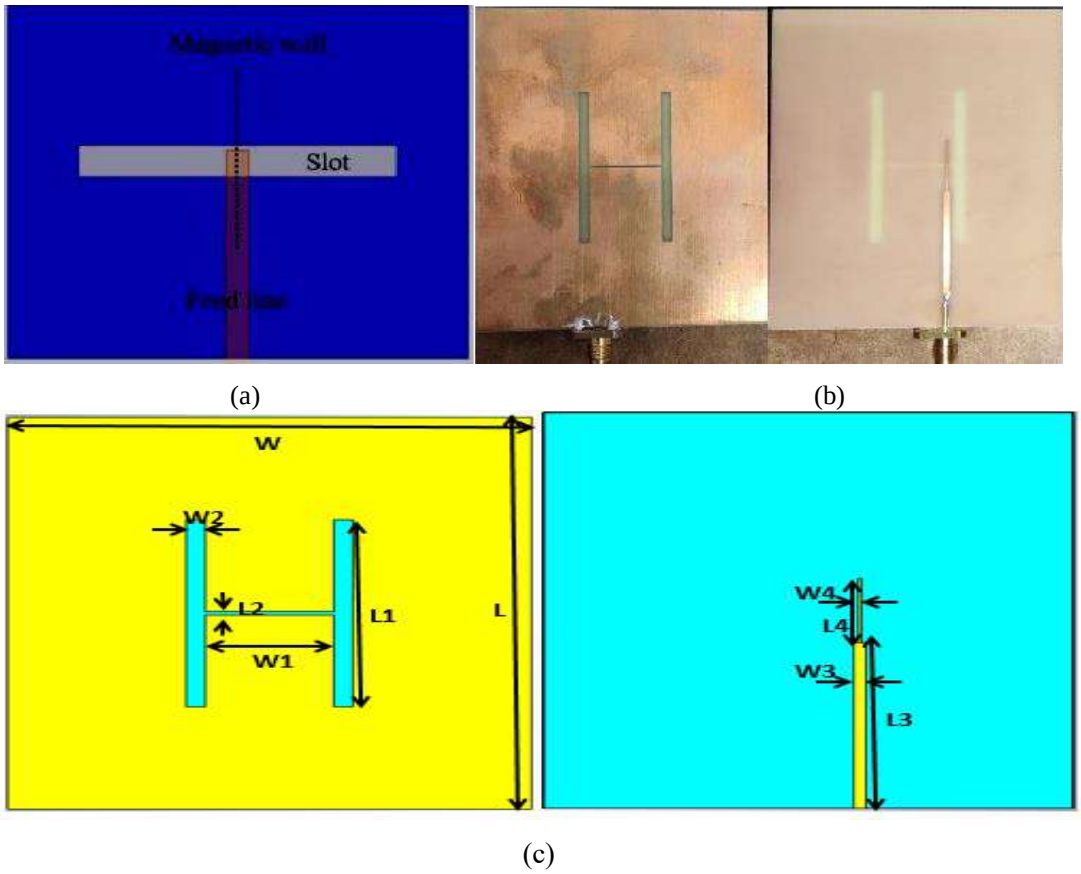

Fig.1. Proposed antenna layout (a) slot antenna, (b) photo of the fabricated prototype, and (c) H-shape slot geometry L=92mm, L1=44 mm, L_2=0.74 mm, L_3=38.5 mm, L4=14.9 mm, W=73.5 mm, W1=18 mm,W2=2.75 mm, W_3=1.53 mm, W_4=0.55 mm.

3. ANTENNA RESULTS

The designed antenna is fabricated using photolithography process and tested using Vector Network Analyzer. The antenna is designed using the FR-4 substrate which is of very low cost K connector is used in the measurements which affects the measured results slightly. The measurement setup is shown in Fig.2

Fig.2.Measurement setup

A. *S-Parameters of Antenna*

Fig.3 shows the S-parameter plot indicating the reflections from the antenna. It can be observed that the antenna radiates between 4.8GHz to 6.48GHz. Therefore bandwidth of the antenna is 1.7GHz. Fig.4 shows the excellent concurrence between the simulated and measured S-parameters for the H-shaped slot antenna.

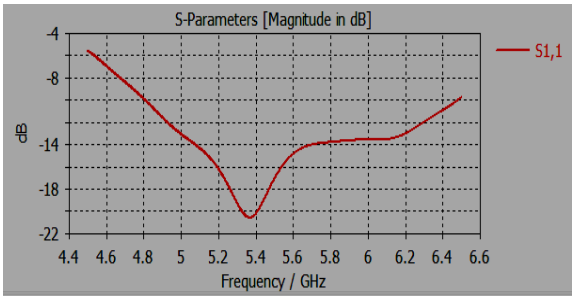

Fig.3.S-Parameter plot

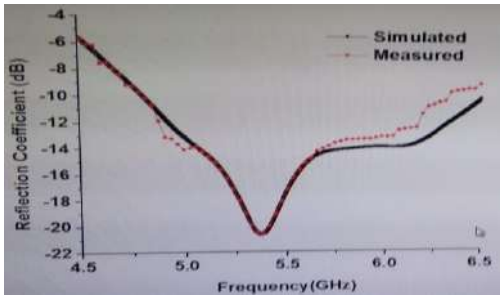

Fig.4.Simulated vs measured S-parameters of the antenna

As seen from the figure, it can be noticed that the antenna has a bandwidth for reflection coefficient ≤ -10 dB from 4.8GHz to 6.4GHz. Therefore, the bandwidth of antenna is 1.6GHz.

B. *Voltage Standing Wave Ratio (VSWR)*

Fig.5 shows the Voltage Standing Wave Ratio (VSWR) plot of the simulated antenna. It can be noticed that the VSWR obtained at 5.4GHz frequency is nearly 1.21which indicates that

the antenna has very less reflections. Fig. 6 shows excellent agreement between simulated and measure VSWR for the H-shaped slot antenna. The antenna has VSWR ≤ 2 from 4.8GHz to 6.4GHz. The antenna efficiency is more than 90% for the entire bandwidth.

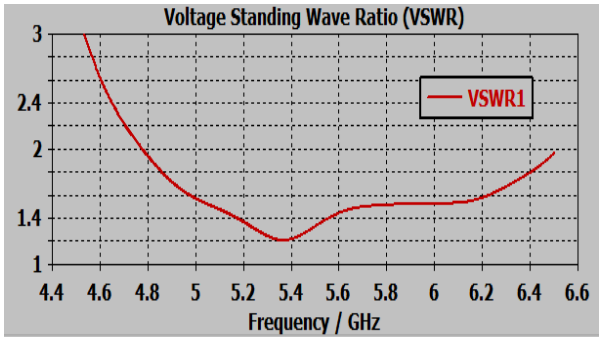

Fig.5.VSWR plot

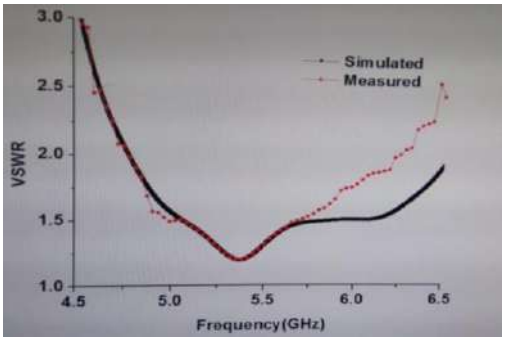

Fig.6. Simulated vs Measured VSWR results

C. Gain

Fig.7 shows the polar pattern of the gain. It is observed that at 5.4GHz frequency4.34dBi gain is obtained.

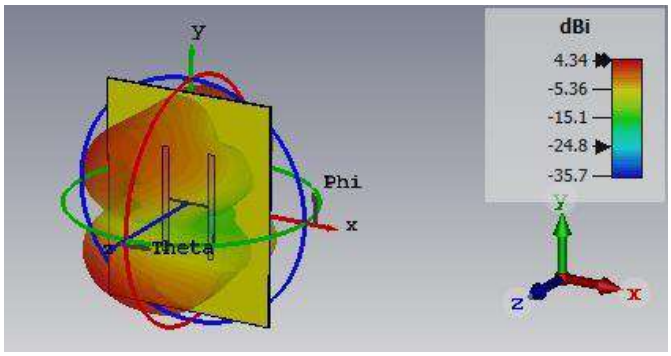

Fig.7.3D Polar Plot of Gain

D. Radiation Pattern

E-plane and H-plane radiation pattern is shown in the Fig. 8. It is observed that the antenna radiates with a gain of 4.35dBi at 5.4GHz. The designed antenna has a relatively stable Radiation Patterns (RP) and around 90% radiation efficiency over the entire frequency range.

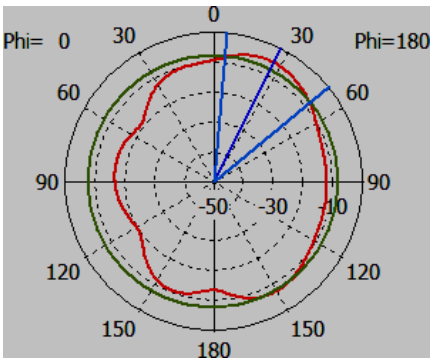

Fig.8.E-plane (Red line) and H-plane (Green line) radiation patterns at 5.4GHz

E. Surface Current Distribution

The surface current distribution (SCD) is shown in the Fig. 9.The red portion indicates the maximum current distribution over the radiating patch.

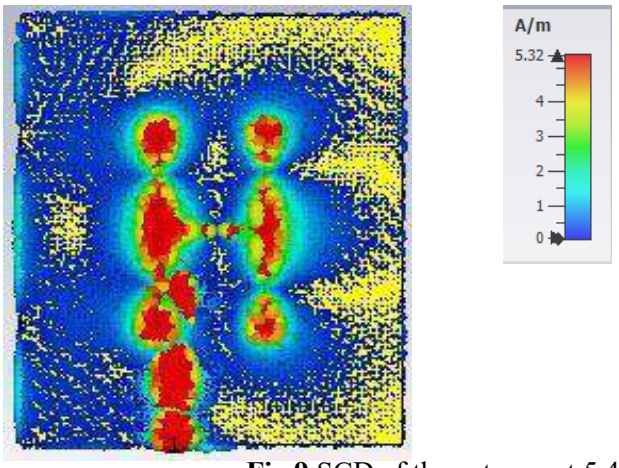

Fig.9.SCD of the antenna at 5.4GHz

F. Directivity

The Directivity of the designed antenna shown in the Fig.10 The obtained directivity is 6.1dBi.

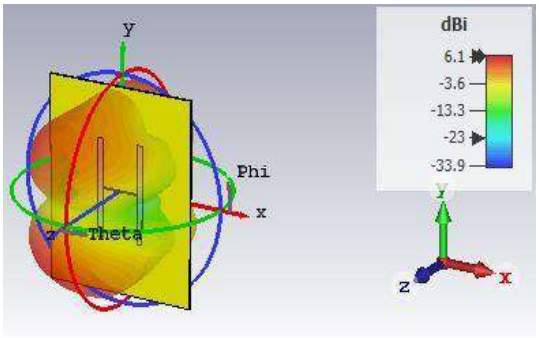

Fig.10.Directivity of designed antenna

G. Efficiency

Fig.11 and Fig.12 depicts the radiation efficiency and total efficiency of the designed antenna respectively. With the designed antenna 90% efficiency is obtained.

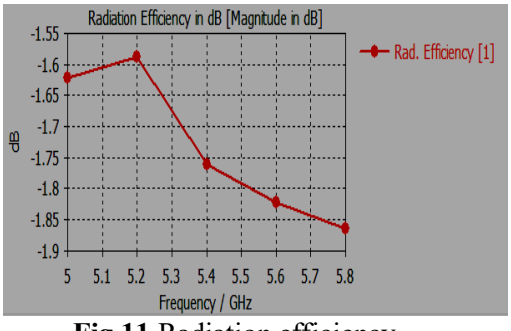

Fig.11.Radiation efficiency.

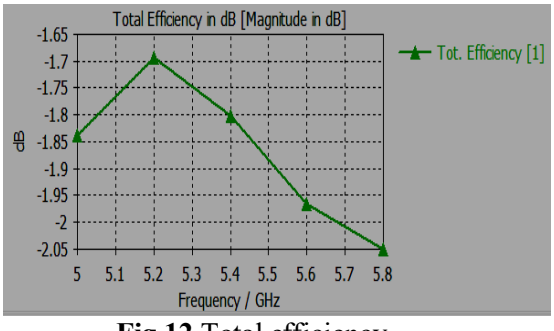

Fig.12.Total efficiency

4. CONCLUSION

This paper presents an H-shaped microstrip slot antenna which resonates at 5.4GHz frequency. The antenna was designed and simulated using CST microwave studio software. The designed antenna has achieved very low return loss and excellent voltage standing wave ratio. The techniques employed for investigating the antenna characteristics shows high efficiency and high accuracy. The fabricated antenna has a bandwidth of 1.6GHz and a gain of 4.35dBi at resonant frequency of 5.4GHz with an Omni directional radiation pattern. Since, the fabricated antenna meets the requirements of energy harvesting systems; it can be used in energy combining techniques.

5. FUTURE SCOPE

The bandwidth of the antenna can be further increased by including multiple slots, but increasing the number of slots increases the complexity in design. Further the directivity of the system can be increased by incorporating array of antennas and also gain can be improved by coupling the slot with another slot antenna.

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Hardware realization of Bathymetry rover using Embedded C

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Abstract: Bathymetry is a process of finding water bodies depth; it is widely employed method in most of the unexplored areas of oceans and lakes. Estimating Depth using bathymetry with incorporation of velocity of sound in underground water, which depends on pressure, temperature and salinity of water body. Need for the Rover is properly justified, because of the prevailing climatologically condition on high altitudes of Himalayas. On such altitudes with temperature of glacial lakes are mostly below zero degree Celsius, hence performing bathymetry by human inspection on floating boats are very hazardous to human life.

This main purpose of this paper is to Measure water depths in lakes by means of sonar or digital transducer for calculation of depths in lakes. We use GPS (global positioning system) for tracking out the location. Arduino is used for controlling system which acts as a micro controller for working of motor, measuring the depth, identifying the location and transmission purpose. At last we use latitude and longitude to point out way in maps. State-of-the-art robotic embedded sonar vehicles are too expensive and heavy. Robotic system provides less-cost, high-accuracy bathymetric surveys of lakes, rivers and oceans is proposed. It is able to identify the exact position of rover during transmission and reception of sonar pulse. It has ability to derive the bathymetry of glacial lakes thereby controlling from the longer distance.

Keywords: Arduino; Bathymetry; GPS; Transducer.

I.INTRODUCTION

The Bathymetry rover can monitor the location of the rover and also helping to monitor the rove and displaying the depth of the lakes, river and sea. It gives mint to mint updates related to rover location in the Google maps. Arduino Uno is the major device in this system and Sever helps to store the data and display output. Bathymetry data gives information related to Shape of underwater terrain and depths, has a range of use. Nautical charts [1] formed based on the information received from Bathymetry and it is useful for mariners like a road map guide to motorists to safe and effective maritime transportations. Climate change in the environment can be learning from the bathymetry charts. These charts can alert ongoing and sea level rises, potential beach erosion and land sinking. Hydrodynamic models are created by using bathymetric data. The key element for biological oceanography [2] is bathymetry. Researchers use high resolution bathymetry to find fish and other sea food.

In this paper we constructed and designed a model which will provide vehicle location and security information to user by displaying on location in the web page by using Google Maps.

In this paper we discussed interfacing of GPS and Arduino, finding the latitude and longitude of rover location and sent to Arduino. We discussed how Sensor helps to give the river depth. It sends the latitude and longitude data and sensors data in the form bit streams via GPRS. This data is read by the server and published in Google map for this total process program is implemented in Arduino and server part in PHP language.

II. LITERATURE

The 7th International Geographic Congress presented a commission on the sub-oceanic nomenclature in Berlin 1989. It is only responsible to publish the conventional bathymetric chart. Another commission convened in Wiesbaden (April 15-16, 1903), with prince Albert-1 of Monaco is the chair person and also adopted the characteristic determined in a memorandum by J. Thoulet. The second version published between 1912 -1931 surrounded by the contour line which is representing altering of nomenclature and terrestrial relief. The utilization of sonic and ultrasonic devices are enhanced the amount heavily. The bathometry charts were initiated in 1903 by an international group geographers and oceanographers, under leadership of Prince Albert-1 of Monaco. During this time there is huge interest in the study of real time nature thereby identifying the set of group. The set of maps describes importance of the structure of ocean floor. GEBCO is maintaining in digital form as GEBCO Digital Atlas. European Marine Observation and Data Network (EMODnet) is an intelligent project which is

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funded by European govt., to bring both marine and data into interoperable, continuous and freely accessible data sets for the entire maritime basins in European waters. As part of this the EMODnet Bathymetry portal presents the bathymetry data set in the form of Digital Terrain Models (DTM) for specified basins of the maritime. The DTMs produces central DTM which is integrated and collated bathymetric data sets. If high resolution DTMs not available at that time Bathymetry information is collected from GEBCO-30 arc Second grid. In association with the GEBCOs global Bathymetric and EMODnet Hydrographic team is including bathymetry data-set from the DTMs given to EMODnet Bathymetry portal. The Baltic Sea Bathymetry Data base (BSBD) is effective the solution of an effort to create and generate a bathymetric grid for the Baltic Sea region which is using data from Baltic sea countries hydrographic offices under Baltic sea hydro graphic commission. Southwest Indian Ocean bathymetric compilation is also data set that it cover the area 4°S-40°S; 20°E-45°E. The major objective of this multinational project is to collate, assemble, publish and archive entire environment available bathymetric data set from all sources through the Indian Ocean and construct a new bathymetric map and grid of Indian Ocean using data-set from the entire open sources.

If we look around we will find ourselves to surround by computing system. Nowadays embedded systems can find all the fields like mobile phones, digital cameras, portable video games, camcorders, smart watches, calculators, washing machines, fax machines, transmission control unit, anti lock brakes, automobile industries, automated teller machines, cash registers, alarm systems, and many more. Embedded systems are used in all fields making the life easy, simpler and secure.

III. PROPOSED SYSTEM

Bathymetry is the study of under water depth of river, lake or Ocean. It can track the location of the rover and also helps in monitoring the rover and displaying the depth of water. The proposed model block diagram is as shown in below figure 1

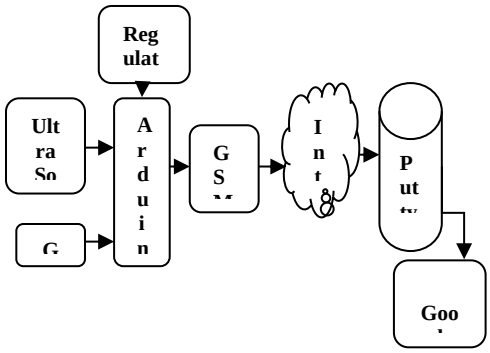

Fig 1 proposed block diagram

Ultra Sonic Sensor [3] is generates short bursts of voice and listens for this sound to echo off of objects. The frequency of the voice is very high for human being to hear (ultrasonic 40 kHz). It provides accurate, non contact distance from .02 meters -3 meters and it is easy to interface controller. Sensors will work by sending ultrasonic rupture and giving output data it corresponds to the time required for the rupture echo signal to sensor by calculating the echo signal width we can easily identify the target distance. The ping))) sensor can't measure the exact distance if the object is more than the sensor range 3 meters, if the reflected angle is $\theta<45^{\circ}$ and if the object is very small then it is difficult to get the accurate distance of the object. Along this a soft skin animals or if the objects have irregular or stuffed surface are not reflect the proper echo signals so that it is difficult to get the accurate distance. Ping))) sensors are temperature sensitivity if the temperature range is 0 to 70°C is significant in the magnitude of 11-12 percent.

C_{AIR}= 331.5 + (T_C x 0.6) m/s [4]

Global Position System (GPS) is provides time and location information in all environmental conditions, in or one the earth. The GPS System provides critical positioning capability to Civil, military and commercial user around the earth. The U S Department of Defence (D o D) is developed GPS system in 1995. The GPS module REB-1315S4 is connected to the Arduino it continuously gives information related to the longitude, altitude, latitude and relative speed also. The frequency range of the REB-1315S4 is L1 band 1575.42 MHz, it provides C.A Code and it can operate on different temperature conditions in the range between -35 to +85℃ the default bud rate of the REB-1315S4 is 9600 bits per second. In order to operate REB-1315S4 we need 3.3V DC power supply we need the power supply must be added by bypass capacitor 10µf and 1µf it is used to reduce the Noise from power supply and will increases the Power stability.

Global System for Mobile Communication (GSM) [5] is a group of ETSI standards indicating that infrastructure related to digital Cellular system. More than 85 countries are following the ETSI standards. The GSM [6] will send and receive text messages and we can also do the same for voice calls we are using SIM card. SIM800 is a wireless module and Ultra compact. It is complete dual band GSM/GPRS [7] solution SMT. SIM800A provides GSM (800MHz)/ GPRS (1800MHz) for messages, data, fax and voice with low power consumption and form factor. With small size 2.4cm X 2.4 cm X 3cm and weight of 3.4gm. It

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is controlled by using AT commands and the temperature sustainability range is -40 - 85℃. The GSM need power between 700-1000mA it is getting from external power supply. To make a call we are using AT command like ATD + mobile number with country code then press Enter similarly to disconnect the call use command ATH and Enter. Select COM port to burn the program from Laptop into Arduino board. Next power supply provided to the GSM modem for programming we use only T_X and R_X these pins are pin1 and pin2 in Arduino Uno then we have to burn the program in Board. The GSM T_X and R_X pins are connected to Arduino Uno R_X and T_X pins.

The Arduino Uno [8] is a controller based board the ATmega328. It has 16 digital input/output pins (in which 6 are used as PWM outputs), six are analog inputs, one USB connector, a power jack, ICSP header, a 16 MHz Ceramic resonator and r eset

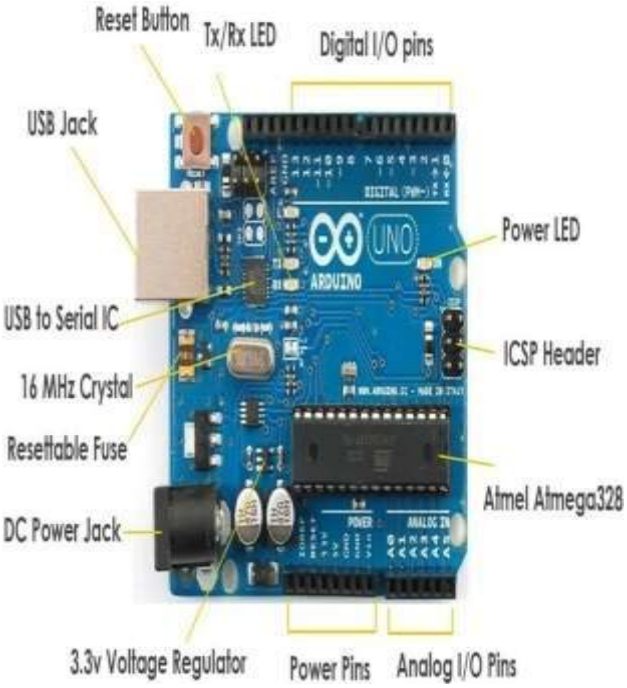

Fig 2 Arduino Uno

button. Compare to other preceding boards it won't have FTDI USB-serial driver chip. In built it is programmed as USB-Serial converter. It is having powerful reset circuit. Power supply to the board is given by using USB port. The power supply may receive from Battery or AC-DC adapter [9]. By default board will select power source. It can operate external power supply up to 6-20 Volts. The memory storage of ATmega328 has 32KB in this 0.5KB for boot loader. Along this it have 1KB of E^2PROM and 2KB OF SRAM. It is also compatible for UART Transistor – Transistor logic serial communication. It supports SPI and I^2C Communication. The Arduino Integrated Development Environment (IDE) have editor for writing programs, a text console, a message area and toolbar. It connects to Arduino Uno and Hardware to upload programs and communicating them. Writing a program in Arduino software is called Sketch. Sketches written in editor and saved with extension file .ino. The toolbar icons allow programmer to verify and upload program, open, create and save.

Hyper text Preprocessor is a scripting language in server side to design Web development. PHP code is embedded in to hyper text markup language (HTML/HTML5), it can be used in addition with web frame works and web content management system. PHP interpreter is used to process the PHP code. The web server combines the results of executed PHP code and interpreted data it may be in any form information with generated web page. PHP program may executed by using command line interface and it is used in standalone graphic applications. In PHP integer range will store depending on the platform either 32-bit/ 64-bit similar to C language. Similarly floating point numbers will store based on platform based. Standard problems are solved by using Standard PHP Library (SPL).

PuTTY is open source terminal emulator, serial console and is free network file transfer application. It supports different network communication protocols. Originally PuTTY application is meant for Microsoft windows but it is used in Linux and other operating systems. PuTTY was designed by British programmer Simon Tatham. PuTTY supports Single Sign on through the Generic Security Service Application program. PuTTY integrated with Command line Secure Copy Protocol and SSH File Transfer Protocol are called "PSCP" and "PSFTP". PuTTY does not allow Session Buttons directly.

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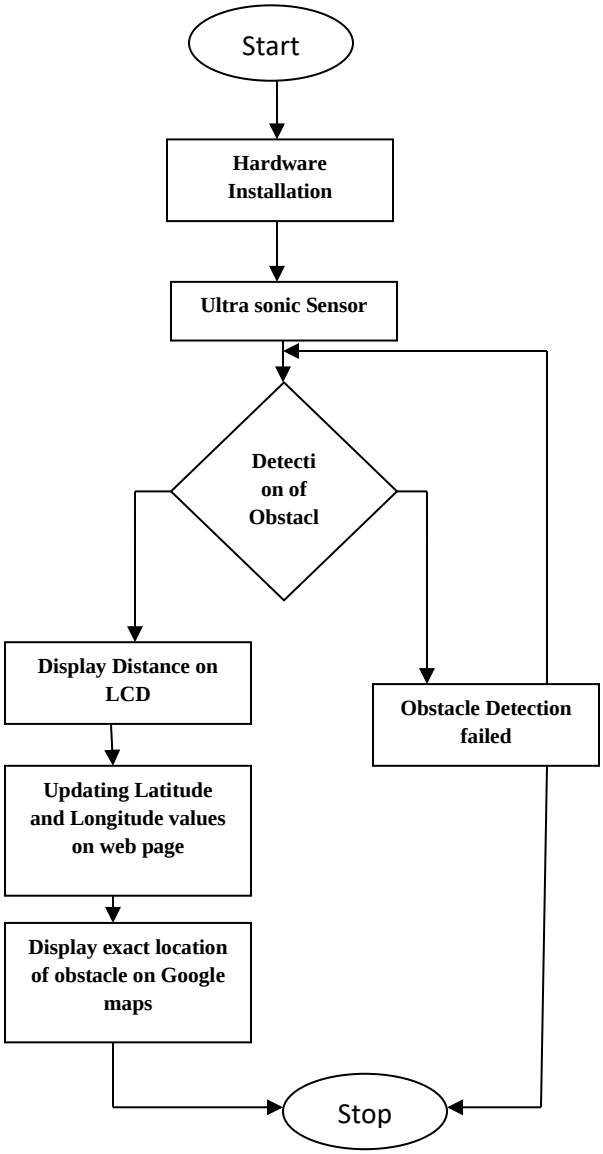
IV. PROJECT FLOW CHART



V. RESULTS

When the system is powered on the LCD will Display a welcome string "BATHYMETRY ROVER". The total kit is powered on and a sensor starts working and does respective works. Shown in figure 3.

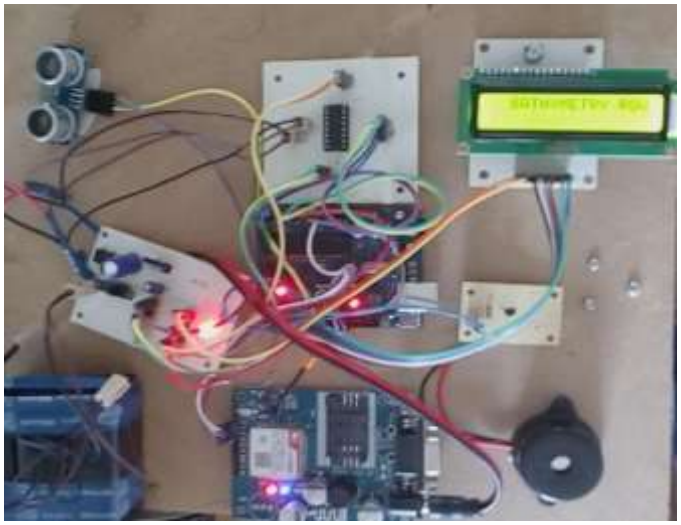


Fig 3 Bathymetry rover

HARDWARE INSTALATION

The information obtained from sensor is computed in Arduino for further processing and then the Arduino drives the DC motor according to the inputs. GPS get initialized when kit is turned on. It is shown in fig 4.

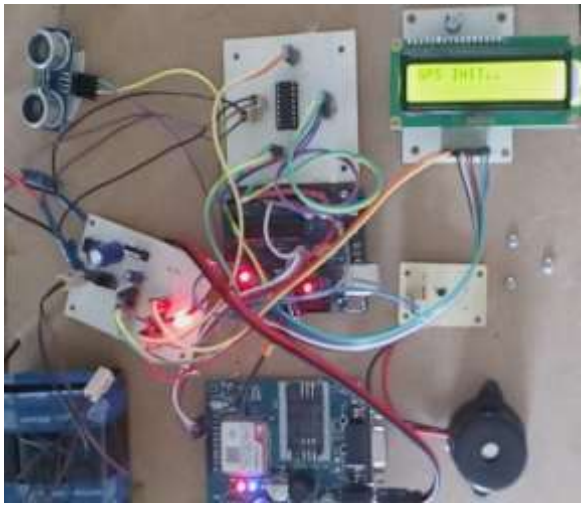


Fig 4 GPS initialization

DISPLAYING THE DISTANCE

When the sensor detects obstacles then the distance of obstacles displayed on the LCD and updates the distance in the server. It is shown in fig 5.

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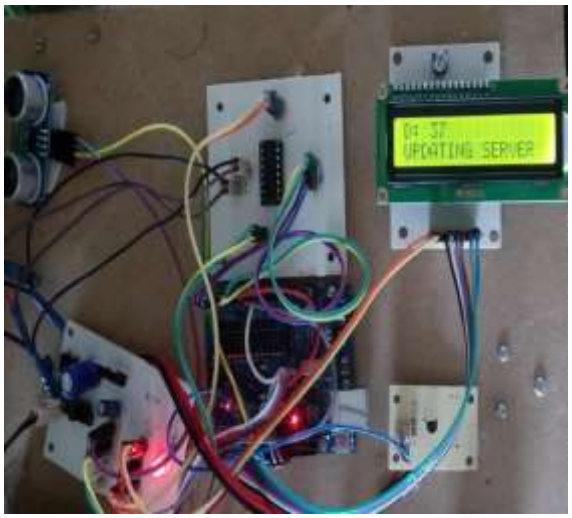

Fig 5 Displaying the Distance

UPDATING LATITUDE AND LONGITUDINAL VALUES ON WEB PAGE

Fig 6 Displaying latitude and longitude

Updating the latitude and longitudinal values which are given by GSM on web page it was created on server using PuTTY and also the pin location is displayed on Google Map and Shown in above image.

VI. CONCLUSION & FUTURE SCOPE

The proposed system is playing an important role in real time tracking and monitoring the rover and finding the water depths in lakes, sea and rivers. Knowledge of the Bathymetry has progressed quickly due to using advanced technologies like Acoustic, RADAR and optics. Maximum acoustic sounds are required to validate gravimetric Bathymetry in remote regions in the world.

FUTURE SCOPE

The Bathymetry rover system can be further improved by using multi beam sonar it is having greater resolution with greater productivity.

By the help of Airborne LIDAR Bathymetry (ALB) we can survey costal and land waters in single approach.

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IDENTIFYING FRESHNESS OF A LEAF BASED ON COLOUR USING VECTOR QUANTIZATION METHOD

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***Abstract*- Quality of a leaf is influenced by its age and maturity. Edible leaves like spinach, fenugreek, curry leaves, etc., are mostly used in Indian Dishes, consumers depend on the sensory properties like appearance, colour, texture and aroma to assess the internal quality of the internal quality of the leaf. However, with the onset of automated food chains and IOT based food recognition applications, vegetables are identified by capturing their images and processing. IOT is effectively used to reduce waste, cost management and risks. For an instance, IoT facilitates food companies to ensure superior levels of traceability, food safety and, therefore accountability all through the farm-to-plate supplies chain operations. The IoT network in the food supply chain greatly helps in reducing waste, costs, and risks as well, in all stages of the procedure. In this paper a simple method is proposed to assess the quality of leafy vegetables based on its colour using vector quantization method. Cropped images are processed and fed to the algorithm to identify the number of colours in the algorithm.**

***Keywords*: k-means, IOT, colour identification, clustering, food monitoring**

I. INTRODUCTION

IOT in agriculture and food is still in early stages of development. Utilization of IOT in food chains and for food safety is increasing gradually. Food safety for perishable goods is of more concern [1]. To ensure food safety till it reaches the customer from the yield continuous food monitoring has to be done [5]. One of the highly used ingredients in Indian dishes is green leafy vegetables. Also, scientifically it is known as Spinciaoleracea Linn. (Family-Chenopodiaceae). The Spinach used as a food and has medicinal value also. Spinach bundled up with vitamins such as vitamin A, vitamin B, vitamin C and vitamin E and minerals like magnesium, manganese, iron, calcium and Folic acid. Spinach is great source of chlorophyll, which speedup digestion [7]. They are also highly perishable and have a very less shelf time as compared to other vegetables. There are varieties of green leaves that are edible and frequently used in Indian dishes like spinach, fenugreek leaves, coriander, curry leaves etc. spinach is used extensively in northern states of our country as well as southern states. There have been various algorithms used in recognizing leaves based on texture and outline characteristics [3]. Spinach leaves are a main source of calcium and are recommended as a regular diet for people with liver ailments. Spinach unlike fenugreek has a lesser shelf life and once the leaves start to lose their freshness they gradually lose their nutrition value. Freshness of a leaf is identified primarily by its colour [4]. When the leaves are placed in the shelf after harvesting they have a life span of one day without freezing and four days with freezing. Often, the leaves are kept in the fridge in super markets or at home. Monitoring perishable goods like spinach is essential in super markets to reduce loss and wastage. IOT can utilized to continuously monitor the freshness of the leaf and replace the product [2]. In this paper a solution is proposed to continuously monitor the product using a camera that captures pictures at regular intervals and directs to the central server. At the server the algorithm processes the images and sends a notification if the leaf is losing its freshness. A leaf is said to be fresh by looking at its colour, a bright green leaf is fresh, and a darker shade of green indicates an aged

leaf. A leaf with traces of brown colour can indicate spots or disease. Leaf that is yellowish could have less nutrition content and traces of black or dark brown could mean the leaf has started to decompose.

II. METHODOLOGY

A. Data Collected

Images of spinach leaves are collected from different sources using Samsung mobile camera. These images are primarily belonging to Spinach and hence images of a spinach leaf in different conditions are collected and fed to the algorithm. Leaves tend to change colour based on the environmental conditions and also the way in which they are stored. Also the time taken to store the leaf is very vital. The following common conditions are considered:

1. When the leaf is freshly plucked by hand.

2. When the leaf is plucked and maintained in cool temperatures for a day or two to retain freshness.

3. When the leaf was plucked after it aged on the plant itself

4. When the leaf has aged and also damaged without proper storage.

Images of leaves with bright green, dark green, yellowish and yellowish leaves with spots are used. Some of the images are presented below

Fig.1 Examples of the spinach leaves used in dataset

B. Procedure

The image is captured using a pinhole camera that is fixed inside the fridge or in a place where the leaves can be viewed properly. Images are captured at regular intervals and sent to a central server. The algorithm resides at the server that processes the images. The image is first cropped and only the leaf without the background is fed to the algorithm. The algorithm extracts the colours from the leaf and displays the percentage of each colour. Based on the amount of colour the server sends a notification to the client. The colours are identified using clustering K means algorithm is used to cluster the colours.

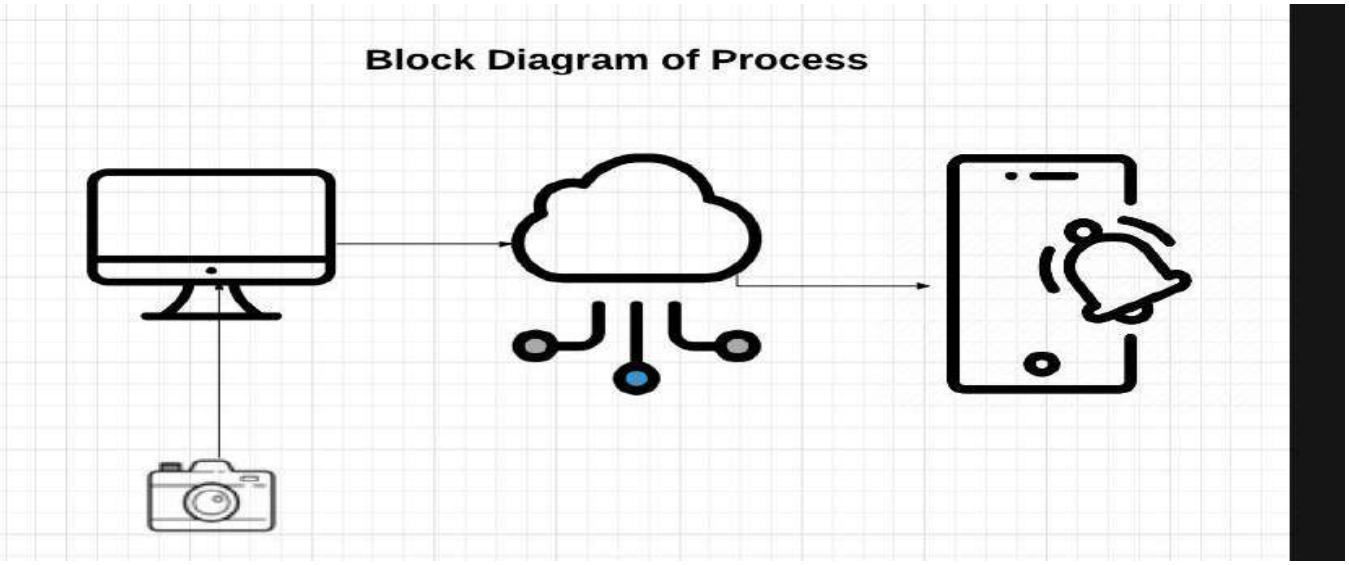


Fig. 4 A simple architecture depicting the process

The pre-processed and cropped images are fed to the algorithm that performs the following tasks:

1. Extract the RGB values of the image as hexadecimal numbers.

2. The image is then resized to a fixed height and width for uniformity.

3. The image is fed to the k-means clustering algorithm with the number of clusters as n. In our case the number of clusters depicts the number of colours. The clusters are formed using the following formula

$$J(V) = \sum_{i=1}^{c} \sum_{j=1}^{c_i} (\|x_i - v_j\|)^2$$

4. The hexadecimal values of the colours are then again converted back to RGB values and plotted on a Pie chart with the percentage of each colour.

The flow chart presented below depicts the process adopted to identify the colour of the leaf.

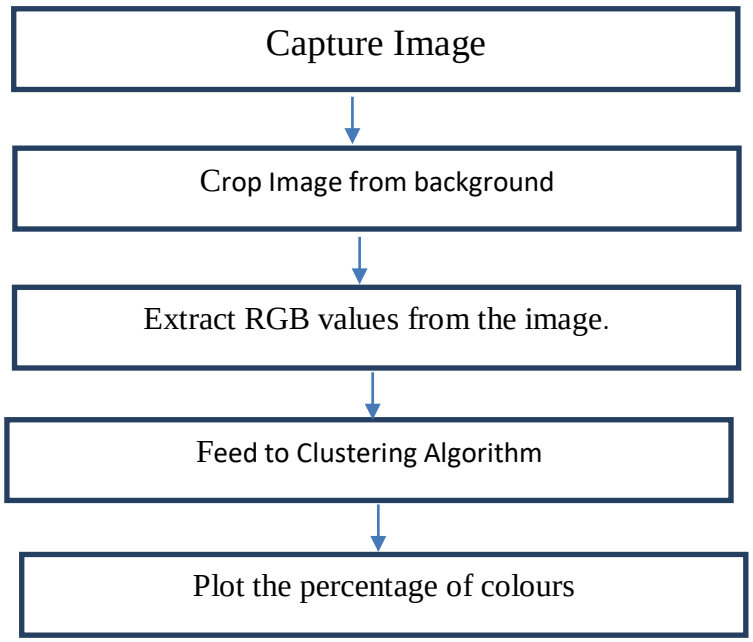


Fig. 2 Flow chart of the proposed solution

C. K means Clustering algorithm

k-means clustering is a method used for vector quantization, originating from signal processing which is popular among different cluster analysis methods in data mining[6]. k-means clustering aims to partition n observations into k clusters in which each observation belongs to the cluster with the nearest mean, serving as a prototype of the cluster. This results in a partitioning of the data space into Voronoi cells. k-Means minimizes within-cluster variances (squared Euclidean distances), but not regular Euclidean distances, which would be the more difficult Weber problem: the mean optimizes squared errors, whereas only the geometric median minimizes Euclidean distances. Better Euclidean solutions can for example be found using k-medians and k-medoids.

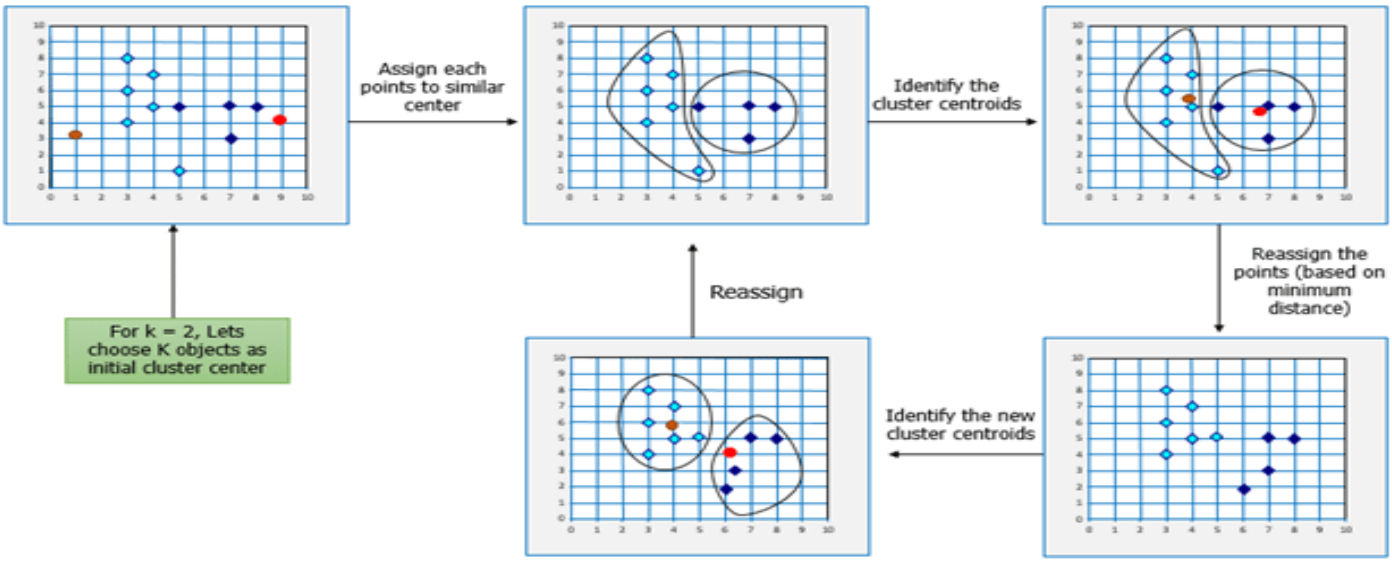
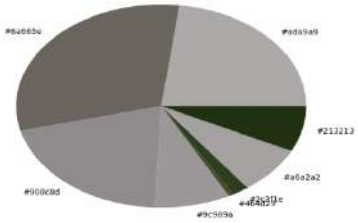
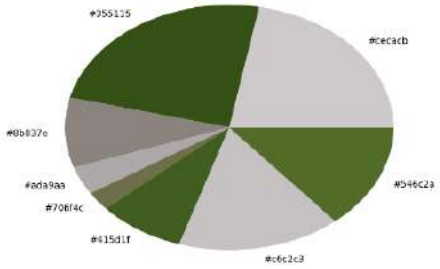


Fig. 3 A simple working model of K-means clustering

III EXPERIMENTAL RESULTS

Pre-processed images of the leaves were fed as input to the k-means clustering algorithm. The output of the algorithm is plotted using a pie chart in order to get a clear percentage of colours in the leaf. The results are presented as follows:





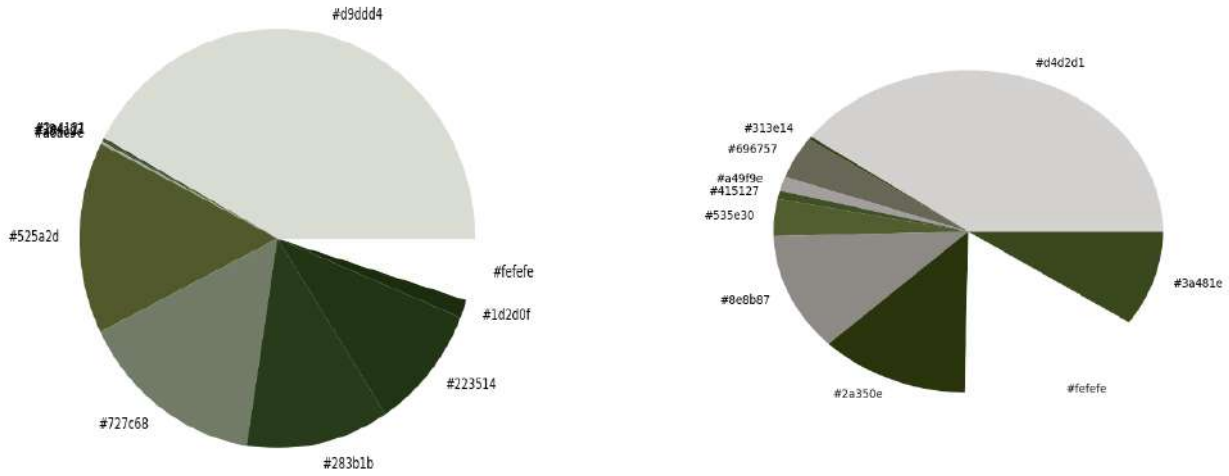


Fig 5: Results showing the colours extracted from four different leaves depicted in the previous section namely a,b,c and d.

IV CONCLUSION:

The approach proposed in this paper to identify the amount of colour present in an image of a leaf can be used to determine the freshness of a leaf. The application of this model is in food chain units where freshness of the food ,must be identified and retained. Automation of identification of the freshness using small pinhole camera with a microcontroller can be used to avoid food wastage. The percentage of different shades on the leaf is successfully extracted. Further, more work can be done to extract the amount of colour from images and predict if the leaf will decompose in a few days using machine learning algorithms. Also, notification can be sent to the store manager. More features of the leaf and its environment can be captured and predictions can be made.

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- The **BEST ENGINEERING COLLEGE** in India with **"AA"** Grade Ranked by Career 3600 Magazine.
- **Dr. M. V. SUBRAMANYAM,** Principal, received a National **PATENT CERTIFICATE** for his Research work in 2015.
- SREC Received **2 GOLD MEDALS** from JNTUA, Ananthapuramu and **8 PRATHIBA AWARDS** from the Govt. of A.P.
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- Received nearly **Rs.20,00,000/- worth AICTE/IE/UGC Research Projects**
- More than **500 RESEARCH ARTICLES** published in reputed publications
- Signed **MOU** with **LINCOLN UNIVERSITY, Malaysia** for bilateral R&D activities.
- Signed **MOU** with **NUCLEUS VISION (Eleven 01 Labs)** to promote Block chain Technology across Indian college students.
- Our student won the **GOLD MEDAL** in the **3rd HEROES TAEKWONDO INTERNATIONAL CHAMPIONSHIP, Thailand in 2017.**
- Secured 2nd prize in **AICTE CHHATRA VISWAKARMA AWARD, 2018**

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Information resource planning for a health-care System using Goal programming model

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Abstract:

This paper presents a goal programming (GP) model which aids in allocating a health care system's information resources pertinent to strategic planning. This GP model facilitates decision-making planning process and managerial policy in health-care information resources planning and similar planning settings.

Key words: *GP Model, Optimization, Decision-Making Planning Process, health-care information resources planning.*

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INFORMATION RESOURCE PLANNING FOR A HEALTH-CARE SYSTEM USING GOAL PROGRAMMING MODEL

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Abstract

This paper presents a goal programming (GP) model which aids in allocating a health care system's information resources pertinent to strategic planning. This GP model facilitates decision-making planning process and managerial policy in health-care information resources planning and similar planning settings.

Keywords—GP Model, Optimization, Decision-Making Planning Process, health-care information resources planning

1. INTRODUCTION

The data utilized to formulate the GP model is collected from the major health-care system in Hyderabad. The group of decision-makers involved in the strategic planning development process identifies the necessary goals and criteria. The goals and criteria are derived from the strategic plan of the health-care system. The success of the model is dependent on the accurate measurement of goals and criteria established by the group of decision-makers. **Tables 1 to 4** present the necessary data for GP model formulation.

Table 1 Project Categories and Available Budgets

Project Category	Resource Usage Rs. Lacs			Available Budget
	Year 1	Year 2	Year 3	
x_1	45	60	75	180
x_2	6	7	0	13
x_3	18	8	4	30
x_4	7	7	14	28
Total	**76**	**82**	**93**	**251**

Table 2 Annual Cost and Human Resources for Network Alternatives

Network Design	Resource usage Rs. Lacs		
	System Construction	System Manpower	System Software
Type 1 (x_5)	16	11	8
Type 2 (x_6)	18	12	8
Type 3 (x_7)	18	12	8
Available Budget	**22**	**15**	**9**

Table 3 Available Human Resources in Each Department

Human Resource	Department			Personnel level in shift
	Emergency	Radiology	Nuclear Medicine	
Physician	6	11	9	26
Nurse	20	-	-	20
Technician	-	45	18	63
Total	**26**	**56**	**27**	**109**

Table 4 Human Resource Distribution

Shifts	Available Personnel (Persons)					
	Emergency		**Radiology**		**Nuclear Medicine**	
	Physician	Nurse	Physician	Technician	Physician	Technician
Shift 1	2	6	10	26	5	12
Shift 2	3	8	1	12	3	4
Shift 3	1	6	-	7	1	2

2. GOAL PRIORITIZATION

Figure 1 presents the following goals for strategic information resource planning in a health-care system:

(G1) A budget allocation goal,

(G2) A project implementation goal,

(G3) A network construction goal, and

(G4) A human resource allocation goal.

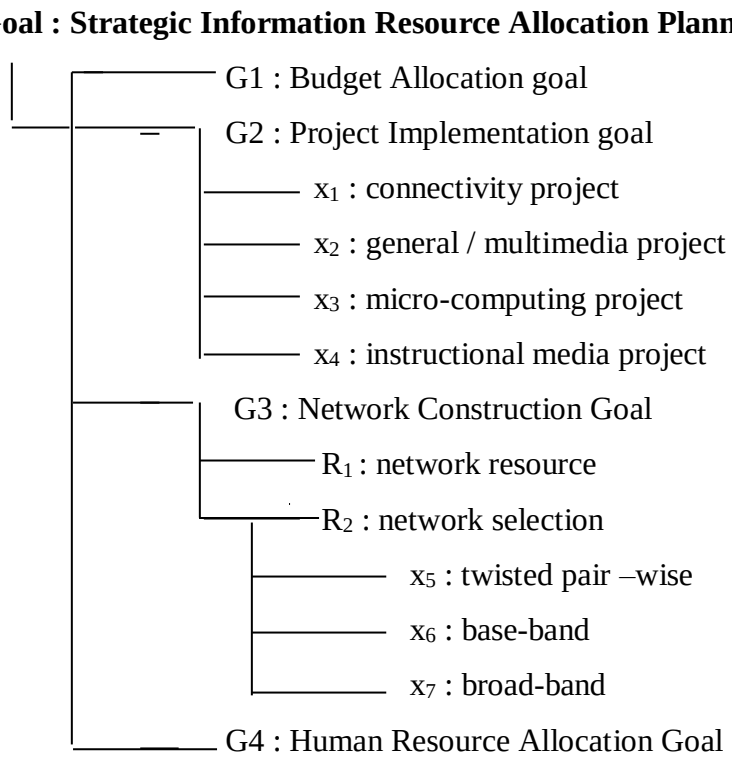

Figure 1 Goal Decomposition for Strategic Information Resource Planning

3. MODEL FORMULATION

In the model formulation, weighting of deviational variables at the same priority level can be considered to improve the GP solution method, since most goals are conflicting in terms of utilization of scarce resources. A numerical weight can be assigned to differentiate among goals at the same priority level. The coefficient of a numerical weight represents the relative value of unsatisfied deviation from the goal. Thus, the criterion to be used in determining the differential weights of deviational variables are the minimization of the marginal substitution cost [opportunity cost].

The generalized linear integer goal programming model can be stated as:

$$\text{Minimize } Z = \sum_{k=1}^{K} \sum_{i=1}^{m} w_{ki} P_k (d_i^- + d_i^+)$$

Subject to

$$\sum_{i=1}^{m} a_{ij} x_j + d_i^- - d_i^+ = b_i \qquad (j = 1, 2, \ldots n)$$

x_j, d_i^-, d_i^+ are non-negative integers $(i = 1, 2, \ldots m; j = 1, 2, \ldots n)$

Where Z = the sum of the weighted deviational variables

w_{ki} = the relative weight assigned to *k* priority level for the *i*th goal constraint

P_k = the *k* th preemptive priority

d_i^- = a negative deviational variable describing under-achievement of the *i*th goal

d_i^+ = a positive deviational variable describing over-achivement of the *i*th goal

a_{ij} = technical coefficient for the decision variable x

x_j = the *j*th decision variable x

b_i = the right-hand-side value for the *i*th goal constraint.

3.1 Decision Variables

The integer GP problem for this study consists of three different types of decision variables.

Firstly, there are four decision variables for four possible projects to which available amounts can be allocated over a three-year period. They are:

x_1 = connectivity project

x_2 = general / multimedia project

x_3 = micro-computers project

x_4 = instructional media project

Secondly, there are three decision variables for three types of network designs to be selected with various budgetary and resource constraints. They are:

x_5 = twisted pair-wire

x_6 = base-band coaxial cable

x_7 = broad-band coaxial cable

Thirdly, there are 18 decision variables related to the human resource allocation as follows:

x_8, x_{14}, x_{20} = number of physicians in the Emergency department in shift 1 (x_8), shift 2 (x_{14}) and shift 3 (x_{20})

x_9, x_{15}, x_{21} = number of nurses in the Emergency department in shift 1 (x_9), shift 2 (x_{15}) and shift 3 (x_{21})

x_{10}, x_{16}, x_{22} = number of physicians in the Radiology department in shift 1 (x_{10}), shift 2 (x_{16}) and shift 3 (x_{22})

x_{11}, x_{17}, x_{23} = number of technicians in the Radiology department in shift 1 (x_{11}), shift 2 (x_{17}) and shift 3 (x_{23})

x_{12}, x_{18}, x_{24} = number of physicians Nuclear Medicine department in shift 1 (x_{12}), shift 2 (x_{18}) and shift 3 (x_{24})

x_{13}, x_{19}, x_{25} = number of technicians in Nuclear Medicine department in shift 1 (x_{13}), shift 2 (x_{19}) and shift 3 (x_{25})

3.2 Constraints

The formulation of a GP model assumes that all problem constraints become goals from which to determine the best possible solution. There are two types of constraints in GP: systems constraints and goal constraints. System constraints are called the ordinary linear programming constraints or hard constraints which cannot be violated. Goal constraints are called the goal equations or soft constraints.

Systems Constraints 1. Select one of three network designs.

$$x_5 + x_6 + x_7 = 1 \qquad \text{.....(1)}$$

Systems Constraints 2. Balance human resources distribution in each department in each shift.

(a)desired number of physicians in emergency department in shift 1, shift 2 and shift 3

$$x_8 + x_{14} + x_{20} = 6 \qquad \text{……(2)}$$

(b)desired number of nurses in emergency department in shift 1, shift 2 and shift 3

$$x_9 + x_{15} + x_{21} = 20 \quad \text{.....(3)}$$

(c)desired number of physicians in radiology department in shift 1, shift 2 and shift 3

$$x_{10} + x_{16} + x_{22} = 11 \quad \text{.....(4)}$$

(d) desired number of technicians in radiology department in shift 1, shift 2 and shift 3

$$x_{11} + x_{17} + x_{23} = 45 \quad \text{.....(5)}$$

(e) desired number of physicians in nuclear medicine department in shift 1, shift 2 and shift 3

$$x_{12} + x_{18} + x_{24} = 9 \quad \text{.....(6)}$$

(f) desired number of technicians in nuclear medicine department in shift 1, shift 2 and shift 3

$$x_{13} + x_{19} + x_{25} = 18 \quad \text{.....(7)}$$

Priority 1 Allocate the health-care systems resources adequately, while the desired budget should:

(a) not exceed the available budget of all projects for a three-year period.

$$180x_1 + 13x_2 + 30x_3 + 28x_4 - d_8^+ = 251 \quad \text{.....(8)}$$

(b) not exceed the available budget for projects in year 1.

$$45x_1 + 6x_2 + 18x_3 + 7x_4 - d_9^+ = 76 \quad \text{.....(9)}$$

(c) not exceed the available budget for projects in year 2.

$$60x_1 + 7x_2 + 8x_3 + 7x_4 - d_{10}^+ = 82 \quad \text{.....(10)}$$

(d) not exceed the available budget for projects in year 3.

$$75x_1 + 4x_3 + 14x_4 - d_{11}^+ = 93 \quad \text{.....(11)}$$

Priority 2 Minimize the total cost to select an optimal network alternative by using:

(a) a total budget for system construction of Rs.22(lacs).

$$16x_5 + 18x_6 + 18x_7 - d_{12}^+ = 22 \quad \text{.....(12)}$$

(b) a total budget for system manpower of Rs.15(lacs).

$$11x_5 + 12x_6 + 12x_7 - d_{13}^+ = 15 \quad \text{.....(13)}$$

(c) a total budget for system software of Rs.9(lacs).

$$8x_5 + 8x_6 + 8x_7 - d_{14}^+ = 9 \quad \text{.....(14)}$$

Priority 3 Select the optimal network design.

$$x_5 + d_{15}^- - d_{15}^+ = 1 \quad \text{.....(15)}$$

$$x_6 + d_{16}^- - d_{16}^+ = 1 \quad \text{.....(16)}$$

$$x_7 + d_{17}^- - d_{17}^+ = 1 \quad \text{.....(17)}$$

Priority 4 Implement connectivity project – project 1.

$$x_1 + d_{18}^- - d_{18}^+ = 1 \quad \text{.....(18)}$$

Priority 5 Implement instructional media project – project 4.

$$x_4 + d_{19}^- - d_{19}^+ = 1 \qquad \text{……..(19)}$$

Priority 6 Implement general / multimedia project – project 2.

$$x_2 + d_{20}^- - d_{20}^+ = 1 \qquad \text{……...(20)}$$

Priority 7 Implement micro-computing project – project 3.

$$x_3 + d_{21}^- - d_{21}^+ = 1 \qquad \text{……...(21)}$$

Priority 8 Balance the utilization of human resource distribution.

(a) desired number of physicians in emergency department in shift 1, shift 2 and shift 3 gives :

$$x_8 - 2 + d_{22}^- - d_{22}^+ = 0 \qquad \text{……(22)}$$

$$x_{14} - 3 + d_{23}^- - d_{23}^+ = 0 \qquad \text{……(23)}$$

$$x_{20} - 1 + d_{24}^- - d_{24}^+ = 0 \qquad \text{……(24)}$$

(b)desired number of nurses in emergency department in shift 1, shift 2 and shift 3 gives :

$$x_9 - 6 + d_{25}^- - d_{25}^+ = 0 \qquad \text{……(25)}$$

$$x_{15} - 8 + d_{26}^- - d_{26}^+ = 0 \qquad \text{……(26)}$$

$$x_{21} - 6 + d_{27}^- - d_{27}^+ = 0 \qquad \text{……(27)}$$

(c)desired number of physicians in radiology department in shift 1, shift 2 and shift 3 gives :

$$x_{10} - 10 + d_{28}^- - d_{28}^+ = 0 \qquad \text{……(28)}$$

$$x_{16} - 1 + d_{29}^- - d_{29}^+ = 0 \qquad \text{……(29)}$$

$$x_{22} + d_{30}^- - d_{30}^+ = 0 \qquad \text{……(30)}$$

(d) desired number of technicians in radiology department in shift 1, shift 2 and shift 3 gives :

$$x_{11} - 26 + d_{31}^- - d_{31}^+ = 0 \qquad \text{……(31)}$$

$$x_{17} - 12 + d_{32}^- - d_{32}^+ = 0 \qquad \text{……(32)}$$

$$x_{23} - 7 + d_{33}^- - d_{33}^+ = 0 \qquad \text{……(33)}$$

(e) desired number of physicians in nuclear medicine department in shift 1, shift 2 and shift 3 gives :

$$x_{12} - 5 + d_{34}^- - d_{34}^+ = 0 \qquad \text{……(34)}$$

$$x_{18} - 3 + d_{35}^- - d_{35}^+ = 0 \qquad \text{……(35)}$$

$$x_{24} - 1 + d_{36}^- - d_{36}^+ = 0 \qquad \text{……(36)}$$

(f) desired number of technicians in nuclear medicine department in shift 1, shift 2 and shift 3 gives :

$$x_{13} - 12 + d_{37}^- - d_{37}^+ = 0 \qquad \text{……(37)}$$

$$x_{19} - 4 + d_{38}^- - d_{38}^+ = 0 \quad \text{.....(38)}$$

$$x_{25} - 2 + d_{39}^- - d_{39}^+ = 0 \quad \text{.....(39)}$$

Objective Function The objective function of a GP problem consists of deviational variables with preemptive priority factors for ordinal ranking and weighting at the same priority level.

The GP models objective function is formulated as

$$\text{Minimize } Z = P1(d_8^+ + d_9^+ + d_{10}^+ + d_{11}^+) + P2(d_{12}^+ + d_{13}^+ + d_{14}^+) + P3(0.392d_{15}^+ + 0.131d_{16}^+ + 0.184d_{17}^+) + P4(d_{18}^- + d_{18}^+) + P5(d_{19}^- + d_{19}^{+)} + P6(d_{20}^- + d_{20}^+) + P7(d_{21}^- + d_{21}^+) + P8 \sum_{i=22}^{39}(d_i^- + d_i^+)$$

4. RESULT AND ANALYSIS

The integer GP model used in this study contains 103 variables [decision and deviational], 39 constraints and 8 priorities. The solution of the problem is obtained by a QSB+ computer package. The possible solutions are enumerated at the first priority level and reduced at each subsequent priority level until overall goal achievement is no longer possible. The computer solution yields the following results as shown in **Table 5**.

The budget allocation goal (G1) is one of the most important overall goals for the strategic planning of resource allocation in the health care system. The priority is fully satisfied [P1=0]. All related deviational variables are zero [i.e.$d_8^+ = 0$,$d_9^+ = 0$, $d_{10}^+ = 0$ and $d_{11}^+ = 0$].

The network construction goal (G3) deals with two aspects: priority 2 and priority 3. Priority 2 of minimizing the total cost of network construction is fully satisfied [P2 =0]. All positive deviational variables are zero [$d_{12}^+ = 0$, $d_{13}^+ = 0$ and $d_{14}^+ = 0$]. But not all the negative deviational variables are zero [$d_{12}^- = 4$, $d_{13}^- = 3$, and $d_{14}^- = 1$]. The negative deviational variables, $d_{12}^- = 4$, imply savings of Rs.4,00,000 in system construction; $d_{13}^- = 3$, savings of Rs.3,00,000 in system manpower; and $d_{14}^- = 1$, savings of Rs.1,00,000 in system software.

Table 5 Solution Results

Decision Variables	Deviational Variables	Goal Priority	Goal Achievement
$x_1 = 1$	$d_{12}^- = 4$		
$x_2 = 1$		P1	Fully Achieved
$x_3 = 1$	$d_{13}^- = 3$	P2	Fully Achieved
$x_4 = 1$		P3	Fully Achieved
$x_5 = 0$	$d_{14}^- = 1$		
		P4	Fully Achieved
$x_6 = 1$			
$x_7 = 0$	$d_{15}^- = 1$	P5	Fully Achieved
$x_8 = 2$			
$x_9 = 6$	$d_{17}^- = 1$	P6	Fully Achieved
$x_{10} = 10$			
$x_{11} = 26$	$d_{34}^+ = 4$	P7	Fully Achieved
$x_{12} = 9$			
$x_{13} = 14$	$d_{35}^- = 3$	P8	Not Achieved
$x_{14} = 3$			
$x_{15} = 8$			
$x_{16} = 1$	$d_{36}^- = 1$		
$x_{17} = 12$			
$x_{18} = 0$	$d_{37}^+ = 2$		
$x_{19} = 2$			
$x_{20} = 1$	$d_{38}^- = 2$		
$x_{21} = 6$			
$x_{22} = 0$			
$x_{23} = 7$			
$x_{24} = 0$			
$x_{25} = 2$			

All other deviational variables are zeros.

Priority 3 of selecting the optimal network alternatives is fully satisfied [P3 =0]. The positive deviational variable d_{16}^+ is zero [$d_{16}^+ = 0$]. Among the three network design types, the decision variable in the network design type 2 is $x_6 = 1$. Thus network design type 2 is selected as the best network design with the given resource limitation.

As one of the overall goals in the health-care information resource planning, the project implementation goal (G2) provides the following GP solutions. All projects are selected for implementing, since P4, P5, P6 and P7 are fully satisfied and their associated deviational variables are zero [$d_{18}^- = d_{19}^- = d_{20}^- = d_{21}^- = 0$ and $d_{18}^+ = d_{19}^+ = d_{20}^+ = d_{21}^+ = 0$].

One of the overall goals in the health-care information resource planning is the human resource allocation goal (G4). Priority 8 of balancing the human resource distribution is not satisfied. The following deviational variables are not zero: $d_{34}^+ = 4$, $d_{35}^- = 3$, $d_{36}^- = 1$, $d_{37}^+ = 2$, $d_{38}^- = 2$. Decision-makers focus on balancing the current manpower flow in each individual subsystem (i.e. each individual department), while providing proper health-care services to patients as well as maximizing the utilization of total manpower. Since the human resource allocation goal (G4) is not satisfied, this means that the target levels of human allocation are not achieved. d_{34}^+ indicates that 4 extra physicians are needed in the nuclear medicine department in shift 1. Likewise, $d_{35}^- = 3$ and $d_{36}^- = 1$ indicates that three physicians in the nuclear medicine department in shift 2 and one physician in shift 3 are under-allocated. $d_{37}^+ = 2$, indicates that two extra technicians are needed in nuclear medicine department in shift 1 and $d_{38}^- = 2$, indicates that two technicians in the nuclear medicine department in shift 2 are under- allocated.

5. CONCLUSION

Several new goals and criteria, along with new objectives, need to be formed to improve the health-care systems overall effectiveness. Therefore, decision-makers should attempt:

(i) To improve the satisfaction of patients who are the end-users of the health-care system.

(ii) To provide more assistance to faculty and staff of the academic area in the system, and

(iii) To establish partnerships with other health-care systems.

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Comparison of Wavelets for EEG Denoising

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Abstract

EEG signals which are used in recognition of diverse cerebrum diseases is prone to divergent noises because of its small amplitudes. In this paper, we are going to denoise the EEG signal by executing the amalgamation of stationary wavelet transform (SWT) and discrete wavelet transform(DWT). We have also incorporated universal threshold estimation (UTE) and statistical threshold estimation(STE) for the wavelets symlet,haar,coif and bior4.4.To examine the fulfiment of these wavelets, we used four perform -ance parameters namely Signal to Artifacts Ratio (SAR),Correlation Coefficient(CC) and Normalized Mean Square error (NMSE). MATLAB has been used to implement the denoising of EEG signal.

Keywords: *EEG, denoising, SWT, DWT, UTE, STE, SAR, CC, NMSE, MATLAB*

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Abstract: EEG signals which are used in recognition of diverse cerebrum diseases is prone to divergent noises because of its small amplitudes. In this paper, we are going to denoise the EEG signal by executing the amalgamation of stationary wavelet transform (SWT) and discrete wavelet transform(DWT). We have also incorporated universal threshold estimation (UTE) and statistical threshold estimation(STE) for the wavelets symlet,haar,coif and bior4.4.To examine the fulfiment of these wavelets, we used four perform -ance parameters namely Signal to Artifacts Ratio (SAR),Correlation Coefficient(CC) and Normalized Mean Square error (NMSE). MATLAB has been used to implement the denoising of EEG signal.

Keywords: EEG, denoising, SWT, DWT, UTE, STE, SAR, CC, NMSE, MATLAB

1. INTRODUCTION

Electroencephalogram which is generally abbrev -iated as EEG is used to evaluate the electrical activity in the brain. Brain cells communicate with each other through electrical impulses. An EEG can be used to help detect potential problems associated with this activity. The targets of EEG analysis are to help researchers gain a better understanding of the brain;assist physicians in diagnosis and treatment choices; and to boost brain-computer interface (BCI) technology.Wavelet transform is like a mathemat -ical microscope that can analyze different scales of neural rhythm and investigate small scale oscillation of the brain signals while ignoring the contribution of other scales. The two prime roots of noise are anatomical and ancillary anatomical. Anatomical comprises of muscle,eye and cardiac movements while recording EEG signal where as ancillary anatomical consists of line intercession and wire noise. Because of the presence of ghastly severance for ancillary anatomical noises, can be eliminated by approximate filtering techniques. Wire noise can be abolished by notch filter. Classical band pass filters cannot be used to immaculate the EEG signal due to the mix up of white noise power spectral density, optic and thew functions with that of the power spectral density of the EEG signal. Before the analysis of EEG signal, it should be preprocessed as it becomes laborious to examine the raw data. Numerous approaches have been presented for denoising process. Denoising of EEG signal using wavelet transform shows better results [1]. A study on different EEG signal noise removal methods have been discussed in [2]. The efficacy of the wavelet denoising methods on epileptic and healthy EEG signal is collated by the means of root mean square [3]. The denoising of EEG signal is carried out using IIR low pass filter, FIR low pass filter and wavelet algorithms. Signal to noise ratio(SNR) and minimum mean square error(MSE) are incorporated to correlate [4]. The sure-thresholding technique is applied on wavelets and rectified the noise occured due to eye blinks,eyeball movements and facial muscle movements in EEG [5]. The adaptive filtering method which uses RLS(Recursive Least Square) algorithm has been proposed to remove ocular artifacts present in the EEG signal [6]. The unsupervised wavelet transform decomposition technique was incorporated to remove ocular artifacts for a single-channel EEG system [7]. Cerebral EEG rhythms have been extracted using multiresolution analysis which is based on wavelets [8]. The process of extracting the contrast in the approximation of a signal at two levels 2^{j+1} and 2^{j} using wavelet orthonormal basis decomposition has been shown [9]. Application of wavelet analysis to neuroelectric wave forms like EEG and ERP and conceptual introduction has been presented [10]. The time-invariance issue faced by orthonormal wavelet transform has been solved by extending wavelet packet decompositions and also revealed that time-in variance can be achieved by preserving the orthonormality [11]. A analytical method for separating ocular noises in EEG signal using wavelet transform without EOG reference channel has been presented [12].

2. PROPOSED SYSTEM

Initially the noisy EEG data is subjected to the preprocessing.Preprocessing is a process of

converting raw data into a usable format for analysis. Preprocessing plays a crucial role as the signals collected from scalp looses the spatial information.

We are using four wavelets over here namely haar,sym4,coif4 and bior4.4. A wavelet is a swing-like structure which originates from zero,surges and then decays to zero.Using Convolution, wavelets can be coalesced with known parts of a blighted signal to extricate information from unknown parts.

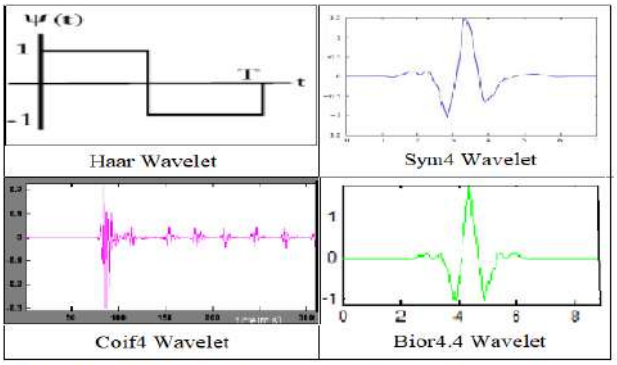

Fig 1: Mother Wavelet Functions used for EEG denoising

Discrete Wavelet Transform(DWT)

A wavelet transform where the wavelets are disjunctly sampled.The focal advantage possessed by DWT over fourier transform is temporal resolution along the other wavelet transforms. It is non-redundant and most coherent transform for resolution of a signal at several levels using wavelets.The signal is made to pass through several high pass and low pass filters till the required frequency range to obtain the detailed and approximate coefficients.

Stationary Wavelet Transform(SWT)

The major drawback of the DWT is time-variance which is achieved by stationary wavelet transform(SWT).It is redundant and comparatively less coherent where the length of the coefficients is as the raw data.The coefficients are upsampled by a factor of $2^{level-1}$ after individual level.

3. THRESHOLD ESTIMATION

The threshold is calculated and appertained

on the coefficients obtained after wavelet transform.

Universal Threshold Estimation is calculated as

$U^2 = 2 \log m\sigma$ (1)

$\sigma^2 = \text{median}(1.482*|C_i|)$ (2)

Where U = Amplitude Estimation

m = Length of the data

C_i = Wavelet Coefficient at i^{th} resolution level

Statistical Threshold Estimation is calculated as

$S = 1.504* \text{std}(C_j)$ (3)

Where S = Amplitude Estimation

$\text{std}(C_j)$ = Standard deviation of wavelet coefficient

at j^{th} level

Generally, the values of the soft threshold lies between 0 and 0.5 and the values of hard threshold lies between 0.5 and 1. In case of soft threshold, if the utter value of wavelet coefficient exceeds the threshold value, threshold value is docked from the coefficients else the coefficients are kept back.In case of hard threshold, if the utter value of wavelet coefficient exceeds the threshold value, wavelet coefficients are kept back else the wavelet coefficient value is made zero.Generally,hard thresholding outperforms soft thresholding.

4. PERFORMANCE PARAMETERS

Correlation Coefficient(CC), Signal to Artifacts Ratio(SAR), Normalized Mean Square Error(NMSE) are the performance metrics used to evaluate the efficacy of each wavelet with common EEG signal as input.

Correlation coefficient is calculated as follows

$$CC(x, y) = \frac{Co(x, y)}{\sigma_x * \sigma_y} \quad (4)$$

Where Co(x,y) = covariance of two coefficients

σ_x = standard deviation of x

σ_y = standard deviation of y

Signal to Artifacts Ratio is calculated as follows

$$SAR = 10\log\left(\frac{\sigma_s}{\sigma_k}\right) \quad (5)$$

Where s = input signal

s1 = denoised signal

k = s - s1

σ_s = standard deviation of s

σ_k = standard deviation of k

Normalized Mean Square Error is calculated as follows

$$NMSE = 20\log\left\{\frac{\sum_{k=0}^{m}[s(k) - s1(k)]^2}{\sum_{k=0}^{m}[s(k)]^2}\right\} \quad (6)$$

Where m = length of the data

s = input signal

s1 = denoised signal

The above parameters and the wavelet coefficients are calculated using matlab.

5. RESULTS

The wavelet coefficients for individual wavelets are obtained and the threshold estimations are computed solely for wavelets and imposed on the coefficients.Thereafter, the performance parameters are enumerated and the performance of each wavelet is compared with other wavelets.

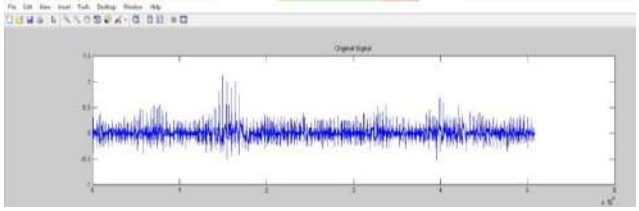

Fig 2 : Noisy EEG signal

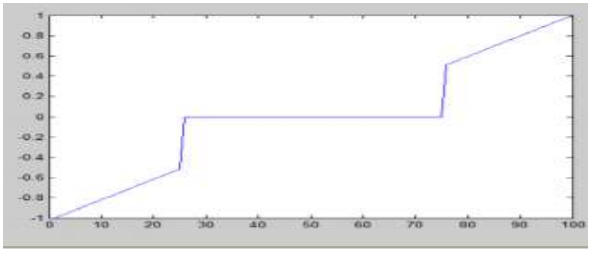

Fig 3 : Hard Threhold

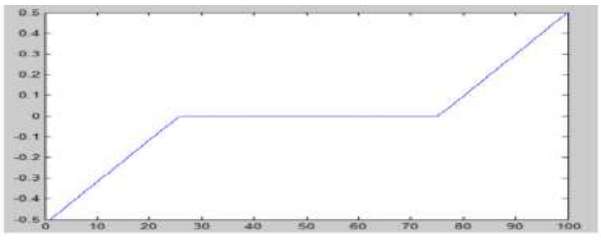

Fig 4 : Soft Threshold

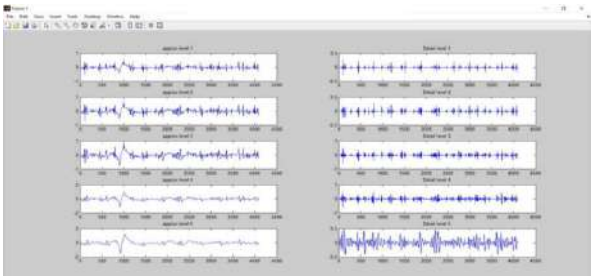

Fig 5 : Detailed and Approximate Wavelet Coefficients

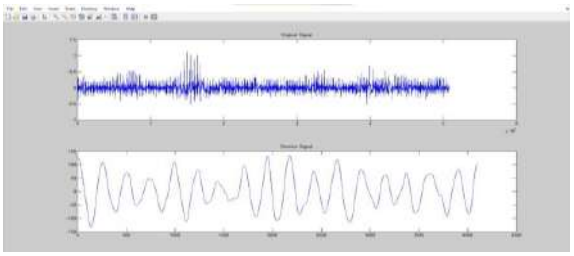

Fig 6 : Noisy signal and Denoised Signal

6. CONCLUSION

Ultimately, on the basis of all the performance parameters, the feasible result for the better denoised signal have given by coif4 and bior4.4 wavelet. When focussed only on the performance parameter correlation coefficient, haar outperformed others

.

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Design and Implementation of Dadda Multiplier for FIR Filters by Compressors

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Abstract

During this paper, we tend to propose compressors 4:2, which can have the pliability to change between the precise operational mode and approximate operational mode. Multiplication is the essential function of arithmetic operation. In signal process applications multiplication primarily based operations like multiply and Accumulate unit (MAC), convolution, quick Fourier remodels (FFT), filtering (FIR) area unit wide used. In DSP systems, multiplication dominates the execution time; therefore, there's a necessity to develop associate degree high-speed multipliers.Within the approximation mode, the dual quality compressor provides higher speeds and lower power consumption by neglecting accuracy. Every one of these compressors in approximate mode has its level of accuracy, equally as utterly completely different power dissipations and delaysat approximate mode, actual mode.Within the body of parallel multipliers, these compressors provide configurable multipliers whose powers,accuracies, and speeds could cause modification dynamically within the runtime. In Xilinx ISE 14.7, efficiencies of those compressors in an exceedingly 32-bit Dadda number for FIR Filter area unit evaluated withinVerilogHDL and simulated and synthesized. Scrutiny the parameters with the prevailing Wallace tree multiplier designed utilizing 4:2 and 5:2 compressor. The comparison results indicate the lesser delay and power intake within the approximate mode.

Keywords: *Approximate Computing, Configurable 4:2 Compressors, Accuracy & Delay.*

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DESIGN AND IMPLEMENTATION OF DADDA MULTIPLIER FOR FIR FILTERS BY COMPRESSORS

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Keywords: approximate computing, configurable 4:2 compressors, accuracy & delay.

1. INTRODUCTION

Digital filters have a strong play in varied digital signal method applications. Filtering will be done to induce the desired output by manipulating input data. The elemental operation of a digital filter is to need a sequence of input numbers and figure a special sequence of output numbers. The Finite impulse response (FIR) filters unit wide utilized in varied DSP application. The FIR Filter consists of 3 basic modules that unit flip-flops, adder blocks and number blocks. The numbers regulate the performance of the FIR filter, that's that the slowest block out of all. Throughout this project, multiplication is finished by Dadda number that will be implemented with any one of the four planned compressor. Throughout this project, we've got an inclination to propose the four 4:2 compressors that have a pliability of switching between the precise operational mode and approximate operational mode. Among the approximate mode, this dual-quality compressor gives less power consumption, higher speeds at a price of lesser accuracies. Every one of those compressor has its level of accuracy among approximate modes, however, totally fully totally different delays & power dissipation among the approximate mode and actual mode. Pattern of compressors among the structures of a parallel multipliers provide configurable multiplier whose accuracies, powers and speeds might modification dynamically throughout the run-time. Efficiencies of proposed compressors throughout a 32 bit Dadda number unit evaluated throughout a 45-nm commonplace CMOS-technology by examining their parameters and comparing with those of the progressive approximate multipliers. Results of these comparisons indicate on average of forty-sixth and sixty-eight lower delay and power consumption among the approximate mode. Similarly, the effectiveness of these compressors is evaluated by some image method application. The planned style of this project analyzes the logic area, size, and power consumption.

Motivated by restricted analysis on approximate multiplier, compared with the full analysis on approximate adder, and expressly the

shortage of approximate technique targeting a partial product generation and we've got an inclination to debut the partial product perforation methodology for making approximate multiplier. We've got an inclination to omit an generation of some partial merchandise, thus decreasing the number of partial merchandise that required accumulating; we've got an inclination to decrease the ability and depth of the build-up tree.

2. LITERATURE SURVEY

We have referred to various IEEE papers and international journals. The FIR filter projected with the proposed compressors is coded in Verilog, Synthesized, and Simulated using ISE Simulator.Xilinx FPGA is employed for Hardware realization and Verification. It's projected to match resource utilization and temporal order performance of the projected filter style thereupon of existing ones.

A. Afzali-Kusha, O. Akbari, M. Kamal, and M. Pedram projected a quick, however energy efficient reconfigurable approximate carry look-ahead adder (RAP-CLA). Adder like this has the pliability of modification between the approximate and precise operational modes making it acceptable for every error-resilient and precise application. The structure, that could be a heap of area and power economical than progressive reconfigurable approximate adders, is achieved by some modifications to the quality carry look-ahead adder (CLA). It is to be noticed that each of those approaches given in [1] suffers from high relative errors. In [2], the field of approximate computing has received vital attention from the analysis community within the past few years, particularly in sight of assorted applications of signal process. Video and compression algorithms, like MPEG, JPEG, and so on.

In [3], configurability and low quality unit the 2 key wants of the finite impulse response (FIR) filters utilized in multi customary wireless communication systems. In this, 2 new reconfigurable architectures of low-quality FIR filters square measure projected specifically constant shifts methodology and programmable shifts methodology. In FIR Filter Realization, Transpose kind of FIR filters support multiple constant multiplication (MCM) technique are naturally pipelined which leads to saving major a part of computation as planned in [4]. In [6], the need to support various signal processes (DSP) and its applications on energy-constrained devices has mature up steady. Such applications sometimes extensively use fixed-point arithmetic to perform matrix multiplications, whereas exhibiting tolerance for a couple of procedure errors. In [7], they specifically focused on multiplication operation and proposed a novel approximate multiplier factor with a dynamic vary choice theme. They designed the multiplier factor to possess associate degree unbiased error distribution, which ends up in fewer process errors. In [8], the programmable complexity of VLSI digital filters is dominating by the number of adders used in the implementation of the multipliers using fixed-point binary multiplier coefficients. In this, three new algorithms for the multiplier block design as described, an efficient modification to an existing algorithm gives better results, and a hybrid of these two, which trades off performance against computation time.

In [9], W. L. Goh, K. Y. Kyaw and K. S. Yeo. proposed an algorithmic approach of multiplier design where the input to the multiplier is divided into two parts (a) multiplication part to generate the higher-order bits of the productand (b) non-multiplication part to give the lower order bits of the final output. Vaibhav Gupta [10] proposed an inaccurate or rather say approximate adder structure, which can be used in many applications, including multiplication. Their proposed design contains a schematic level of changes with the main goal of switching power reduction with less number of transistor uses. Parag Kulkarni [11] proposed an approach of architecture modification of a multiplier block where inaccuracy is introduced only when all the input bits are 1.Economakos & Anagnostopoulos. (2006) conferred a method for the look of low power array multiplier factor. The appliance of this technique within the implementation of a Carry-Save array multiplier factor produces important gains in power consumption, creating it ideal for the implementation of power economical DSP VLSI systems.

3. EXISTING SYSTEM

First, some basic knowledge on the compressor 4:2 had given. Schematically, this sort of compressor device shown in Fig. 1 has four inputs (x1–x4) in conjunction with input carry (Cin) and two outputs (carry and sum) in conjunction with output Cout. The internal structure of a certain 4:2 compressor device consists of 2 internally connected full adder cells as shown in Fig. 2. During this structure, the weights of all the sum outputs & inputs are same, whereas the weights of the Cout & carry outputs area unit one binary bit position higher.

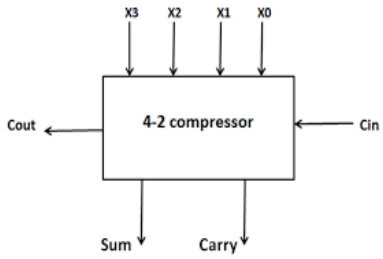

Fig.1: Block diagram of [4:2] compressor

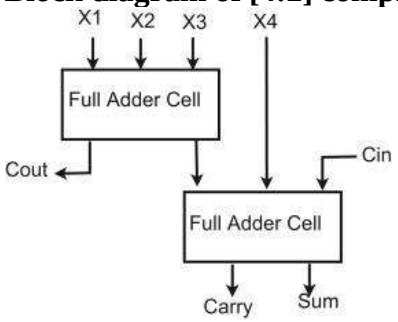

Fig.2: Structure of the conventional [4:2] compressor

The 4:2 compressor trees additionally contain a regular structure and sum the partial product as a binary tree will, victimization 4:2 compressors rather than CSAs.

4. PROPOSED SYSTEM

In this study, we tend to introduce four dual-quality reconfigurable approximate 4:2 compressors that provide pliability between precise & approximate operational modes throughout the run-time. The fundamental structures of the planned compressor accommodate a pair of parts of supplementary & approximate. Within an actual operative mode, supplementary half alongside with some elements of the approximate half area unit active, wherever as within the approximate mode solely an approximate half is active.

The general diagram of the compressors is shown in Fig.3 within the projected structure; to chop back the power consumption & space, majority of the components of an approximate half are utilized throughout the precise operational mode. We tend to utilize the ability gating technique to turn off the unused elements of approximate half. Furthermore note that, as it is clear from Fig. 3, within an actual operative mode, tri-state buffer area unit used to disconnect the output of the approximate half from the first outputs, the supplementary a section of this structure is associate in nursing exact 4:2 compressor devices. At intervals, precise operational mode the delay of this structure is identical to that of the 4:2 compressor devices.

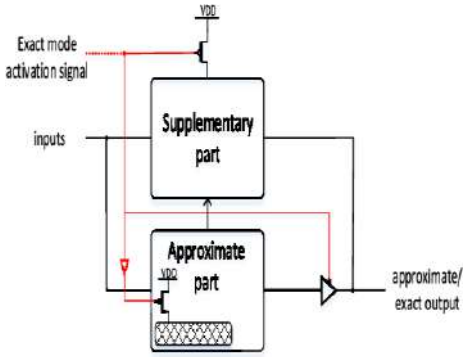

Fig.3: Block diagram of the proposed system

A) Structure 1 [DQ4:2C1]: In the approximate a part of primary projected DQ4:2C1structure, as shown in Fig.4 (a), approximate output carry (i.e., carry) is directly linked to input x4, within the same manner, the approximate output add (i.e., sum) is directly linked to Input x1 (sum = x1). The output Cout is neglected inside the approximate a part of this structure. The approximate part of this structure is undoubtedly fast & consumes less power; however, its error rate is large (62.5%).

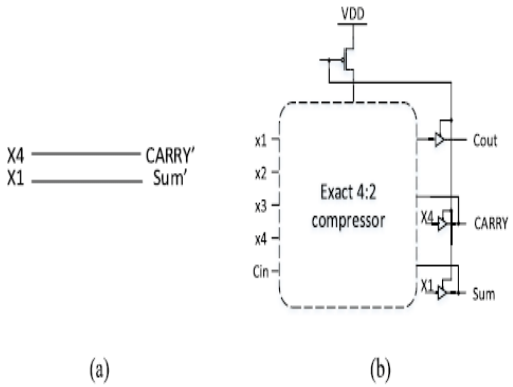

Fig.4: (a) Approximate part of (DQ4:2C1) and (b) overall structure of (DQ4:2C1)

B) Structure 2 (DQ4:2C2): In the structure 1, whereas neglecting Cout, simplifies the inner structure for reduction stage of the multiplication, but its error was huge. Within structure 2, compared with structure 1, the output Cout is generated by joining it on to input x3 within the approximate half. Fig. 5(a) shows inner structure of an approximate half & also the entire structure of DQ4:2C2. Whereas the error rate of structure is the same as that of [DQ4:2C1 (62.5%)].

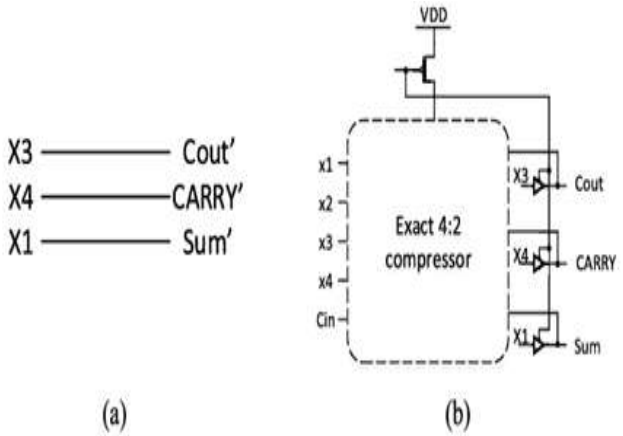

Fig.5: (a) Approximate part of [DQ4:2C2] and (b) overall structure of [DQ4:2C2]

C) Structure 3 (DQ4:2C3): The previous structures, at intervals the approximate operational mode, have the most force and deferred decreases contrasted and those of the exact compressor.

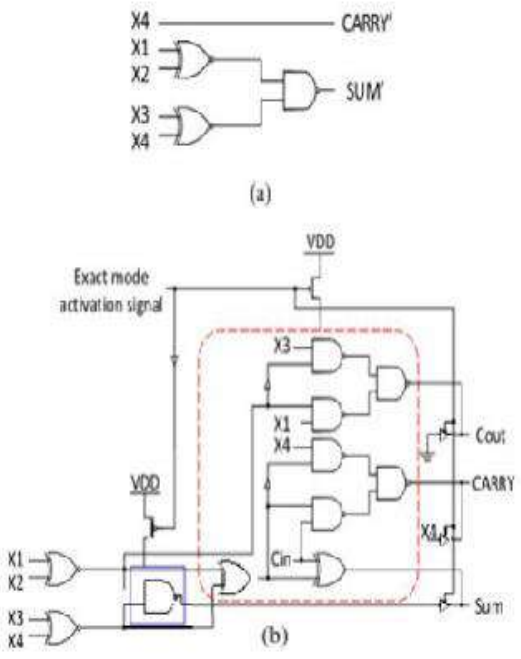

Fig.6: (a) Approximate part of [DQ4:2C3] and (b) overall structure of [DQ4:2C3]

In some applications, however, more robust accuracy is even being needed. Inside structure 3, the accuracy of approximate operational mode is improved by increasing the standard of the approximate half whose internal structure is shown in Fig. 6(a). Throughout this structure, the accuracy of the output sum is enlarged. An equivalent as DQ4:2C1, the approximate a section of this structure does not support output Cout. Error rate of this structure, however, is reduced to 5 hundredths.

D) Structure4 (DQ4:2C4): In this structure, we have tend to improve the accuracy of output carry comparing with DQ 4:2C3 at price of bigger delay & power intake wherever the error rate is decreased to thirty-one 31%. This mechanical device style additionally consists of 2 operative modes. The internal structure of the approximate half & also the overall structure of DQ 4:2C4 unit exhibited in Fig. 7. The supplementary half is shown with broken rectangular red line, whereas the gates of approximate half, powered off throughout the precise operational mode shown using the blue line.

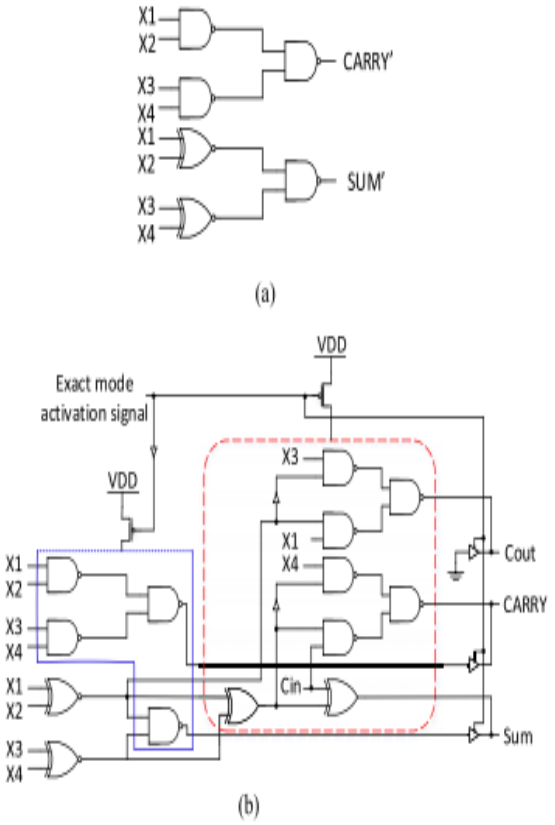

Fig.7: (a) Approximate part of [DQ4:2C4] and (b) overall structure of [DQ4:2C4]

5. STUDY OF MULTIPLIER CREATED WITH PROPOSED COMPRESSORS

In this project, we have a tendency to analyze the trade-off accuracy and energy conservation of mounted dimension multiplier factor in image process applications. In most cases mounted purpose arithmetic is employed to stay the dynamic ranges inside the bound limit primarily based accuracy trade-off over resource constraints our projected approximated multiplier factor use consecutive 4:2 mechanical device units that apply on partial product accumulated supported dadda multiplier factors that have the leading ones from 2 operands to associate degree m×m multiplier. a certain approximation followed by tree primarily based pp reduction provides hefty quality reduction and additionally consumes abundant less energy and space than direction truncation approaches

5.1Dadda Multiplier

Dadda proposed a reduction method that achieves the reduced two-rowed partial products in a minimum number of reduction stages. Dadda succeeded this by placing the [2,2] and [3,2] compressors in the maximum critical path in an optimal manner. In this project, we use [4,2] compressors, which were proposed in the above section in order to increase speed and also to reduce complexity. By making use of compressors, accuracy is also improved. For example, an N-bit multiplier and N-bit multiplicand, multiplication process results in an N by N partial product. The partial products obtained are arranged in the form of a Matrix. The N by N Matrix so formed is reduced into a two-rowed matrix, by following a sequence of reduction stages.

5.2 Algorithm for 8*8Dadda multiplier

1. In the first reduction stage, the column compression is carried with the [4,2],[3,2], and [2,2] compressors such that the reduced matrix height, which is obtained, should not exceed 4.
2. During the compression, the sum is to be passed to the same column, which is to compress in the next reduction stage, and carry is to be passed to the next column.
3. The above two steps are to be repeated until a two-rowed reduced matrix is obtained.
4. Now, the result can be obtained by reducing the two-rowed matrix using adders.

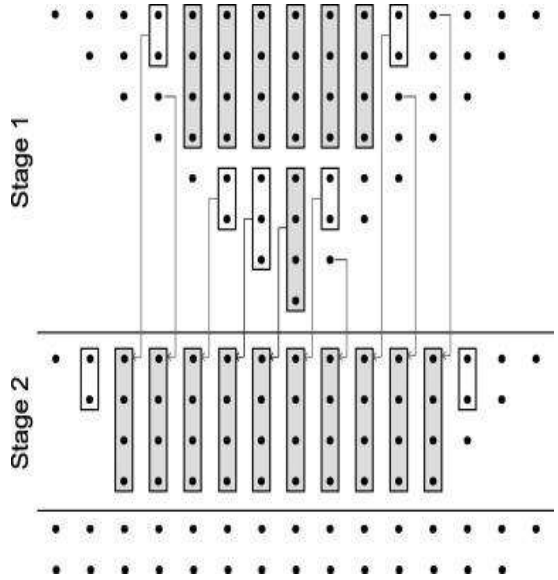

Fig.8: Dot diagram of 8*8 data multiplier using 4:2 compressors

The general structure of the reduction of electronic equipment in associate 8-bit Dadda multiplier factor that makes use of 4:2 compressors is shown in Figure.9. Dadda multipliers need less space and square measure slightly quicker than Wallace tree multipliers. Among tree multipliers, the Dadda multiplier factor is that the hottest multiplier factor. Dadda multipliers arrange to minimize the input and output delay moreover because of the range of gates used. The importance of the dadda multiplier factor is that it makes use of a minimum range of gates to perform multiplication.

6. IMPLEMENTATION OF THE FIR FILTER DESIGN

The FIR filter is generally utilized to compute the sum of an input signal by analyzing different types of accumulating and multiply operations. The structure of the filter is described by the differential equation, which is represented with general elements like adders, time delays and multipliers.

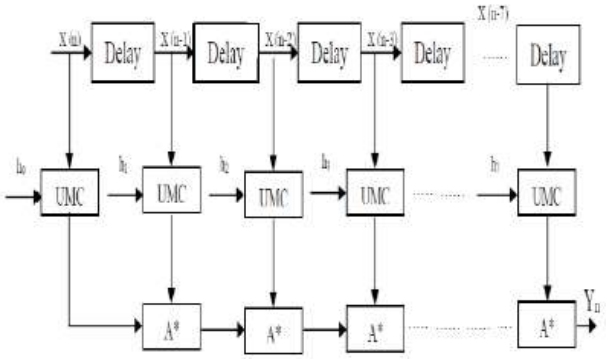

Fig.9: Block diagram of FIR filter

The input signal is multiplied by a series of constant coefficients. Input data is forwarded to either the coefficient bank or sample register based on the given input to control unit. In sample register, the sample values are recorded, whereas the coefficient bank is used to store the multiple coefficients. Coefficient bank is designed to store a maximum of 256 coefficients. The coefficient bank and the sample output are given as inputs to the Dadda multiplier. The multiplication and accumulation process continues. And output gets stored in the fir filter register.

7. RESULTS

Dadda multipliers using the proposed compressors are implemented in the FIR filter design. The results of the area, power and delay are analyzed and compared. Also, Xilinx was used to synthesize and simulated the design, and the parameters of the existing system were also taken as reference values in order to compare with the proposed design. Fir filteris designed, analyzed, and simulated using Xilinx ISE 14.7. TheRTL block diagram is shown in Fig. 11.

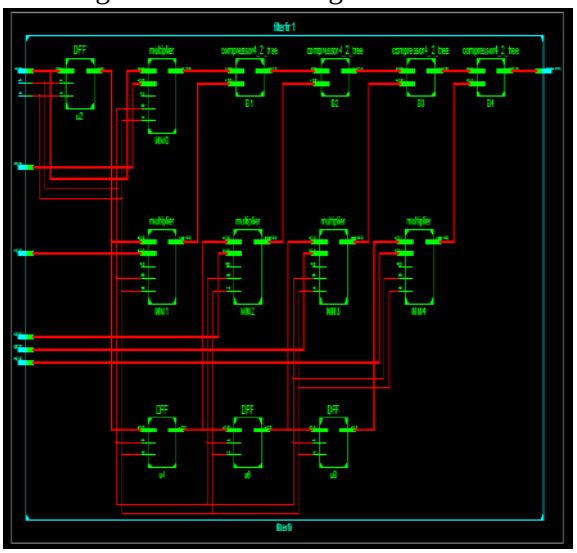

Fig.10: RTL Schematic of the proposed FIR filter

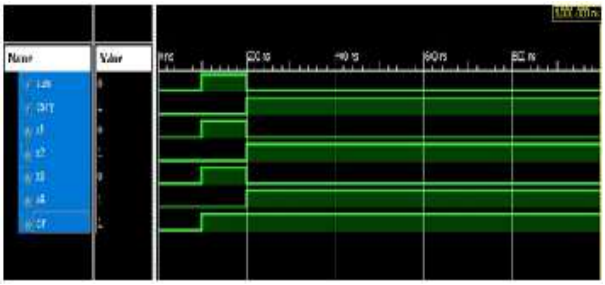

Fig.11: Dual quality compressor DQ4:2C1 simulation

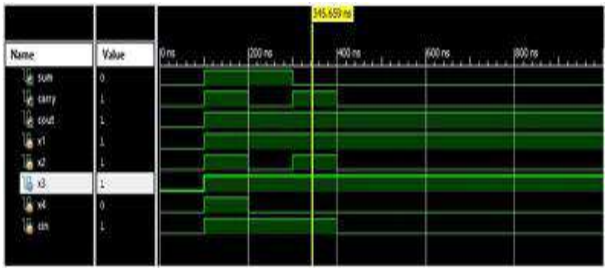

Fig.12:Dual quality compressor DQ4:2C4 simulation

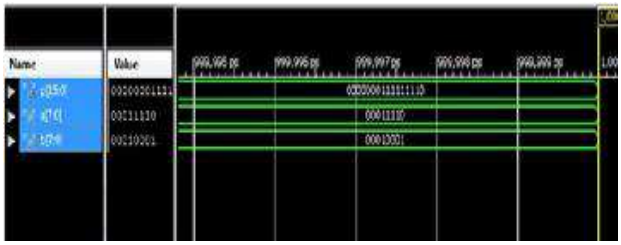

Fig.13: 8x8 Dadda Multiplier Simulation

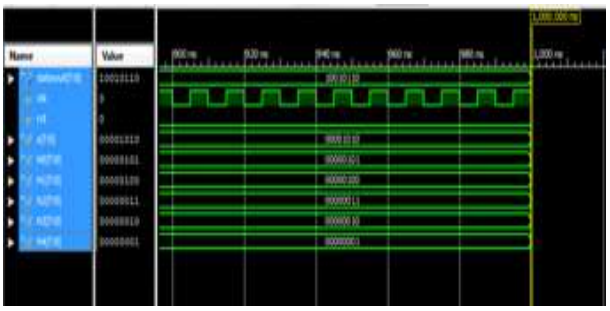

Fig.14: FIR Filter Simulation

8. CONCLUSION

The approximate compressors area unit accustomed build dadda multipliers that allocate the approximate compressors with the aim of optimizing electrical performance, whereas providing little error. The projected fourDQ4:2Cs had the flexibleness of modification between the precise operative mode and approximate operative mode. Inside the approximate mode, these compressors provided less power and higher speeds consumption at the price of lower accuracy. Every one of those compressors has its own level of accuracy inside the approximate mode, furthermore as totally different delays and powers inside the approximate and precise modes. The projected approximate compressors area unit styled and analyzed for 8-bit dadda number and also the multipliers area unit enforced in FIR filter design. The results of fir filter style space, power and delay parameters area unit analyzed. The simulation results area unit enforced for the filtering application by victimization Xilinx ISE style suite 14.7.

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Design and implementation of High speed and Low power FIR used in EEG analysis

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***Abstract*— The power and area management of a transistor on silicon has become a vital role in finite impulse response (FIR) filters, both of the above parameters are important in current CMOS large scale integration manufacturing industry. Multiplier has become basic building block in electroencephalogram (EEG signal), Digital signal processing and in communication system. It is utilized in signal and image processing applications including fast Fourier transforms convolution and correlation. Hence it is mandatory to design and develop a low power and energy efficient finite impulse response filter. In this paper 2x2 and 4x4 finite impulse response filter has been proposed with simulation results which consume less power. The proposed Finite impulse response filter consist of Multiplier, adder, it has been designed with basic building blocks of universal gates, half adder and full adder by using CMOS physical designed tool Mentor graphics 0.25um based Tanner tool to reduce the number of transistors utilized in compare with other ISE EDA simulation soft wears.**

Keywords— ***FIR, universal digital gates, combinational multiplier, low power, high throughput***

1. INTRODUCTION

Recent advances in electronics and communication engineering applications demand high speed and low power VLSI digital signal processing modules. [1][2] Many previous experts have focused on realization of FIR filters, in this paper we are going to implement FIR filter behavior by using CMOS transistors. Many applications require high speed low power FIR filters.[3] The development in the field of electronics and communication engineering has identified the research to design high speed and low power FIR filters using traditional concepts. Filters play an important role in the field of communications, radar, microwave frequency, mobile communications, Antennas engineering. Filtering [4] is the class of signal processing in which suppress any unwanted signal in the finite signal frequency. And reduce any interfacing coming from the neighbor signals.

Filters are basically two types' first analog filters and second digital filters. In digital filter FIR filter play an important role according to the requirement such as filtering based on window technique.

FIR filters [5] are good because of their construction and working principles. Basically FIR filters have a finite number of input samples.

In this paper we implemented the FIR filter basic building blocks using CMOS transistors. The basic building blocks of FIR filters are 1. Delay elements 2. Multiplication circuit and 3. Summer circuit.

II. LITERATURE SURVEY

A finite impulse response filter can be realized by using either mat lab or through Xilinx integrated synthesis environment (ISE) [6] or full custom design with a certain process design kit (PDK). There are many techniques to realize FIR filters [5]. Each has its own important in terms of speed, linearity, power consumption and area. But whereas for implantation the above parameters will not perform in better way because of tool environment limitations. Out of those techniques which we had to designing FIR filter, implant with Physical design tool is a wise choice shown in Figure 14: a ,b and table [2]. Hence this paper proposed to implement finite impulse response (FIR) all the basic building blocks in CMOS [6] physical design EDA

III. IMPLEMENTATION & RESULTS

To design digital FIR filter [5] the basic primitive building blocks are shown in the Fig.1.And those are:
1. Delay element.
2. Multiplier & Summer circuit

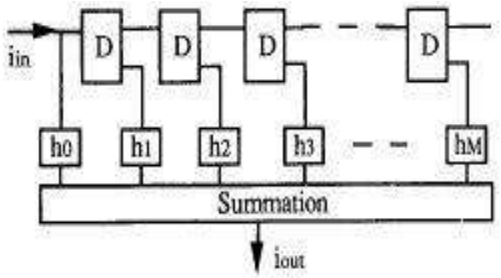

Figure1: Conventional schematic of FIR filter

1. Delay element:

Which is an element transferred data with low time delay in this paper delay element has been implanted with the help of D flip- flop.

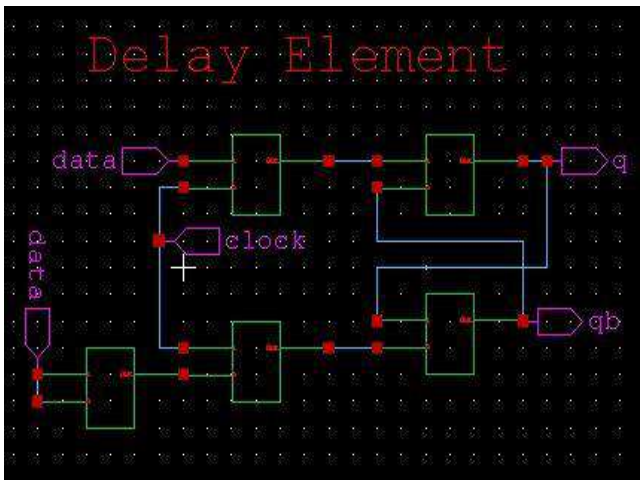

Figure: 2. Delay element using NAND gates

The above delay element schematic consists of 5 NAND gates with external clock signal is shown in Fig.2

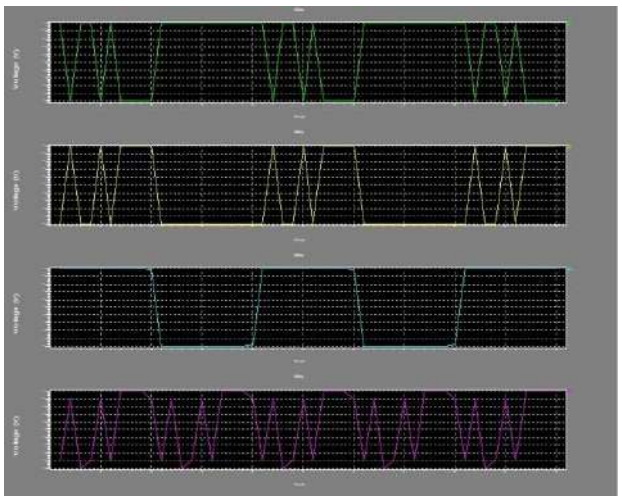

Figure: 3. Delay element D F/F output

The Fig. 3 shows the simulation results of delay element, If clock =1, data= 1 then q=1 and qb=0. It means whenever data is on the bus it need to drive to the output by the enabling the clock.

2. Multiplier & Summer:

After getting the data from the delay element it need to transfer the data to the multiplier. Multiplier is an element which is used to multiply the two operands and produce output in terms of product terms. To implement multiplier primitively need to construct 1.CMOS inverter 2. CMOS NAND gate 3. CMOS AND gate 4. CMOS NOR gate. 5. CMOS OR gate. 6. CMOSXOR gate. 7. Half adder. 8. Full adder. 9. FIR 2X2 multiplier 10.FIR 4X4 multiplier.

CMOS inverter shown in Fig.4 is constructed with one PMOS and one NMOS in series. In which both the gates of the transistor are connected together taken as a input terminal of the circuit. And both the drains are short together to drive the output. Which produce complement of the input signal across the output.

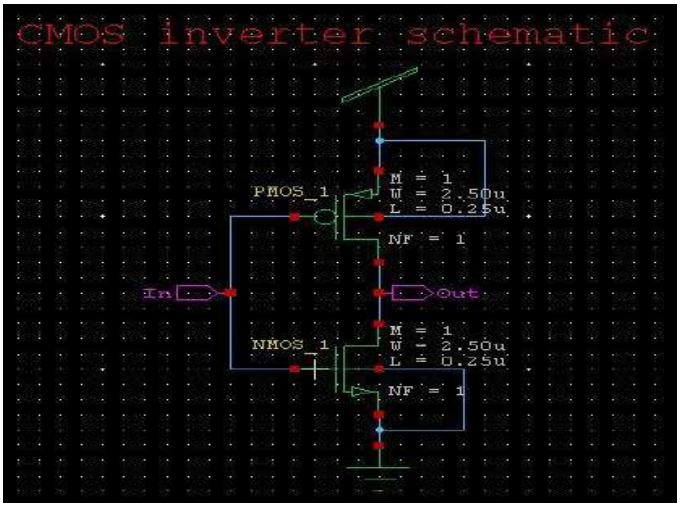

Figure: 4. CMOS Inverter schematic

CMOS NAND Gate:

In this module two NMOS act as pull-down circuit and two PMOS transistor act as pull up transistors are shown in Fig.5.

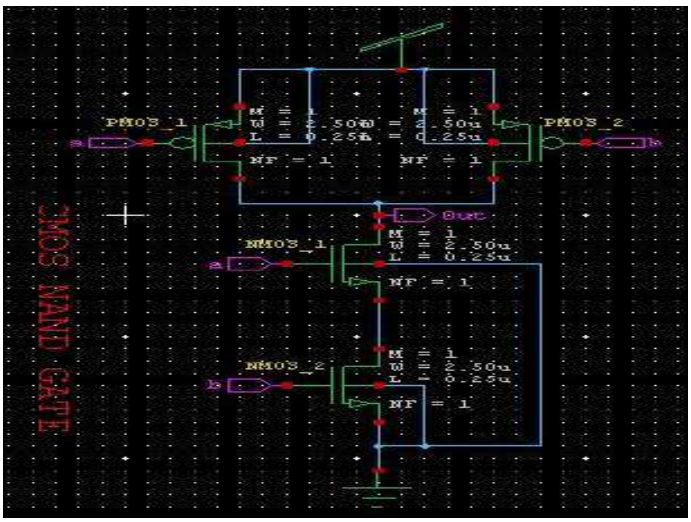

Figure: 5. CMOS NAND Gate schematic

CMOS AND Gate:

CMOS AND gate implemented with 3 PMOS transistors and 3 NMOS transistors is shown in Fig. 6. This is act as opposite to the NAND gate structure.

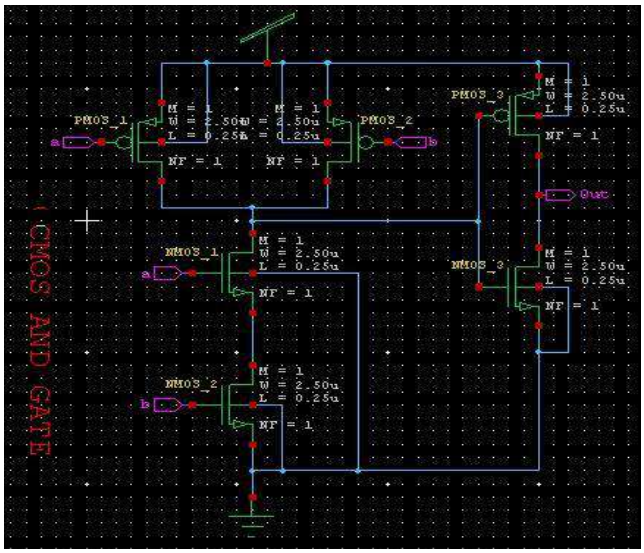

Figure: 6. CMOS AND schematic

CMOS NOR Gate:

The basic building blocks of this gate are constructed with 2 PMOS in series and 2 NMOS are in parallel is shown in below Fig.7.

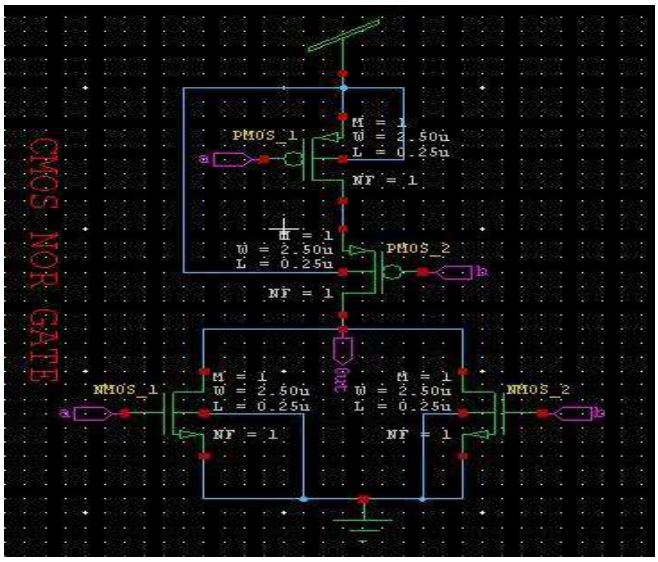

Figure: 7. CMOS NOR gate

CMOS OR Gate:

CMOS OR gate constructed with 3 PMOS transistors at pull-up mode, and 3 NMOS transistors in pull- down mode is shown in Fig.8.

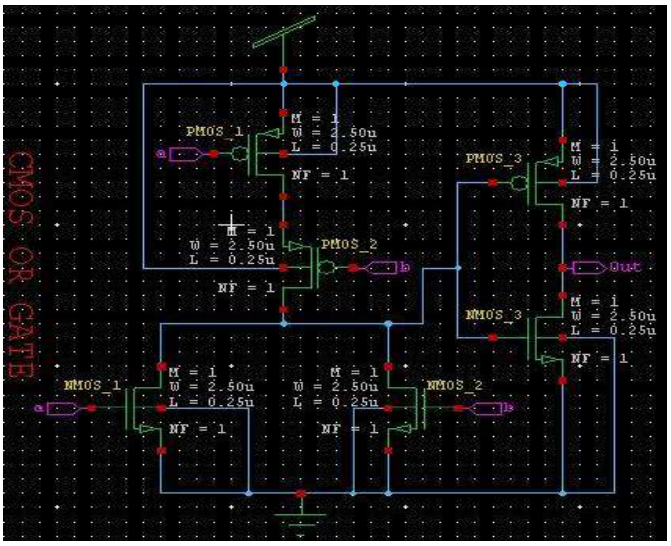

Figure: 8. CMOS OR gate

CMOS XOR Gate:

XOR gate is distributed gate which can be implemented by the help of 5 universal NAND gates are shown in Fig.9.

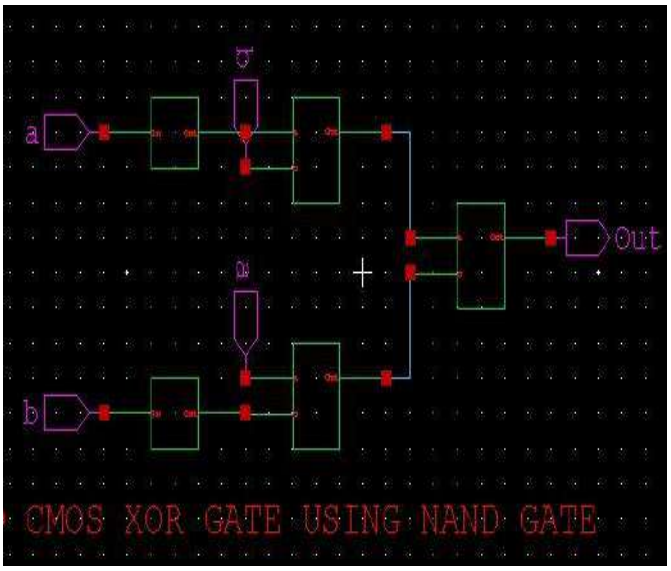

Figure: 9.CMOS XOR gate using NAND gate

Half adder:

CMOS half adder can be constructed with 1 XOR gate and 1 AND gate which produce SUM, Carry.

Full adder:

CMOS full adder can be constructed with 2 half adder with one OR gate. Which produce sum and carry is shown in Fig.10.

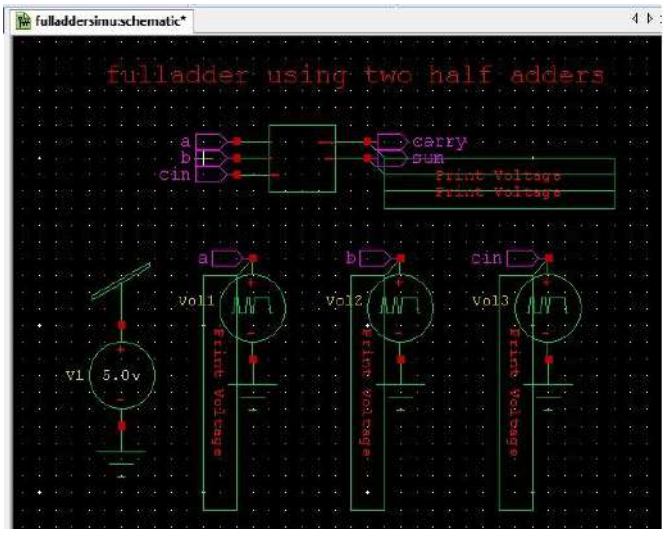

Figure: 10. Full adder schematic

FIR 2X2 Multiplier:

Finite impulse filter finally constructed with basic building blocks are shown in below Fig,11.

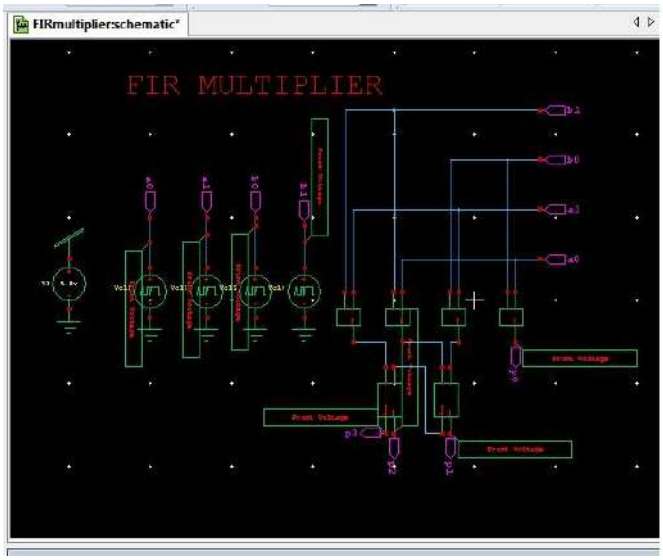

Figure :11. FIR 2X2 multiplier.

The 2X2R FIR[6] [7] bit multiplier module implemented using Four AND gates with 2 half adders or 2 Full adders.implemented with tanner tool.the 2X2 bit multiplier designen start by designed nad simulate individual gates saperately. After getting correct output wave forms create symbols for each block to create final multiplier.

The Truth table of 2X2 FIR multipiler is shown in below table 1.

Table: 1. Truth table 2X2 FIR multiplier.

Input					Output		
A1	A0	B1	B0	COUT	S2	S1	S0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0
0	0	1	0	0	0	0	0
0	0	1	1	0	0	0	0
0	1	0	0	0	0	0	0
0	1	0	1	0	0	0	1
0	1	1	0	0	0	1	0
0	1	1	1	0	0	1	1
1	0	0	0	0	0	0	0
1	0	0	1	0	0	1	0
1	0	1	0	0	1	0	0
1	0	1	1	0	1	1	0
1	1	0	0	0	0	0	0
1	1	0	1	0	0	1	1
1	1	1	0	0	1	1	0
1	1	1	1	1	0	0	1

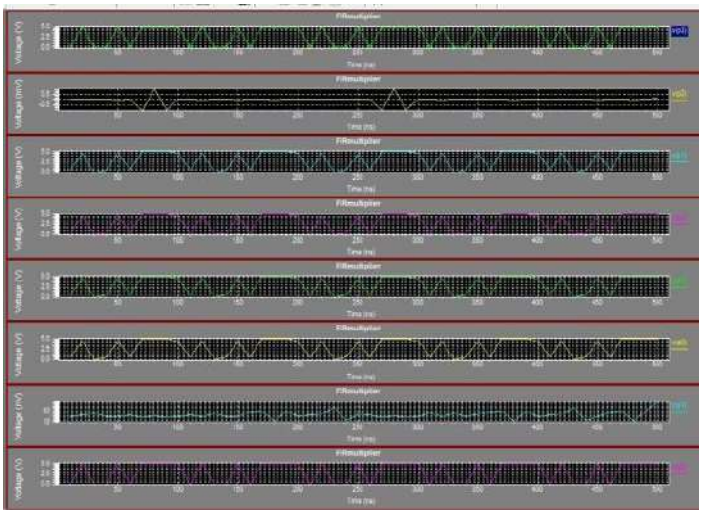

Figure : 12. Simulation results of 2X2 FIR multiplier

The simulation results of 2X2FIR [6] [7] multiplier shows which consist of 4 AND gates and 2 half adders for summing. The output produced in terms of S0, S1, S2, with additional carry.

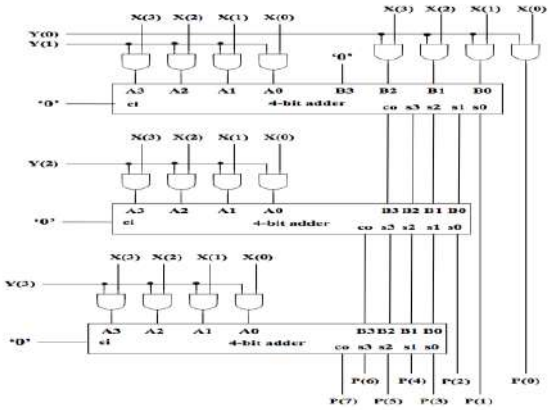

Figure : 13. 4X4 FIR Multiplier.[6] [7]

The simulated output graph of the four Bit FIR filter is demonstarated under figure , the ouput is checked with a sample of input taking all the inputs as '1' and getting output is 10000111.

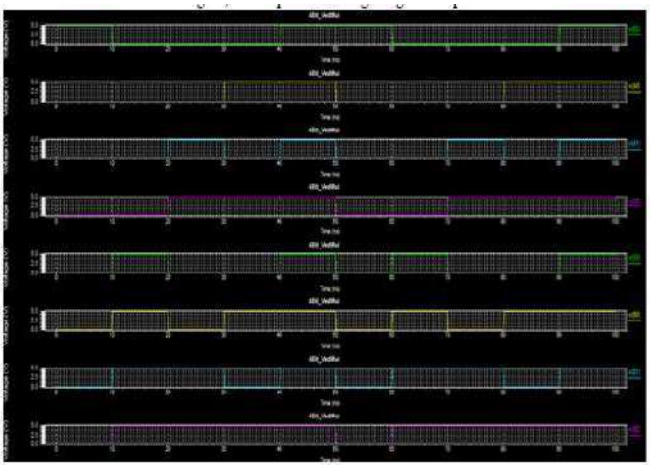

Figure 14: a. output wave form of FIR 4X4 filter

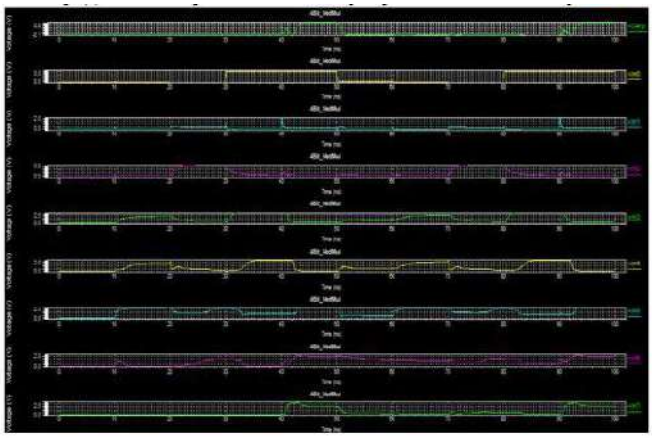

Figure 14: b. output wave form of FIR 4X4 filter

To obtain overall output (S7 S6 S5 S4 S3 S2 S1 S0), 4 2x2 bit Vedic multiplier and 3 4-bit Ripple-Carry. From the results, it is found that the proposed multiplier has the potential to reduce the delay.

POWER ANALYSIS:

The power analysis of FIR 4X4 Multiplier is shown in table 2.

Table: 2. Power analysis table

S.no	Module	Digital	Analog
1.	Adder	10.03mw	72uw
2.	Multiplier	103.67mw	
3.	Latch	1.56mw	
4.	No. transistor	34848 Lookup Tables .(LUT)	640

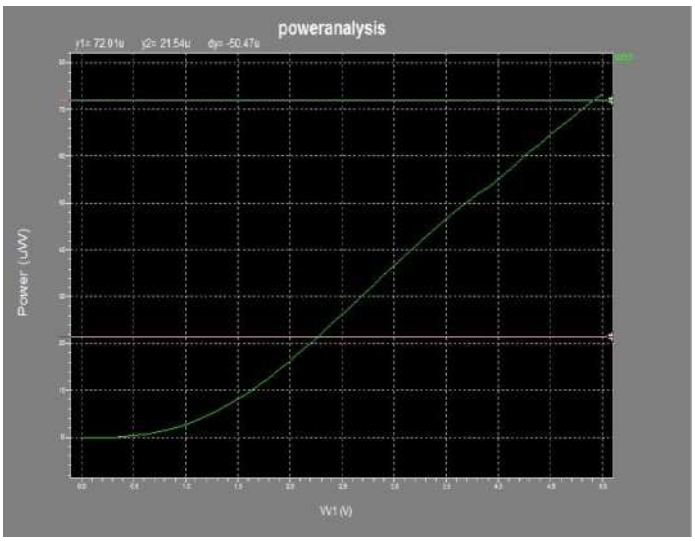

Figure : 15. power analysis FIR 4X4 multiplier

The proposed FIR filter consumes 72.01 microwatt. This proposed model conforms lowest power consumption of invidual modeuls is shown in Fig.15.

IV . CONCLUSION

A new method of CMOS FIR filter implementation has been discussed and by this method both power and area redued . the power consumption in proposed FIR filter around 72.01 microwatt and are required to around 640 transistors.this kind of work has been extended in electro encephalogram EEG signal very much.

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Investigation of magnetic behavior of a composite made of a soft and hard magnetic material

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Investigation of Magnetic Behavior of a Composite Made of a Soft and Hard Magnetic Material

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Abstract. Composite of a soft and hard magnetic material with compositional formula $(NiFe_2O_4)_{60} - (BaFe_{12}O_{19})_{40}$ was synthesized by sol-gel method. Thus synthesized composite was characterized structurally using X-ray diffraction and morphological studies were done by scanning electron microscopy (SEM). The XRD pattern obtained showed both the phases indicating the composite nature of material. Reitveld analysis of X-ray diffractogram confirmed hexagonal structure with *P63mm* space group for Barium hexaferrite (BFO) and cubic structure with *Fd-3m:2* space group for Nickle ferrite (NFO). The SEM micrograph indicates grains of nano size about 100-300nm, while EDAX studies show that there are no other impurities than the expected elements in required proportions. To study the magnetic and electric properties of this material magnetization and impedance was measured with variation of magnetic field and frequency at room temperature. From the magnetization data we observed that the material is exhibiting magnetically single phase. Dielectric studies show a continuous decrease in dielectric constant with increasing frequency.

INTRODUCTION

Nickel ferrite ($NiFe_2O_4$) is one of the most important spinal ferrites. It is a fully inverse spinal structure showing ferromagnetism originating from magnetic moments of anti-parallel spins between Fe^{3+} ions at tetrahedral sites and Ni^{2+} ions at octahedral sites. $NiFe_2O_4$ has a wide range of applications in many fields including biomedical applications, magnetic refrigeration, in magnetic liquids, as a microwave absorber [1-3].

Whereas, $BaFe_{12}O_{19}$ ferrites having magneto plumbite structure commonly called as hexagonal structure are the best ferrites [4]. The unit cell of $BaFe_{12}O_{19}$ is a combination of two structural blocks (R and S) aligned in c-axis direction. In this unit cell, S-block has a spinal structure with closed packed 'O' ions and Fe ions on its tetrahedral and octahedral sites. The R-block is formed of hexagonally closed-packed 'O' ions and one each 'Ba' and 'Fe' ions occupy the interstitial, tetrahedral, octahedral and bipyramidal sites, respectively. Presently, technologies like RADAR, microwave, communication, etc are changing drastically and there is a need of materials which must have a high saturation magnetization, high core activity, high magnetic anisotropy, excellent chemical stability, high natural resonant frequency and good capability of absorbing the unwanted electromagnetic signal to meet the changes and all these properties stated above are observed to be possessed by $BaFe_{12}O_{19}$ [5].

Further, a composite of soft-hard magnetic materials would be useful in various applications due to their enhanced properties. The spring exchange coupling between the soft and hard magnetic phases depends on the various factors, which significantly influence magnetization, coercivity, magnetic energy product and microwave absorption properties of the composite powders.

Therefore, a $(NiFe_2O_4)_{60} - (BaFe_{12}O_{19})_{40}$ composite have been synthesised by sol gel method and the results of structural, magnetic and electric studies of this material are presented here.

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EXPERIMENTAL

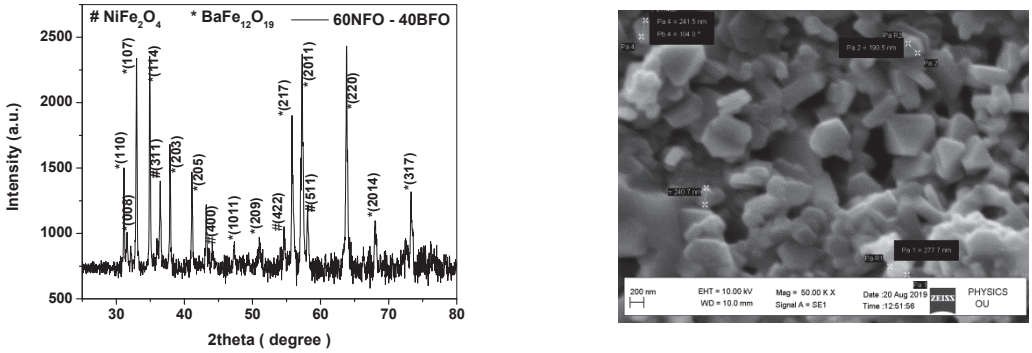
$(NiFe_2O_4)_{60} - (BaFe_{12}O_{19})_{40}$ composite was synthesized using sol- gel method. In this process, stoichiometric amounts of Ba $(NO_3)_2$, Ni $(NO_3)_2.6H_2O$, Fe $(NO_3)_3.9H_2O$, were mixed in a beaker and heated on a magnetic stirrer after neutralizing it by addition of ammonia solution and converting all metal nitrates into citrates. This reaction mixture was added with a gelating agent (ethelyne glycol) and the gel obtained after slow heating was further dried on the hot plate. A black coloured fluffy powder was formed on burning the sample. Thus obtained powder was ground finely and calcined at 900 ^{0}C for 4hrs. After synthesizing NFO and BFO powders separately by above process, they were weighed according to composition $(NiFe_2o_4)_{60} - (BaFe_{12}O_{19})_{40}$ (referred as 60NFO-40BFO) and made into pellets. These pellets were sintered at 1100 ^{0}C for 2 hours to obtain final samples.

The XRD pattern was obtained by X-ray diffraction (XRD) technique, while SEM micrographs were taken using Scanning Electron Microscope. The magnetization measurements were done using vibrating sample magnetometer and dielectric studies were undertaken using impedance analyser.

RESULTS AND DISCUSSIONS

Structural Details

The XRD spectrum of the sample $(NiFe_2O_4)_{60} - (BaFe_{12}O_{19})_{40}$ exhibited diffraction peaks corresponding to both $NiFe_2O_4$ and $BaFe_{12}O_{19}$ and is shown in Fig. 1(a). The observed peaks were indexed with hexagonal structure with p63/mmc space group for Barium hexaferrite and cubic structure with fd-3m:2 space group for Nickle ferrite phase.



(a) (b)

FIGURE 1. **(a)** XRD pattern and (b) SEM image of $(NiFe_2O_4)_{60} - (BaFe_{12}O_{19})_{40}$ composite at 1100 ^{0}C

Morphological Studies

SEM and EDAX measurements were done for the composite material. The micrograph shown in Fig.1(b) indicates grains of size 100-300nm. And EDAX data shows required composition without any detectable impurities. It can be seen from figure that the two phases are well distributed. In this soft $(NiFe_2O_4)$ are light colored and hard $(BaFe_{12}O_{19})$ are dark colored.

Dielectric Studies

To study the electrical properties of the composite prepared dielectric measurements were undertaken with varying frequencies in the range 50Hz to 5 MHz for $(NiFe_2o_4)_{60} - (BaFe_{12}O_{19})_{40}$ composite. The observed behavior is shown in Fig. 2(a). It can be seen from the figure that dielectric constant and impedance values are decreasing with increasing frequency. This dielectric behavior is expected for ferrites and arises due to space charge polarization which is because of the presence of higher conductivity phases (grains) in the insulating matrix (grain boundaries) of a dielectric, causing localized accumulation of charge under the influence of an electric field [5-6].

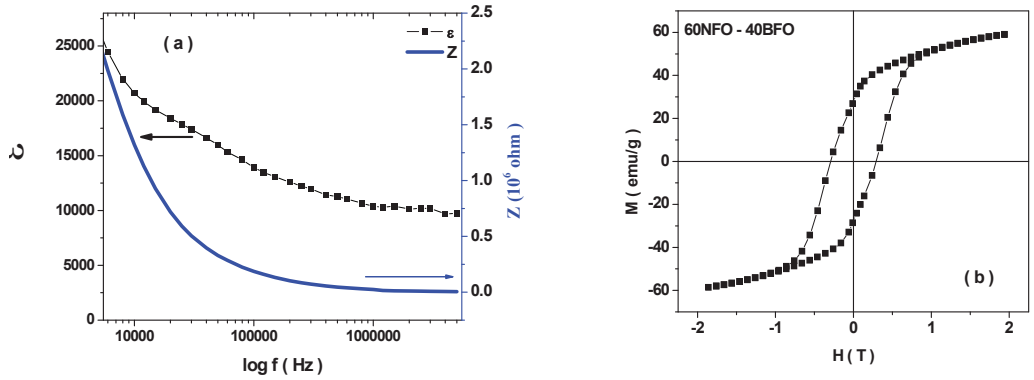


FIGURE 2. (a)The variation of dielectric constant and Impedance (b) M-H curve of $(NiFe_2O_4)_{60} – (BaFe_{12}O_{19})_{40}$ composite.

Magnetic Properties

The magnetic properties of materials were investigated by VSM. The magnetization versus magnetic field plot is shown in Fig. 2(b). It is well known that $NiFe_2O_4$ is a soft-magnetic material with coercivity (H_c) zero as the magnetic hysteresis loop of $NiFe_2O_4$ passes through the origin of the coordinates. The $BaFe_{12}O_{19}$ is a hard magnetic material with large coercivity (0.44 T) and saturation magnetization (M_s) is also very large (57.96 emu/g) [7-11]. Similarly, hysteresis loop was obtained for $(NiFe_2O_4)_{60} – (BaFe_{12}O_{19})_{40}$ composite which is indicating hard-magnetic material. The magnetic parameters are found to be M_s=55.7emu/g, M_r= 27.85 emu/g and H_c = 0.29 T. The composite is observed to show crystallographically two phases but magnetically a good single phase due to exchange spring coupled behavior with high saturation magnetization (M_s) as well as high (H_c) coercivity [12].

CONCLUSIONS

$(NiFe_2O_4)_{60} – (BaFe_{12}O_{19})_{40}$ composite was synthesized by sol-gel method and nano sized composite was obtained**.** The soft –hard composite exhibited excellent exchange spring behavior with high saturation magnetization as well a high coercivity values. The enhanced electric and magnetic parameters in the composite material make it useful for various applications and more so in microwave absorption devices.

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Microwave assisted synthesis of gold nanoparticles with *Phyla nodiflora (L.) Greene* leaves extract and its studies of catalytic reduction of organic pollutants

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ABSTRACT

The synthesis of gold nanoparticles (Au NPs) has drawn attention over the past few years owing to their optical and physico-chemical properties. In this work, synthesis of Au NPs using *Phyla nodiflora (L.) Greene* leaf extract was mediated using microwave irradiation. Gold nanoparticles is used for catalytic reduction of organic pollutants. The AuNPs are prepared by dissolving $HAuCl_4$ and aqueous leaf extract of ornamental plant phyla nodiflora Greene and it is confirmed by different analytical techniques like UV-visible, FTIR, DLS, XRD and TEM. Under the optimal synthetic conditions, the average diameter and zeta potential of AuNPs synthesized were 10±2 nm and -24.0 mV respectively. Phytochemicals present in the extract help to reduce Au^{+3} to Au^0 and act as a stabilizer in the synthesis of AuNPs. Afterwards, the catalytic activity of AuNPs was studied in $NaBH_4$assisted reduction of p-nitrophenol (4-NP), congo red (CR) and methylene blue (MB). The concentrations of *Phyla nodiflora (L.) Greene* and $HAuCl_4$, and duration of microwave irradiation were optimized for the better yield of AuNPsAuNPs synthesized with *Phyla nodiflora (L.) Greene* leaf extract could be an excellent catalyst candidate for 4-NP, CR and MB in chemical industries.

Keywords: *Nanoparticles, Microwave irradiation, UV –Visible studies.*

Microwave Assisted Synthesis of Gold Nanoparticles with *Phyla nodiflora (L.) Greene* leaves extract and its Studies of Catalytic Reduction of Organic Pollutants.

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Abstract

The synthesis of gold nanoparticles (AuNPs) has drawn attention over the past few years owing to their optical and physico-chemical properties. In this work, AuNPs were synthesized using *Phyla nodiflora (L.)* leaf extract by microwave irradiation method. This leaf extract act as reducing and stabilizing agent. The concentrations of *Phyla nodiflora (L.) Greene* leaf extract, $HAuCl_4$ and duration of microwave irradiation were optimized for the better yield of AuNPs. The AuNPs formation was confirmed by different analytical techniques like UV-vis spectrophotometry(UV), Fourier Transform Infrared Spectroscopy (FTIR), Dynamic Light Scattering (DLS), X-Ray Diffraction (XRD) and Transmission Electronic Microscopy (TEM). Under the optimal synthetic conditions, the average diameter and zeta potential of AuNPs synthesized were 10±2 nm and -24.0 mV respectively. Phytochemicals present in the extract help to reduce Au^{+3} to Au^0 and act as a stabilizer in the synthesis of AuNPs. Afterwards, the catalytic activity of AuNPs was studied in $NaBH_4$ assisted reduction of p-nitrophenol (4-NP), Congo Red (CR) and Methylene Blue (MB). Thus, AuNPs synthesized with leaf extract could be an excellent catalyst for 4-NP, CR and MB in chemical industries.

Keywords: Microwave radiation; Phyla nodiflora (L.) Greene; catalytic reduction; P-Nitro Phenol; Methylene Blue and Congo Red;

1. Introduction

The organic dyes and nitro aromatic compounds are widely used tocolor or dye materials within the pharmaceutical, agriculture, textile, paper, leather and plastic industries [1-3]. On the other hand, these organic dyes and aromatic nitro compounds are the key contributors for polluting surface waters and on-lands, because they have been discharged ceaselessly from these industries through their effluents. Environmental effects associated by these effluents will be connected with the toxic effects, bioaccumulation and pose dangerous effects like diarrhea, skin irritation dermatitis, conjunctivitis and painful colic if absorb orally [4-6]. It is very important task to scientists, in view of environmental concerns and health issues, to develop global standards for pollutant safety which inspired

the event of well-organized processes for purifying aqueous toxins. Various conventional methods such as adsorption, electrode deposition, filtration, chemical precipitation, photo catalysis and ion exchange have been tried for the removal of pollutants from aquatic media [7-10]. However, these methods are ineffective and result in generation of novel compounds which require further treatments. Nano catalysis as the modern method for the reduction of effluents from the aquatic media is in considerable attention [11]. The reduction of pollutants in the presence of greenand biocompatible nanocatalyst is the straight forward method. The previously reported metal and metal oxide nanoparticles were used as catalyst on the reduction of industrial effluents [12, 13]. Among them, gold nanoparticles have shown excellent catalytic activity due to AuNPs size and shape dependent optical, electronic, spectroscopic properties and higher stability. AuNPs are reported to have many applications in the bio sensing, biomedical, drug delivery and catalysis [14-16]. AuNPs in general synthesis can be prepared by several methods such as photochemical, chemical, electrochemical, laser ablation and radiolysis [17]. The reported methods for the synthesis of AuNPs make use of strong reducing agents, expensive, time taking processes and extreme temperatures. The green chemistry method of AuNPs synthesis avoids use of strong chemicals against conventional methods. The green chemistry approach has many advantages such as cost effectiveness, biocompatibility, simplicity and less time [18, 19].Thence, in the present work, the aqueous extract of leaves found from *Phyla nodiflora (L.) Greene* was studied for the synthesis of gold nanoparticles. *Phyla nodiflora (L.) Greene* is an important traditional medicinal plant of a *verbenaceae* family which contains diverse of phyto-constituents. This plant is used in traditional system to cure knee joint pain, liver tonic, skin disorders, dieresis, pneumonia and urinary disorder [20-22]. Hence, present investigation for the first time is used to explore the potential of aqueous leaves extract of *Phyla nodiflora (L.) Greene*. These leaves extract act as reducing and capping agents for the synthesis of AuNPs. The synthesized AuNPs were characterized by UV-Visible, FTIR, XRD and TEM. The synthesized AuNPs were applied for the reduction of 4-NP, MB and CR molecules

1.1. Materials and methods

1.2 Materials

Analytical grade $HAuCl_4$ was purchased from Sigma-Aldrich. All chemicals and reagents were purchased from Merck (Mumbai, India) and SD Fine-Chem Limited (Mumbai, India).

1.3 Preparation of *Phyla nodiflora (L.) Greene* extract

The Leaves of *Phyla nodiflora (L.) Greene* was collected from our university (Mahatma Gandhi University, Nalgonda) premises, cleaned, dried and powdered. This powder (1 gr) was mixed in 100 ml of double distilled water and stirred at 60^0C for 30 min. The solution was filtered with whatman filter paper and the filtrate is kept in refrigerator to use further.

1.4 Synthesis of AuNPs

$HAuCl_4$ solution (1 mL, 1mM) was mixed with 3 ml of the aqueous leaf extract. This reaction mixture was irradiated in a microwave oven for 3 min at 600 W. The resulting solution color changed from light yellow to red color indicating the formation of AuNPs.

1.5 Measurements

The absorption spectra were recorded on an UV-Visible spectrophotometer at room temperature (shimadzu UV-

3600). The FTIR spectra were recorded on an IR Prestige-21 spectrometer (Shimadzu). XRD pattern was recorded by Rigaku Miniflex method with Cukα (λ=1.5418 °A) radiation. The Zeta potential was obtained by Dynamic light scattering (UK, Malvern instrument Ltd). Size and morphology was determined by TEM using JEOL 2000 FX-II.

1.6 Catalytic reduction of MB, CR and 4-NP

The catalytic activity of the synthesized AuNPs for the reduction of MB, CR and 4-NP in the presence of $NaBH_4$ is as follows: MB solution (2 mL, 10 mM) was mixed with $NaBH_4$ (1.5 mL, 0.1M) and solution was made up to 10 mL using DD water. 3 mL of this reaction mixture is taken in a cuvette and 0.1 mL of AuNPs was added [13] and same procedure was followed for the reduction of CR. To test the catalytic activity of AuNPs for reduction of 4-NP, 4-NP (1.7 mL, 0.2 mM) was mixed with $NaBH_4$ (1.0 mL, 0.015 M) and followed by addition of AuNPs (1 mL). Absorbance of each mixture was recorded at regular time intervals by using UV-Visible spectrophotometer.

3. Results and discussion

3.1 UV-Visible study

The extract of the leaves was mixed with $HAuCl_4$ solution and subjected to microwave irradiation. The solution's color changed from light yellow to red color which indicates the formation of AuNPs monitored by UV-Visible spectrophotometer. The resultant solution showed Surface Plasmon Resonance peak at 525 nm which can be assigned to AuNPs. The synthetic conditions were optimized by varying the concentration of extract, $HAuCl_4$ and microwave time. Fig.1a shows the absorption spectra of different concentrations (0.1-1%) of extract and remaining parameters were constant. It could be observed that intensity of absorption peak increases with increase in the concentration of extract. Hence it can be inferred that formation of AuNPs increased with the concentration of the extract. The effect of $HAuCl_4$ in the formation of AuNPs was evaluated by changing the concentrations of $HAuCl_4$ are shown in Fig.1b. It reveals that the absorbance value increased gradually with increase in $HAuCl_4$ concentration from 0.1- 2mM. The effect of microwave irradiation time was also studied for the formation of AuNPs as shown in Fig.1c. As the time of the microwave irradiationincreased (0.5min-3min) at a voltage of 500mV, the formation AuNPs also increased [13].

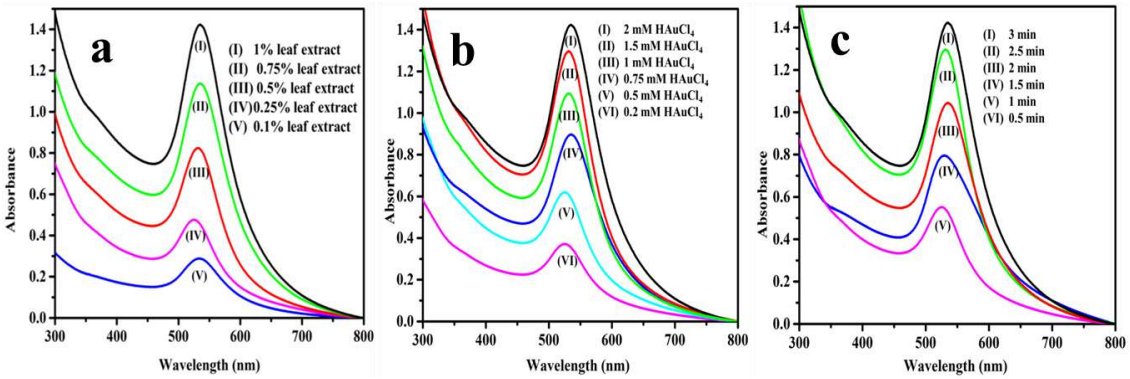

Fig.1 The UV–Vis absorption spectra of Au nanoparticles synthesized by at (a) different concentrations of *phyla nodiflora Greene* leaf extract, (b) different concentrations of $HAuCl_4$, (c) different microwave irradiation time

3.2 FTIR study

FTIR studies were performed to identify which functional groups of extract are involved in the reduction and stabilization of synthesized AuNPs. Fig.2 shows the FTIR spectra of the extract before and after capping with AuNPs. The FTIR spectrum of extract peaks are 3380, 2925, 1595, 1440, 1319, 1230 and 1032cm^{-1}. While, the FTIR spectrum ofAuNPs capped extractpeaks are 3338, 2931, 1739, 1589, 1410, 1319, 1230 and 1032cm^{-1}.The bands at 3380,2925, 1739, 1595, 1440 and 1319 cm^{-1} which correspond to stretching vibration of O-H, asymmetric C-H stretch, carbonyl stretching (CH_3CO-), asymmetric stretch of carboxylate (-COO-), symmetric stretch of carboxylate (-COO^-) and acetyl groups respectively. In the FTIR spectrum of AuNPs, a shift in the peaks was observed from 3380 to 3338 cm^{-1}, 1595 to 1589 cm^{-1} and 1440 to 1410cm^{-1}, and a new peak appeared at 1739 cm^{-1} revealed that the binding of an hydroxyl and carboxylate groups with AuNPs inferred that hydroxyl and carboxyl groups are responsible for the synthesis and stabilization of AuNPs [23].

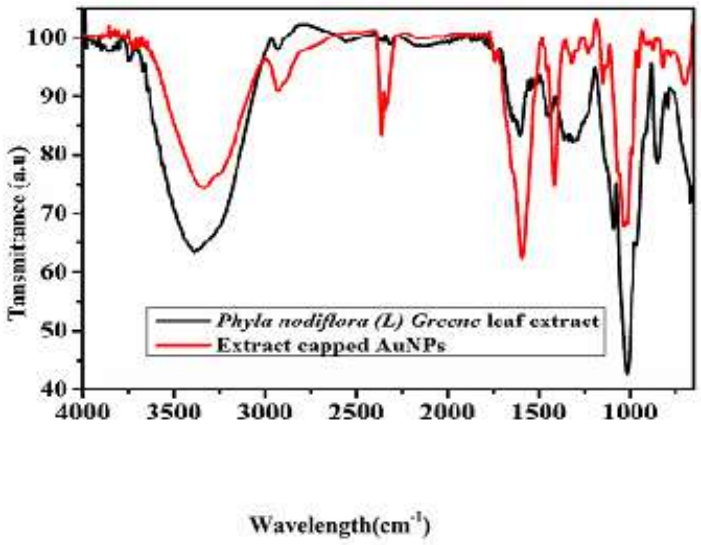

Fig.2 FTIR spectra of a pure *phylanodifloragreene* leaf extract and stabilised extract capped AuNPs.

3.3 XRD Studies

Fig.3 showed the XRD pattern of synthesized AuNPs, the characteristic reflection of the planes (111), (200), (220) and (311) at 2Ɵ values are 38.16, 44.14, 64.47 and 77.36, respectively. This indicated the Braggs reflection of face centred cubic structure of crystalline gold. These values are in good agreement with the previous reports (JCPDC No: 04-0784) for crystalline gold (ref). The crystalline size, calculated using with Scherer formula from XRD pattern using line width of the (111) peak, was obtained as 9.8 nm. The observation from the XRD studies is in good agreement with TEM Studies [24].

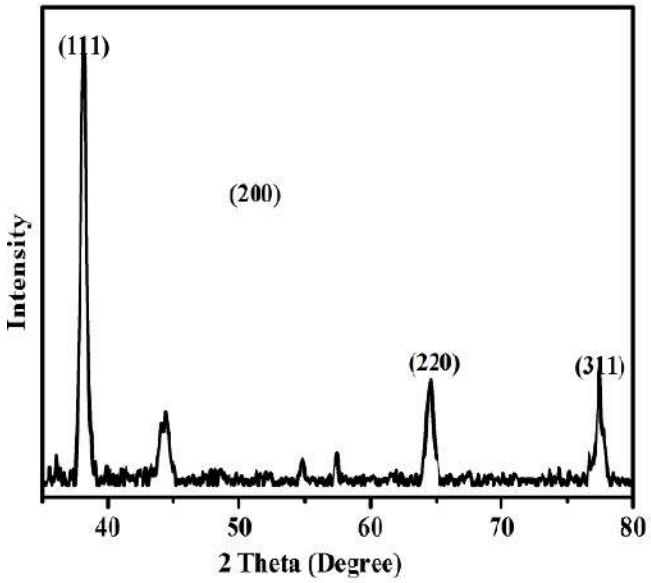

Fig .3XRD pattern ofsynthesizedAuNPs.

3.4 Catalytic activity

The catalytic activity of AuNPs in dispersed *Phyla nodiflora (L.) Greene* leaf extract was tested for the reduction of industrial effluents such as 4-NP, MB and CR in the presence of excess $NaBH_4$. UV-Vis spectrophotometer is used to study the catalytic activity of synthesized AuNPs.

3.5 Catalytic reduction of 4-NP

The UV-Vis spectra (Fig.6a) curve shows pure 4-NP absorption maxima at 318 nm. When $NaBH_4$ solution was added to 4-NP, a peak position was shifted from 318 nm to 400 nm, this is due to the formation of 4-Nitrophenolate ions. The change in intensity of peak position at 400 nm was employed to monitor the entire reduction process [25]. No change in the intensity of the peak was observed in the presence of $NaBH_4$ even after 4 hours of time. This indicate that $NaBH_4$ itself was not able to reduce 4-NP to 4-aminophenol. Then, synthesized AuNPs were added to 4-nitrophenolate mixture and the intensity of peak at 400 nm decreased with time was observed. Simultaneously, a new peak absorbance peak emerged at 297 nm, indicating the formation of 4-Amino phenol (Fig.6b). In this study, the concentration of $NaBH_4$ is much greater than the 4-NP concentration so that the reduction reaction would follow a pseudo first order kinetics. The rate constant was calculated from the slope of the linear graph between ln (A_t/A_0) versus time (Fig.6c), where $A_t$is the absorbance at time and A_0 is the absorbance at initial time and the rate constant was estimated to be 0.612 min^{-1}.

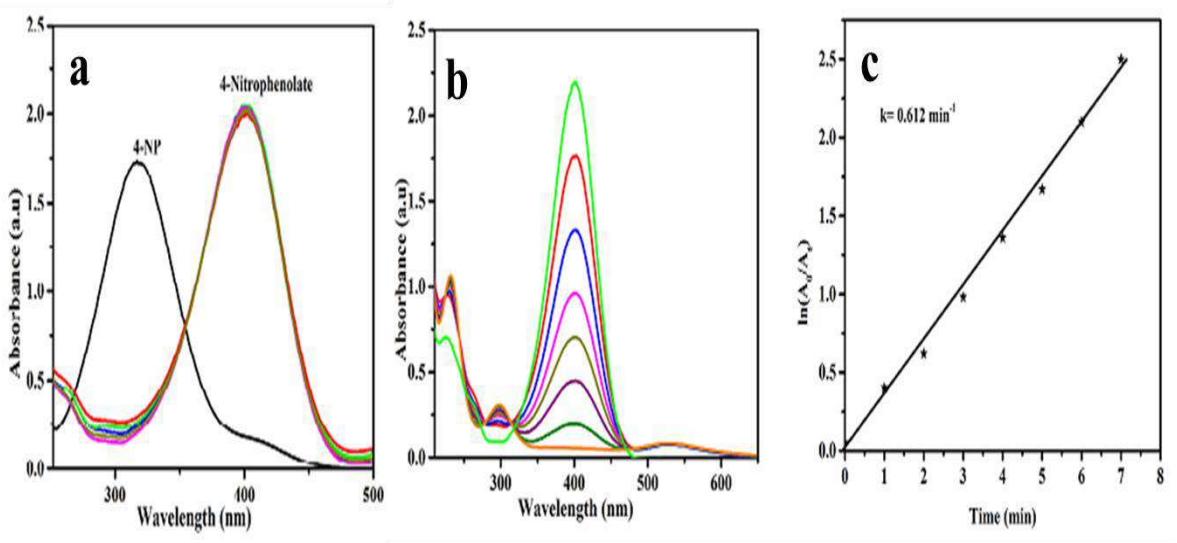

Fig.6 UV-Vis absorption spectra (a) 4-NP and 4-NPin the presence of $NaBH_4$ in the absence of AuNPs (b) catalytic reduction of 4-NP to 4-AP by $NaBH_4$ in the presence of AuNPs, (c) Plot of ln(A0/At) versus time for the reduction of 4-NP to AP

3.6 Catalytic reduction of CR

The UV-Visible spectra (Fig.7a) of CR in aqueous medium in the presence of $NaBH_4$ show two maximum absorptions bands at 493 and 350 nm which corresponds to the π-π* and n-π* transitions and assigned to the (-N=N-) [26]. It indicates that reduction of CR proceeded very slowly and no significant color change was observed even for one hour. Synthesized AuNPs were added to the reaction mixture of CR solution. The reduction reaction is completed within 5 min (Fig. 7b). Here, AuNPs act as electron relay, and electron transfer take place via AuNPs from BH_4^- (donor) to CR (accepter) molecule [12]. The reduction reaction is pseudo first order kinetic and the rate constant (k) was calculated from the kinetic graph (Fig. 7c)ln (A_t/A_o)=-kt.A_o is the initial concentration of CR and A_t is the concentration of at time t. The rate constant is found to be 0.012 sec^{-1}.

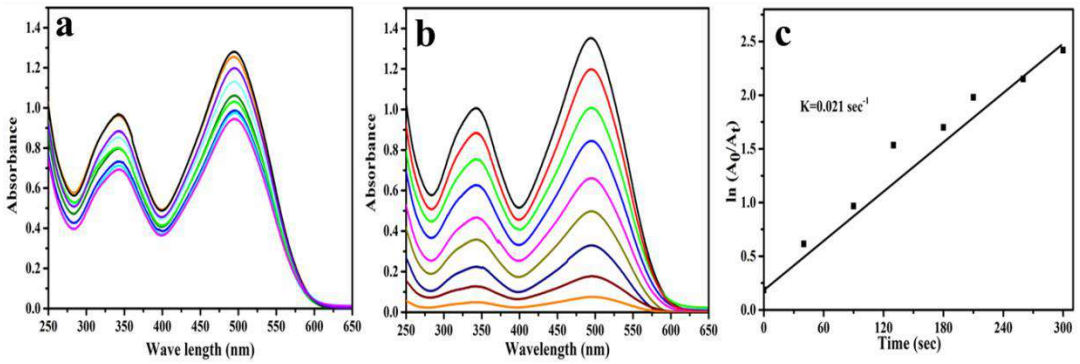

Fig.7UV-Vis absorption spectra (a)CR + $NaBH_4$ without the addition of AuNPs, (b)of CR and $NaBH_4$ mixture in the presence of AuNPs, (c) plot of ln(A_0/A_t) versus time for the reduction of CR

3.7 Catalytic reduction of MB

It has been showed that synthesized AuNPs has good catalytic activity for the reduction of 4-NP. This has promoted our idea in testing whether synthesized AuNPs also effectively used as a catalyst for the reduction of MB. In aqueous medium MB showed absorption major absorption peaks at 664 nm and 614 nm which corresponds to the π-π* and n-π* respectively. The Fig.8a shows the reduction of MB by $NaBH_4$ in the absence of AuNPs, no color change was observed visibly for a long time, kinetically slow and took several hours in the mere presence of the strong reducing agent ($NaBH_4$) as reported earlier. On the other hand, after addition of AuNPs to the mixture of MB and $NaBH_4$, the solution color completely disappeared with in 10 min and the absorption peaks of MB decreased gradually in the UV-Vis spectrum (Fig.8b). The linear correlation between $\ln(A_t/A_o)$ and reduction time, order of the reduction reaction was found to be pseudo first order reaction (Fig. 8c). The rate constant is calculated to be 0.0348sec-1.

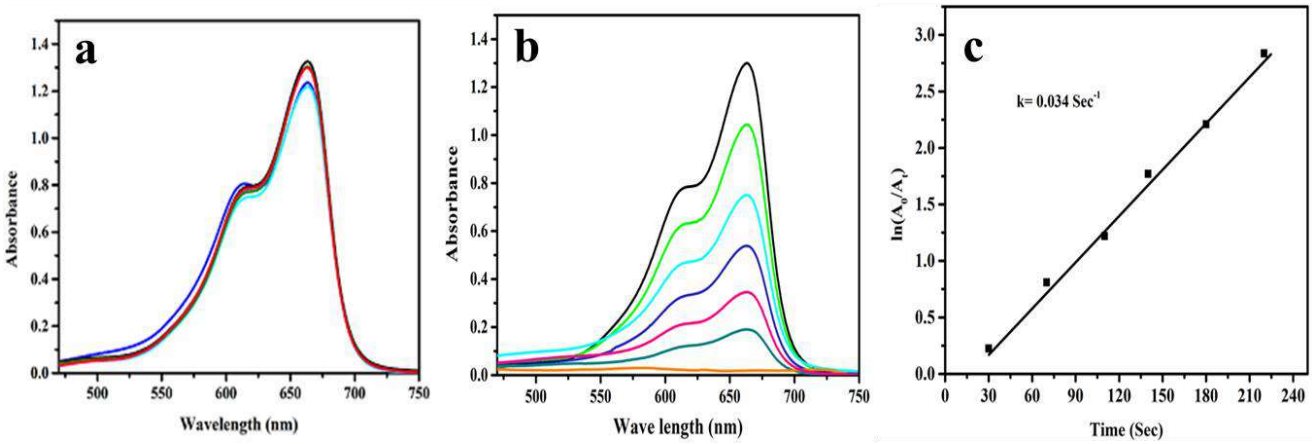

Fig.8UV-Vis absorption spectra (a) MB in the presence of $NaBH_4$ and absence of AuNPs, (b) reduction of MB to leuco methylene blue by $NaBH_4$ in the presence of AuNPs, (c) plot of $\ln(A_0/A_t)$ versus time for the reduction of MB.

Conclusion

The present investigation demonstrates microwave assisted synthesis of nanosized gold nanoparticles was successfully performed by employing the leaf extract of *Phyla nodiflora (L.) Greene*. The phyto-constituents present in the leaf extract act as both reducing and stabilizing agent. The synthesis of AuNPs were optimized by varying the parameters such as concentrations of extract, $HAuCl_4$ and microwave irradiation time with UV-Visible spectrometer. The functional groups present in the extract and AuNPs were analyzed by FTIR. The crystalline nature of AuNPs was confirmed by XRD and DLS studies show the stability of AuNPs. The size and shape of the AuNPs was found to be 10±2 nm and mostly spherical as confirmed by TEM analysis. The catalytic activity of the AuNPs was evaluated against reduction of 4-NP, CR and MB. These results provide a safe and versatile candidate for the reduction of organic pollutants.

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Operational Trans-Conductance Amplifier with Improved Characteristics for Active Filters

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Abstract

Active clear out plays an critical function in today's global of communication. A famous application uses an op-amp to build lively filter out circuits. A filter out circuit may be constructed the usage of passive components: resistors and capacitors, Low pass and excessive skip filter out structure have sizeable utility and the usage of CMOS Operational Trans-conductance amplifier gives capability to perform properly in Nano- meter variety as it has better manage over short channel impact and different scaling problem like gate leakage, sub-threshold conduction. The proposed clear out includes OTA. This filter out suggests low sensitivity to passive components, low element count and simplicity in design.

Design of operational trans-conductance amplifier (OTA) is the principle awareness for designing excessive skip and low pass filter out. The simplicity and linearity are the important capabilities of the OTA intended for any application. There are several in contrast to OTA's are used wherein this OTA is a easy OTA with low energy intake in (µwatt) and high gain (db). The OTA is considered by numerous constraints like open loop gain, Bandwidth, Slew Rate, CMRR and etc. The output of OTA with HLF completed in mentor photographs 0.25µm technology [2].

Keywords: *Basic Current Mirror, Differential Amplifier, Common Source Amplifier, Active Low Pass, Slew Rate, High Pass Filter, Gain, CMRR.*

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OPERATIONAL TRANS-CONDUCTANCE AMPLIFIER WITH IMPROVED CHARACTARISTICS FOR ACTIVE FILTERS

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Abstract:

Active clear out plays an critical function in today's global of communication. A famous application uses an op-amp to build lively filter out circuits. A filter out circuit may be constructed the usage of passive components: resistors and capacitors, Low pass and excessive skip filter out structure have sizeable utility and the usage of CMOS Operational Trans-conductance amplifier gives capability to perform properly in Nano-meter variety as it has better manage over short channel impact and different scaling problem like gate leakage, sub-threshold conduction. The proposed clear out includes OTA. This filter out suggests low sensitivity to passive components, low element count and simplicity in design.

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Keywords: basic current mirror, differential amplifier, common source amplifier, active low pass, slew rate, high pass filter, gain, CMRR.

I: INTRODUCTION

Analogue filters play a very giant position in electronic system. Low pass filter out passes signal with a frequency lower than a certain cut-off frequency and attenuates sign with frequencies higher than the cut-off frequency. The designing of filter using passive ladder filter out as a prototype for lively filters, together with operational trans-conductance amplifiers and capacitors (OTA-C), has emerge as very popular. The designing of OTA is done on Mentor graphics EDA software. It is suite of gear for the design of included circuits. There are particularly 3 tools S-edit, W-edit, and L-edit.

Design of the op amp, accompanied by means of High Pass, Low Pass filters are first carried out on Schematic to test its Simulation by means of software of SPICE device to generate waveforms. Another tool of Tanner EDA is L-Edit and it's miles an incorporated circuit Physical design device it lets in us to draw layout of a circuit and take a look at cross-section, carry out DRC (Design Rule Check) and generate a Netlist of your Layout so that we can perform LVS (Layout Versus Schematic) using a calibrate tool.[3]

II. Literature Survey

Today Power Consumption has become associate degree more and more vital issue in filter. Antecedently filters were designed exploitation Bipolar semiconductor device amplifiers that are a circuit that deliver low-gain, high power consumption and additional noise amplification of the input [3] [4]. Op – amp give a really effective mean of making low pass and high pass filter while not the requirement for electrical device. Low pass and high pass filter exploitation op-amp may be utilized in many areas power provides to the output of digital to analogue converters to get rid of alias signals and plenty of additional application. However because the advancement takes place in technological world Operational Trans-conductance electronic equipment attains some deserves over bipolar devices [5].

A bipolar device is "current Controlled Amplifier" and has just one input whereas op-amp has two inputs.

III. Design and computer simulations

Design of operational trans-conductance electronic equipment (OP-AMP) [1] with active filters is that the main focus of this paper for planning high pass and low pass filter. The simplicity and one-dimensionality are the essential options of the OP-AMP supposed for any application. The Schematic of OP-AMP is shown in Figure one. The Op-amp is taken into account by numerous constraints like open gain, Bandwidth, Slew Rate, Noise and etc. [4]. The performance Measures are mounted Due to Design parameters love Transistors size (W/L), Bias current and etc. during this paper we

tend to describe style of OP-AMP; this design is finished in Mentor graphic zero.25µm technology.The higher order filter will be designed to boost the frequency response and increase the sharpness of filter. They can be designed using different topologies like-cascade and passive ladder. The different types of filters like band pass, high pass and band reject filter can be realized using OTA and capacitor

III A. SCHEMATIC IMPLEMENTATION

The basic building blocks of Operational Trans-Conductance Amplifier are 1. Basic current mirror. 2. Differential amplifier 3. Common source amplifier.4.Low pass filter 5. High pass filter.

1. Current mirror is established to maintain current stability in whole circuit, it has MN1as source and MN2 as a mirror transistor and ammeter as a test point to measure mirror current, and which consumes less power because of its architecture nature.

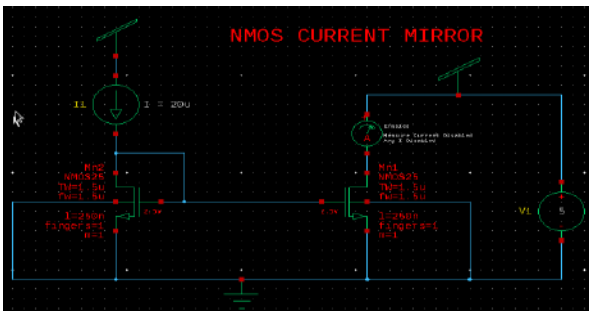

Fig: 1 current mirrors with 20µAms.

2. Differential amplifier

Basic building blocks of DS amplifier has MN3 as a Vin1,MN4 as aVin2, and Two MP1,MP2 are provided proper biasing for DS, Which amplifies the difference of the input stages.

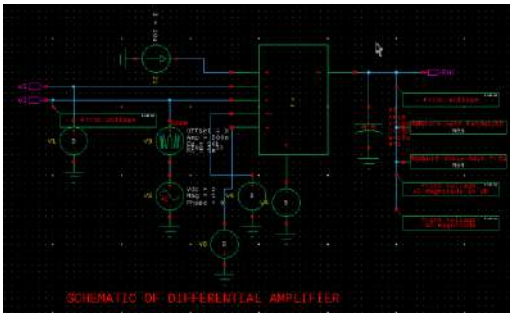

Fig: 2 Differential Amplifiers.

The below figures shows the simulation results of DS producing gain of 23.76dB with output voltage of15.35 volts

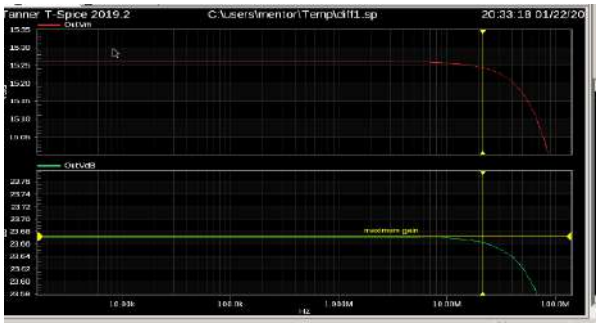

Fig: 3 Differential amplifier gains with phase.

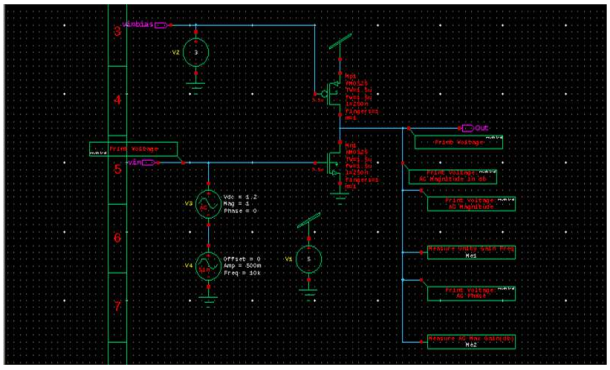

Fig: 4 common source amplifiers.

From the Schematic we can observe that two transistors are used i.e one PMOS and one NMOS transistor.

Two supply voltages are used one is 3v and other is 5v respectively. A sinusoidal AC signal is given with an offset of 0v

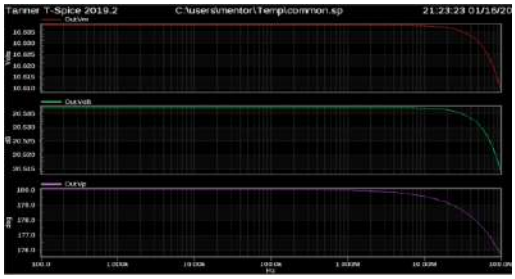

Fig: 5. Gain plot of common source amplifiers

From the output we can observe that the gain of Common Source amplifier is **20.63dB.**where V_{out} is **10.63v** and V_{in} is **0.53v.**

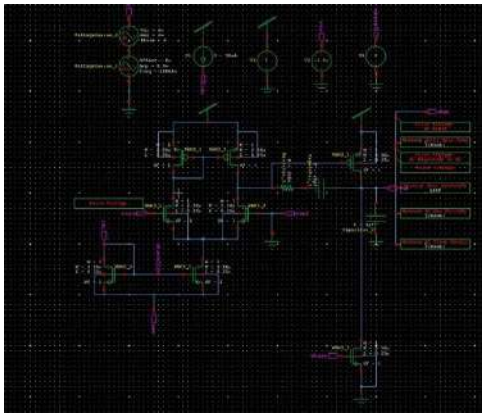

Fig6. OPERATIONAL AMPLIFIER

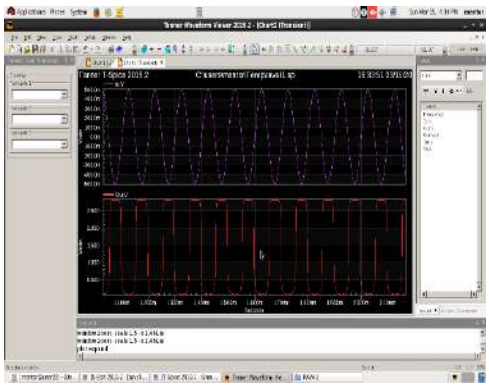

Fig 7: output and input response of op-amp

The above figure 7 shows the simulation results of op amp with input voltage of 500 millivolts produces 2.5 volts as aoutput.

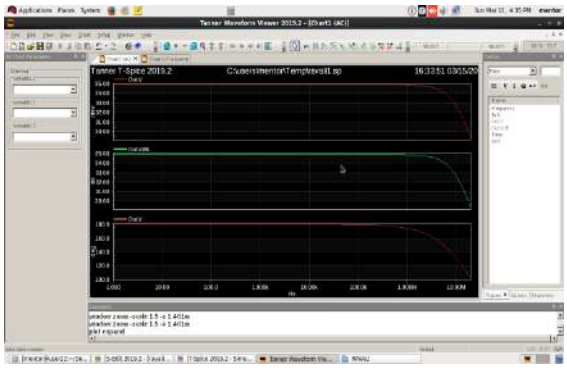

Fig 8: gain with phase plot of op amp

The above figure 8 shows the gain simulation results of operational amplifier with 35 db, with input voltage of 500 millivolts.

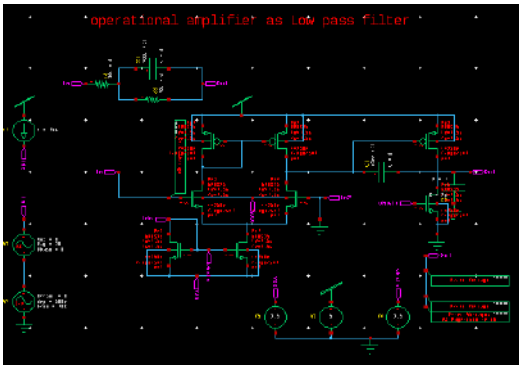

Fig 9: OP AMP with LPF schematic

The above figure9 shows Low pass filter schematic with100nf capacitance R1= 100 Kohms.

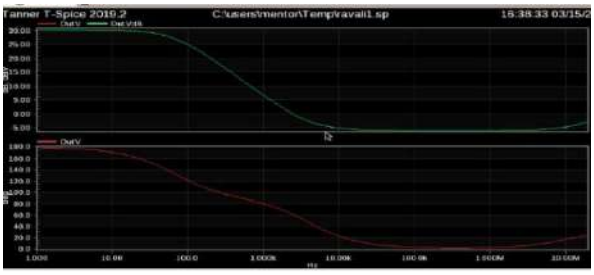

Fig10.LPF with gain plot

The above figure 10 shows low pass filter with lower cutoff frequency of 100 Hz.

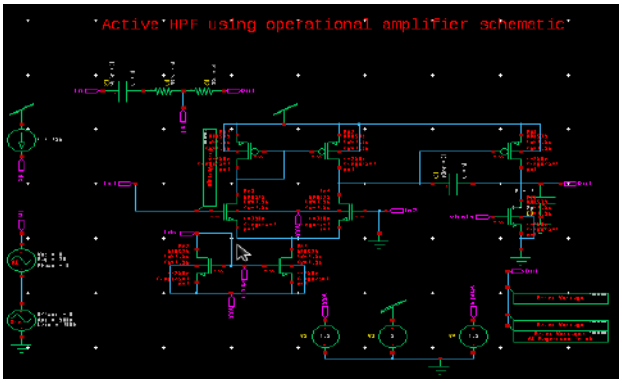

Fig 11. Op amp with HPF

The above shows schematic of HPF with feedback resistance of R15K, R1=1.5K ohms with input capacitance of 4.7nf.

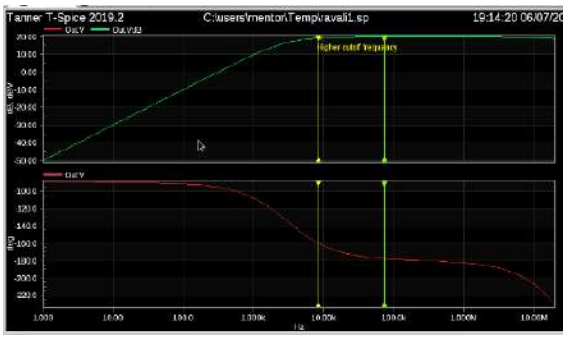

Fig 12: gain of HPF

The above figure shows simulation of gain plot with higher cutoff frequency of 10 KHz.

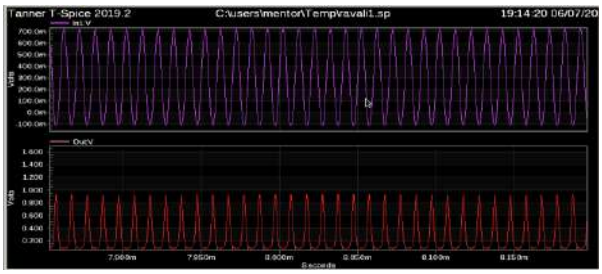

Fig 13:Output OF HPF.

The above figure shows output of HPF with V_{in} 700millivolts which produce V_{out} as 2.60Volts.

IV Design rules, layouts and Result

As the length between the source and drain is 250nm or channel length, [5] we are using 250nm Technology [6].

PMOS			
S.NO	FIELD COMPONENTS	LENGTH	WIDTH
1.	N-WELL	2.995	4.110
2.	SUBSTRATE	1.050	1.050
3.	P IMPLANT	2.005	2.065
4.	GATE	2.100	0.250
5.	METAL	1.140	0.545
6.	GROUND	4.170	0.645

Table 1: PMOS design rules.

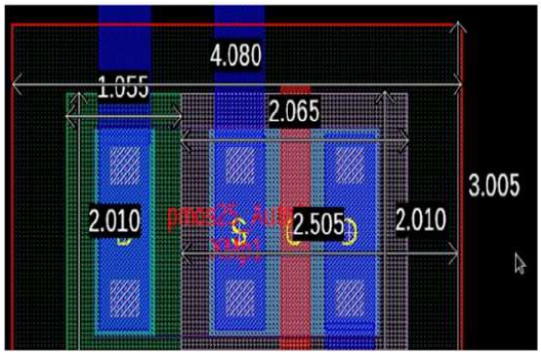

Fig: 14 Design rules for PMOS.

NMOS			
S.NO	FIELD COMPONENTS	LENGTH	WIDTH
1.	P-WELL	2.045	2.000
2.	SUBSTRATE	1.990	1.010
3.	N IMPLANT	1.550	1.495
4.	GATE	2.095	0.250
5.	METAL	3.710	0.625

Table 2: Design rules for NMOS.

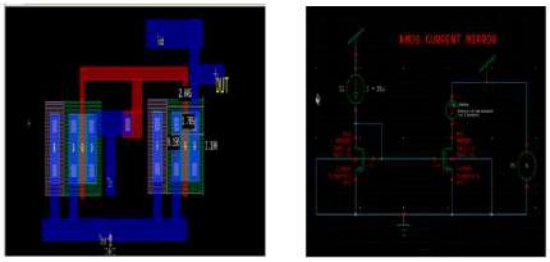

Fig: 15 layout of current mirror

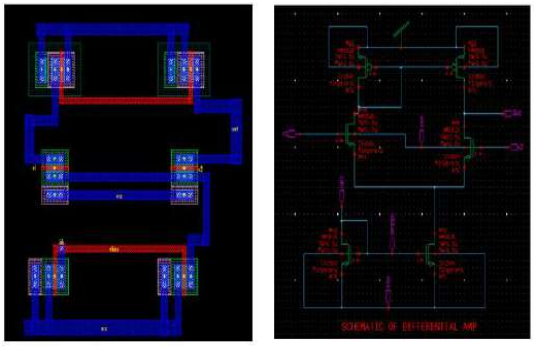

Fig16: Design rules for Differential amplifier.

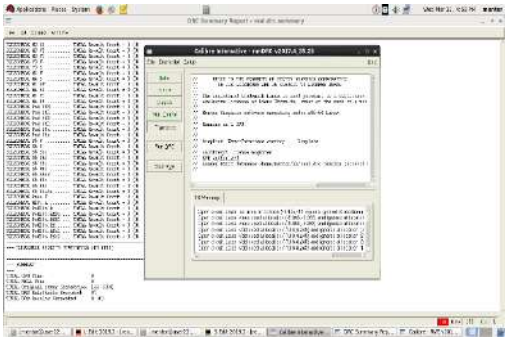

Fig 17: DRC report by calibrate tool

IV Calculations

1. Trans conductance Amplifier (gm):

The ratio of the change in current at the output terminal to the change in the voltage at the inputterminal of an active device.

$$gm = Ids/ Vgs$$

Where Vgs = 500milli, Ids = 1.5 milli
Gm= 0.003

2. SLEWRATE:

How fast vout can follow the input signal
SR= change in Vout to change in time interval

$SR = 2.2/ 0.2 \times 10^{-3}$
SR = 0.012 V/µs.

3. CMRR(COMMON MODE REJECTION RATIO):

CMRR has the ability of an op amp to reject any signal common to both inputs of the op amp

$$CMRR = R_1+R_F/R_1 \text{ X } Vin/Vout.$$

For LPF:

Where R_1=10 KΩ, R_f=100 KΩ, Vin = 0.5volts,
gain = 30db.
CMRR (LPF) = 1.964.
CMRR in db = 5db.

For HPF:

Where R_1=1.5KΩ, R_f=15KΩ, Vin = 0.7volts,
Vout = 2.60, gain = 20db.
CMRR (LPF) = 3.9.
CMRR in db = 11.8 db.

V Conclusion and to be Research

In this project we haveshown that how a low pass and high pass filter designed using operational trans-conductance amplifier can reduce the power consumption in the circuit. A filter circuit can be constructed using passive components: resistors and capacitors , Low pass and high pass filter structure have widespread application and using CMOS Operational Trans-conductance amplifier gives capability to perform well in Nano- meter range as it has better control over short channel effect and other scaling problem like gate leakage, sub-threshold conduction. The proposed filter consists of OTA .The other advantages of our design less power consumption, CMRR & Slew rate are better, gain is high. By this schematic we are proposing to design second order low pass and high pass filter devices and then go for power optimization.

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Spectrum Harvesting using Aggressive and Conservative Techniques in Cognitive Radio

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Abstract

In underlay cognitive radio, a secondary user transmits in the transmission band of a primary user without serious degradation in the performance of the primary user. It proposes a method of underlay cognitive radio where the secondary pair listens to the primary ARQ feedback to glean information about the primary channel. The secondary transmitter may also probe the channel by transmitting a packet and listening to the primary ARQ, thus getting additional information about the relative strength of the cross channel and primary channel. The method is entitled Spectrum Harvesting with ARQ Retransmission and Probing (SHARP). The probing is done only infrequently to minimize its impact on the primary throughput. Two varieties of spectrum sharing, named conservative and aggressive SHARP, are introduced. Both methods avoid introducing any outage in the primary; their difference is that conservative SHARP leaves the primary operations altogether unaffected, while aggressive SHARP may occasionally force the primary to use two instead of one transmission cycle for a packet, in order to harvest a better throughput for the secondary. The performance of the proposed system is analyzed and it is shown that the secondary throughput can be significantly improved via the proposed approach, possibly with a small loss of the primary throughput during the transmission as well as probing period.

Keywords: *Cognitive radio, Outage probability, Spectrum harvesting, probing, Conservative, Aggressive.*

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SPECTRUM HARVESTING USING AGGRESSIVE AND CONSERVATIVE TECHNIQUES IN COGNITIVE RADIO

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Keywords: Cognitive radio, Outage probability, Spectrum harvesting, probing, Conservative, Aggressive.

1. INTRODUCTION

There exists a rich literature on the coexistence of primary and secondary users in the same time/frequency band. It formulates the capacity problem under the power constraints at the receiver side in AWGN channel, which mimics the basic structure of the cognitive radio networks [1]. The cognitive users can exploit intermediate nodes to relay the information when there is no common white frequency band connecting the source and the destination. In three kinds of transmission schemes, namely underlay, overlay and interweave, are introduced.

In order to limit the interference on the primary, the secondary should judiciously adapt its power based on the Channel State Information (CSI) of the primary channel [3]. However, this is not straight forward as the secondary does not have direct access to the primary CSI. In a secondary system is allowed to transmit in the primary frequency band and the control feedback, such as ARQ, channel state, or power control information, from the primary serves as the side information to the secondary terminals. In addition, notices a hidden feedback loop between the primary and the secondary, and proposes a supervised transmission scheme to effectively share the primary spectrum.

It propose to use the ARQ feedback information to harvest excess mutual information in the channel when the primary has constant rate and power, while the channel gains fluctuate due to fading. The essence of the idea of is that whenever the primary receiver sends a NACK, other nodes in the system (potentially) become aware that a second transmission will be underway. [8]

2. LITERATURE SURVEY

In a secondary system is allowed to transmit in the same frequency band provided it ensures that the primary attains a specified target rate. To accomplish this goal, they proposed a scheme in which the secondary eavesdrops on the primary's ARQ to estimate the throughput loss of the primary user and uses this knowledge to tune the transmission policy accordingly and stay within its interference budget. The cognitive radio transmitter and receiver listen to the primary's ARQ, and by calculating the frequency of the primary's ARQ, can estimate the rate of the primary network.[2][4]

They have exploited the temporal redundancy in the channel introduced by primary and secondary retransmissions for interference cancellation. The authors in proposed a scenario wherein the secondary source is allowed to superimpose its transmissions over those of the primary source while guaranteeing a bounded performance loss for the primary network. This protection is achieved through monitoring the frequency spectrum of the primary's retransmission

attempts and by subsequent adaptation of the secondary's transmission.

The work in considers the same model as in a slow fading channel where the channel gain is assumed to be approximately constant over several transmission intervals, but is subject to change over much larger time scales. The authors proposed a method for acquiring partial information about the relative strengths of the cross channel and primary channel through listening to the primary ARQ feedback. The secondary transmitter also probed the channel by transmitting a packet and listening to the primary control signals (ACK/NACK), They titled their method Spectrum Harvesting with ARQ Retransmission and Probing (SHARP) and proposed two varieties of it; conservative and aggressive SHARP.[5] Conservative SHARP leaves the primary operations altogether unaffected, while aggressive SHARP may occasionally force the primary to use two instead of one transmission cycle for a packet, in order to harvest a better throughput for the secondary.

3. EXISTING SYSTEM

Traditionally, the frequency spectrum is licensed to users by government agencies in a rigid manner where the licensee has the exclusive right to access the allocated band. Therefore, licensees are protected from any interference all the time. From a practical standpoint, however, an unlicensed (secondary) user may share a frequency band with its licensed (primary) owner as long as the interference it incurs is not deemed harmful by the licensee. In a fading environment, a secondary user may take advantage of this fact by opportunistically transmitting with high power when its signal, as received by the licensed receiver, is deeply faded.[6][7] In this paper we investigate the capacity gains offered by this dynamic spectrum sharing approach when channels vary due to fading. In particular, we quantify the relation between the secondary channel capacity and the interference inflicted on the primary user. We further evaluate and compare the capacity under different fading distributions. Interestingly, our results indicate a significant gain in spectrum access in fading environments compared to the deterministic case.

4. PROPOSED SYSTEM

The secondary also has knowledge of his own transmissions, therefore it can know whether the ACK/NACK of the primary was under the secondary interference or not. The opportunity for activating the secondary depends on the relative strength of the direct channel g11 and the cross channel g21. We partition the g11-g21 plane into six regions, this partition is motivated by the amount of information that is available to the secondary, as will be shown in the sequel. We use the notations γp Δ = 2Rp − 1 and γs Δ = 2Rs − 1. The regions are characterized below and shown in Figure 1.

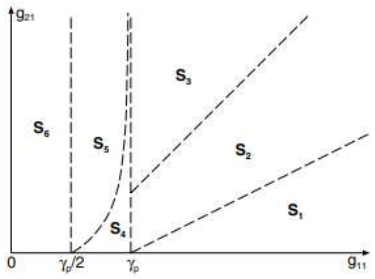

Fig.1: The six regions for the operation of SHARP cognitive radio.

1) The primary channel supports the rate in one transmission despite secondary interference. This is the best of all worlds, the condition under which this is true can be characterized by eq. (1)

$$\frac{P_p g_{11}}{P_s g_{21} + N} > \gamma_p \qquad \textbf{(1)}$$

Under this condition, the secondary should always transmit.

2) The primary channel can support its rate in one transmission if there is no interference, but needs two transmissions to succeed if there is interference eq.(2). This happens if:

$$\frac{\gamma_p}{2} < \frac{P_p g_{11}}{P_s g_{21} + N} < \gamma_p \qquad \textbf{(2)}$$

Under this condition, again the secondary can transmit at all times without pushing the primary into outage, but the throughput of the primary will be degraded.

3) The primary channel can support its rate in one transmission if there is no interference, but in the presence of interference it cannot succeed even with two transmissions:

4) The primary channel can support its rate in two (but not one) interference-free transmissions; it can also succeed in two transmissions as long as only one of the two transmissions is subject to interference eq .(3).

$$\frac{P_p g_{21}}{N} + \frac{P_p g_{11}}{P_s g_{21} + N} > \gamma_p \qquad \textbf{(3)}$$

$$\frac{\gamma_p}{2} < \frac{P_p g_{11}}{N} < \gamma_p$$

5) The primary channel can support its rate in two (but not one) interference-free transmissions; it cannot support its rate with any interference (not even on one of its two transmissions). eq (4)

$$\frac{P_p g_{11}}{N} + \frac{P_p g_{11}}{P_s g_{21} + N} < \gamma_p$$
$$\frac{P_p g_{11}}{N} > \frac{\gamma_p}{2} \quad \textbf{(4)}$$

Under this condition, the secondary should remain silent.

6) If g11 is sufficiently small, the primary is doomed to outage even with retransmission and even in the absence of any interference. This happens if eq.(5):

$$\frac{P_p g_{11}}{N} < \frac{\gamma_p}{2} \quad \textbf{(5)}$$

5. SYSTEM MODEL

5.1. Aggressive Algorithm:

Initially we transmit a new packet by primary and secondary should be silent. If Acknowledgement is positive, then primary transmits new package along with secondary. This region is called as S1. The region S2 allows one interference free transmission. The region S3 indicates the primary channel supports the rate in one interference-free transmissions, but in the presence of interference it is in outage even with retransmission. The region S4 supports primary transmission rate in two interference free transmissions, it also transmits when only one of transmissions subject to interference. The S5 region it supports primary the rate in two interference free transmissions. Cannot support with interference. Here in region S6, secondary is silent for two transmissions.

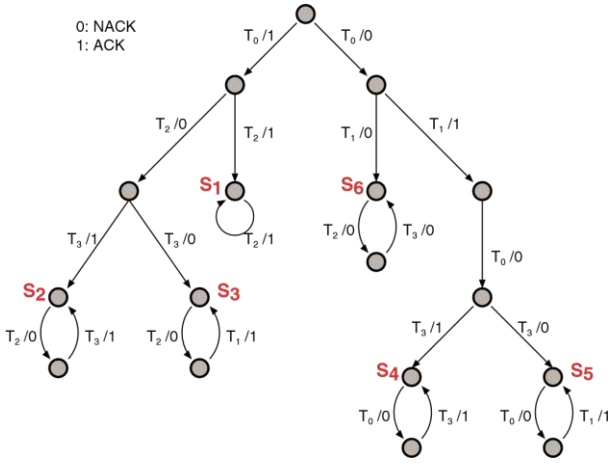

Fig.2: Algorithm for the aggressive SHARP

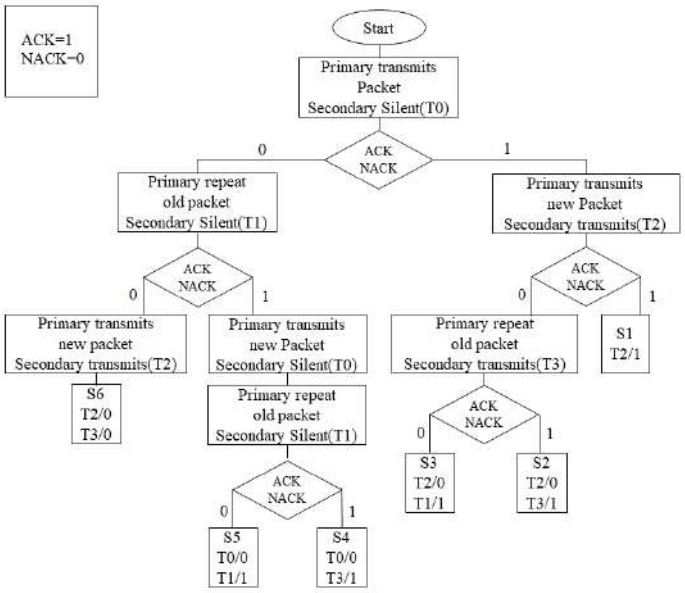

Fig.3: Flow Chart for the aggressive SHARP

5.2. Conservative Algorithm:

Initially we transmit a new packet by primary and secondary should be silent. If the Acknowledgement is positive, then primary transmits new package along with secondary. This region is called as S1. In previous S2, S3 secondary transmission will reduce primary throughput, so here we refrains from transmitting those regions. The region S4 supports primary transmission rate in two interference free transmissions, it also transmits when only one of transmission subjected to interference. The S5 region it supports primary the rate in two interference free transmissions. Cannot support with interference. Here in region S6 secondary is silent for two transmissions.

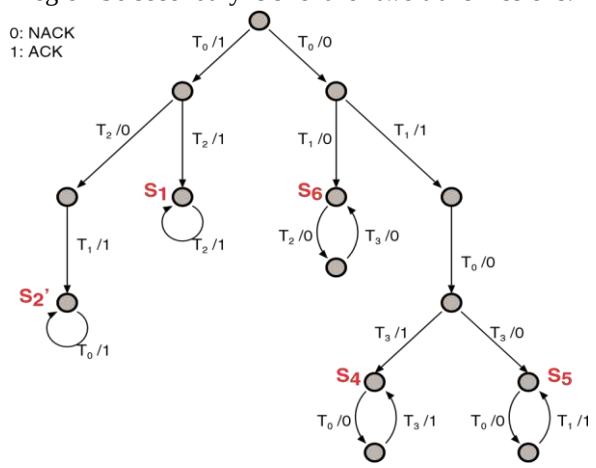

Fig.4: Algorithm for the conservative SHARP.

This requires the secondary to periodically re-do the channel probing and re-assess the situation. In particular, each of the tree branches in our flow chart leads to a loop, which composes of one or two transmission modes from T0, T1, T2, or T3 and the corresponding ARQ feedbacks (1 or 0). Remark 2.The main difference between them is that aggressive SHARP may occasionally slow down the primary by

forcing it to use two time slots instead of one. This is a slightly different form of degradation compared to, where the primary is slightly degraded in throughput because the secondary imposes on the primary (a small amount of) additional outage.

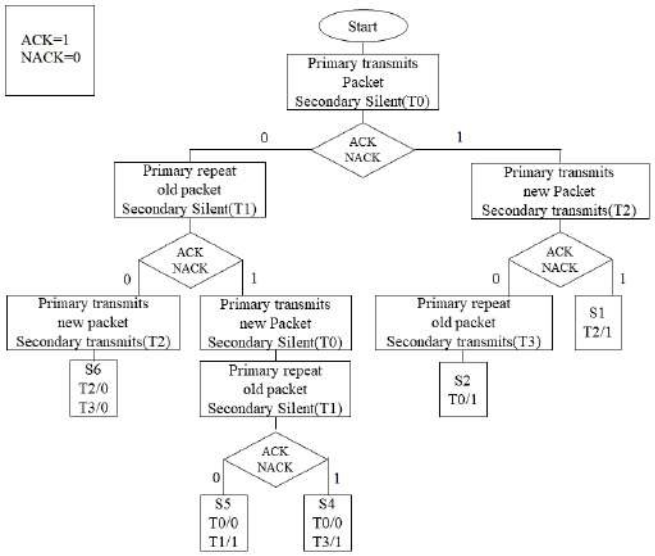

Fig.5: Flow Chart for the conservative SHARP

6. RESULTS

6.1. Channel Estimation by Probabilities of MIMO System:

The channel is estimated by using EM CE, MMSE and LS by finding the probabilities of primary and secondary users. From the fig.6, we can observe the throughput of all the parameters mentioned below at minimum are 0. The throughput of perfect CSI with MUD and with SUD at maximum EbNo(dB) are 3.1*105. The throughput of proposed system, when carrier rate (i=2,5) at maximum EbNo(dB) is also 3.1*105. The throughput of conventional EM CE at maximum EbNo(dB), when carrier rate (i=2) and carrier rate (i=5) are 2.8*105 and 2.6*105 respectively. The throughput of conventional MMSE with MUD and SUD at maximum EbNo(dB) are 2.8*105 and 2.5*105 respectively. From the fig.6, we can say that the throughputs of proposed systems, when carrier rate (i=2,5) graphs are approximately same with slight changes. We can say that carrier rate does not affect the throughputs too in channel estimating.

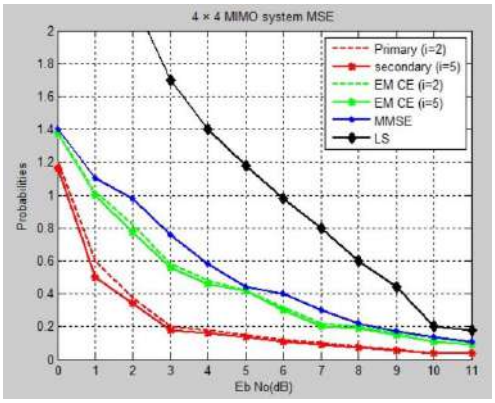

Fig.6: Probabilities of 4*4 MIMO system by MSE

- **EM CE:** Energy Maximization Channel Estimation
- **MMSE:** Minimum Mean Square Error
- **LS:** Least Square
- **i:** Carrier Rate

6.2. Channel Estimation by Throughput of MIMO System:

From the fig.7, we can observe the throughput of all the parameters mentioned below at minimum are 0. The throughput of perfect CSI with MUD and with SUD at maximum EbNo(dB) are 3.1*105. The throughput of proposed system, when carrier rate (i=2,5) at maximum EbNo(dB) is also 3.1*105. The throughput of conventional EM CE at maximum EbNo(dB), when carrier rate (i=2) and carrier rate (i=5) are 2.8*105 and 2.6*105 respectively. The throughput of conventional MMSE with MUD and SUD at maximum EbNo(dB) are 2.8*105 and 2.5*105 respectively. From the fig.7, we can say that the throughputs of proposed systems, when carrier rate (i=2,5) graphs are approximately same with slight changes. We can say that carrier rate does not affect the throughputs too in channel estimating.

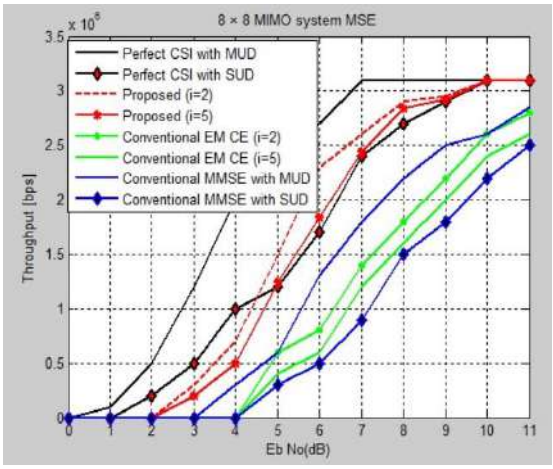

Fig.7: Throughput of 8*8 MIMO system by MSE

- **EM CE:** Energy Maximization Channel Estimation
- **MMSE:** Minimum Mean Square Error
- **CSI:** Channel State Information
- **MUD:** Multiple User Detection
- **SUD:** Single User Detection
- **i:** Carrier Rate

6.3. Comparison between the performance SHARP schemes:

Aggressive, Conservative and Legacy are the three types of SHARP schemes. Legacy is a traditional technique. We used Aggressive and Conservative technique in our project. Fig.8 shows the comparison between the performances of three SHARP schemes. We can observe that the throughputs of three schemes are starting at one point and reducing with the increase of P0/dB as shown in the Fig.8, At minimum throughput the P0/dB value of legacy is less when compared to Aggressive and Conservative. The throughput graphs of Aggressive and Conservative are same with slight changes. Hence, we can conclude that the performance of both the SHARP schemes i.e. Aggressive and Conservative are better than the legacy systems. The performance of Conservative is better when compared between them.

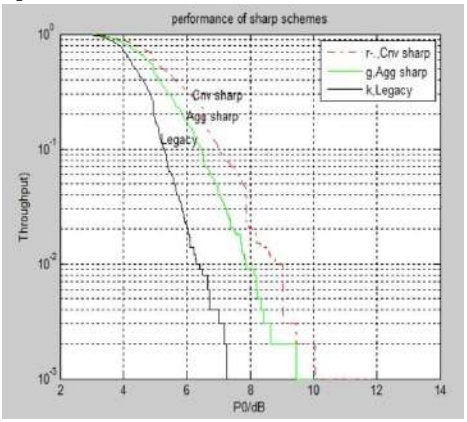

Fig.8: Comparison between the performances of SHARP schemes

7. CONCLUSION

This paper proposes a transmission scheme, namely SHARP, for the secondary user co-existing with an ARQ based primary system. Based on the ACK/NAK message from the primary only, the proposed SHARP schemes utilize several probing time slots to obtain a general picture about the primary channel condition, and operate accordingly with suitable transmission modes. The proposed schemes have been analysed and validated through Monte Carlo simulations. Furthermore, it was demonstrated that the aggressive SHARP achieves a better throughput than the conservative scheme with a small primary throughput loss. The conservative SHARP makes no negative effect on the primary system, and performs even better than the legacy system in terms of the primary user throughput. Both SHARP schemes do not generate unnecessary outage to the primary system, and are able to provide dramatic throughput gains to the secondary user without perfect CSI at the transmitter side.

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Souvenir

MSSA PS O-03

Design and Synthesis of Novel Bis-1,2,3-Triazol-1H-4-Yl-Substituted Aryl Benzimidazole2-Thiols, their Antimicrobial Evaluation and Molecular Docking Studies

Aparna Yeddla, Nirmala Gurrapu, Sharada Nalanda, Subhashini NJP and Sreekanth Sivan

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Email Id: aparna_bdm@rediffmail.com

A new series of triazole conjugates were prepared by click reaction of propargylated benzimidazole-2-thiols with corresponding azides. Simplistic 1,3-dipolar Huisgen coupling reactions of the respective aromatic azides with benzimidazole-2-thiol alkyne units gave the corresponding triazole conjugates. The structure of these conjugates have been established by various spectroscopic techniques including IR, NMR and mass spectra. Molecular docking studies were performed on these conjugates based on antibacterial activity studies which showed moderate to good activity

MSSA PS O-04

Fabrication of Novel Ag/AgBr/Cs2Nb$_4$O$_{11}$ Ternary Composite for Visible-Light Driven Photocatalysis

Perala Venkataswamy, Manasa Sunku*, Ravi Gundeboina, Radha Velchuri and Muga Vithal

Department of Chemistry, Osmania University, Hyderabad-500 007, Telangana, India
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In recent years, tuning the structural and photocatalytic properties of semiconductors with the support of noble metal (Ag, Au) nanoparticles through their well-known surface plasmon resonance (SPR) effect has gained much interest in the field of environmental applications. Herein, a new plasmonic Ag/AgBr/$Cs_2Nb_4O_{11}$ composite was successfully fabricated by applying a visible

Design and Synthesis of Novel Bis-1,2,3- Triazol-1H-4-yl-Substituted Aryl Benzimidazole-2-Thiols, their Antimicrobial evaluation and Molecular docking Studies

Aparna Yeddala,Nirmala Gurrapu,Sharada Nalanda,Subhashini NJP ,Sreekanth Sivan

Department of Chemistry,Osmania University,Hyderabad500007,Telangana,India.

Abstract

Twelve triazoles were prepared from benzimidazoles by propargylation followed by click reaction with substituted aromatic carboxylic acidsThe constitution of all the compounds has been established by their physical properties, elemental analysis and spectral analysis like ^{1}H NMR, ^{13C} NMR, IR and Mass spectra.All the compounds were screened for their antibacterial activity and molecular docking studies were performed.All the compounds exhibited moderate to good activity and binding studies showed good docking.

.

Keywords: benzimidazoles propargyl bromide,click reaction,antibacterial study, docking study

1. Introduction

Heterocyclic scoffolds bearing five-membered ring with three nitrogens are termed triazoles. Triazole, a heterocyclic core has gripped ample attention in scientific fraternity in search of new therapeutic molecules of medical importance. Triazoles are well known five membered heterocyclic moieties as most widely used class of antifungal drugs identified as azoles. Triazoles exist in isomeric forms as 1,2,3-triazole and 1,2,4 triazole which exhibit tautomerism. These tautomers are characterised by the position of nascent Hydrogen. Although 1,2,3triazoles are not naturally occuring ,they have explored new pathways in the area of drug discovery.Numerous 1,2,3 triazole moieties displayed appealing biological behavior like antibacterial, antiHIV activity and anti-allergic.
In addition to their usage as antimicrobial agents, they are used as synthetic intermediates ,polymers ,Supramolecules dyes and materials. There has been substantial concentration in 1,2,3-triazoles as light stabilizers and as optical brightening agents, photo stabilisers, corrosion inhibitors and fluorescent whiteners.

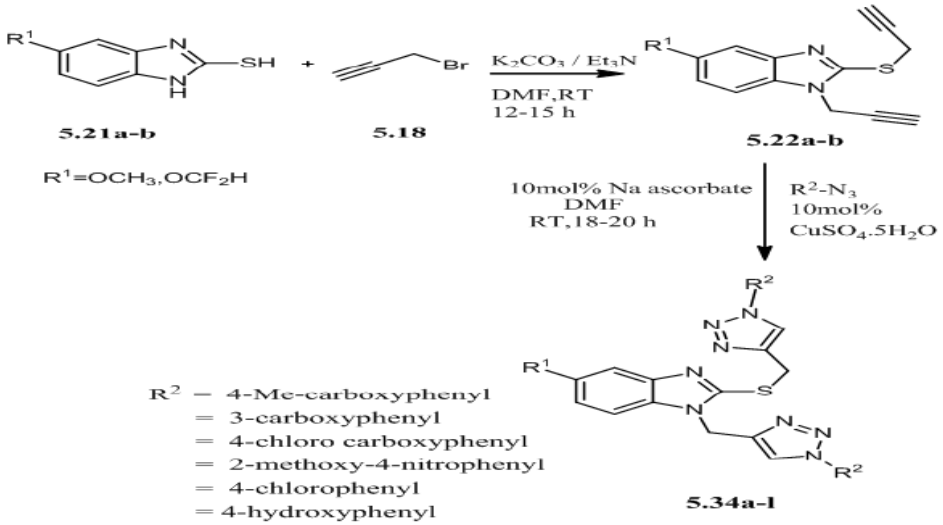
2.Materials

All chemicals and reagents were of analytical grade and purchased from Merck and SD Fine-Chem Limited .

3. Preparation of triazoles

The substituted 1H-benzo[d]imidazole-2-thiol derivatives have been synthesized starting from 4-hydroxyacetanilide and anisidine . The substituted 1H-benzo[d]imidazole-2-thiol derivatives are subjected to alkylation with propargyl bromide in presence of potassium carbonate in DMF at room temperature for 12-15 hrs to yield substituted 1-(prop-2-yn-1-yl)-2-(prop-2-yn-1-ylthio)-1H-benzo[d]imidazoles .These substituted 1-(prop-2-yn-1-yl)-2-(prop-2-yn-1-ylthio)-1H-benzo[d]imidazoles on reaction with different aromatic azides in presence of copper sulphate and sodium ascorbate in DMF for 18-20 hrs at room temperature.

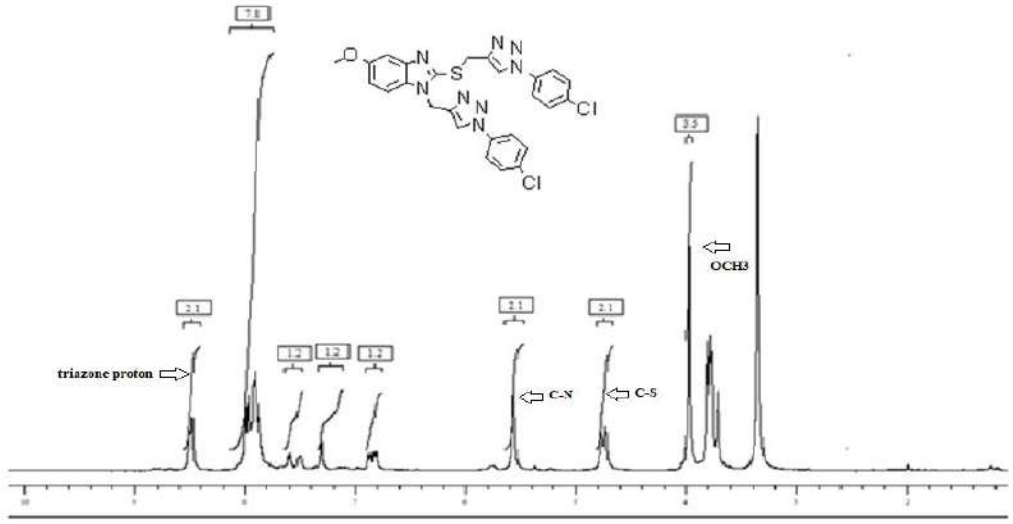
3.synthesis of imidazolones



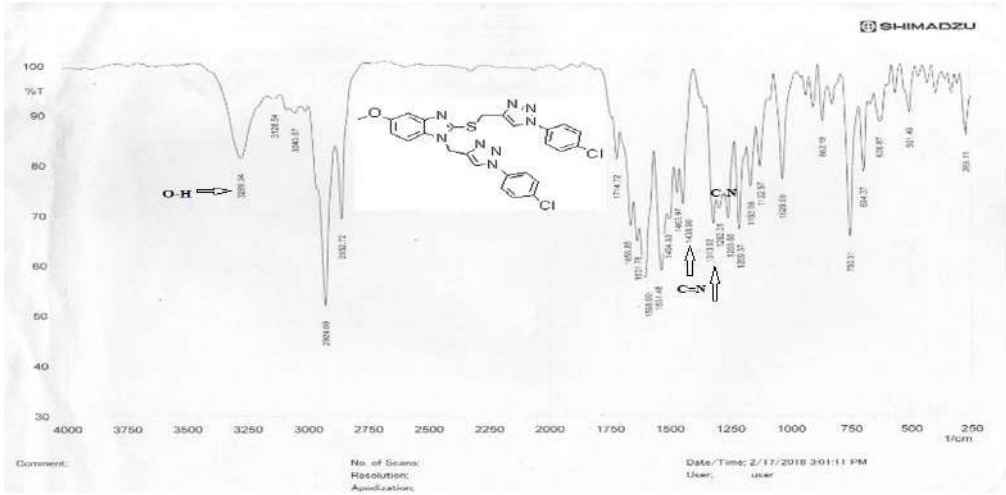
4.Results and discussion

The structures of imidazolones were confirmed based on ^{1}H NMR, ^{13}C NMR and Mass spectral data. In the IR Spectrum of the compound ,characteristic (C=N) absorption was observed at 1438.9cm^{-1} and (C-N) group absorption was observed at 1313.5 cm^{-1}.The stretching frequency at 3269.3cm^{-1} indicates absorption due to (O-H) group and absorption at 2850cm^{-1} and 2785cm^{-1} refers to aliphatic (C-H) group. The ^{1}H NMR spectrum(400 MHz, $CDCl_3$,of compound showed singlet at δ 3.89 corresponding to methoxy protons, singlet obtained at δ 4.85 corresponding to methylenic protons flanked between sulphur and triazole ring, a singlet appeared at δ 4.9 corresponding to methylenic protons flanked between nitrogen and triazole ring, a singlet obtained at δ 8.68 due to corresponding triazole protons. For ESI-MS mass spectrum of compound m/z 563$(M)^{+}$ appeared as base peak.

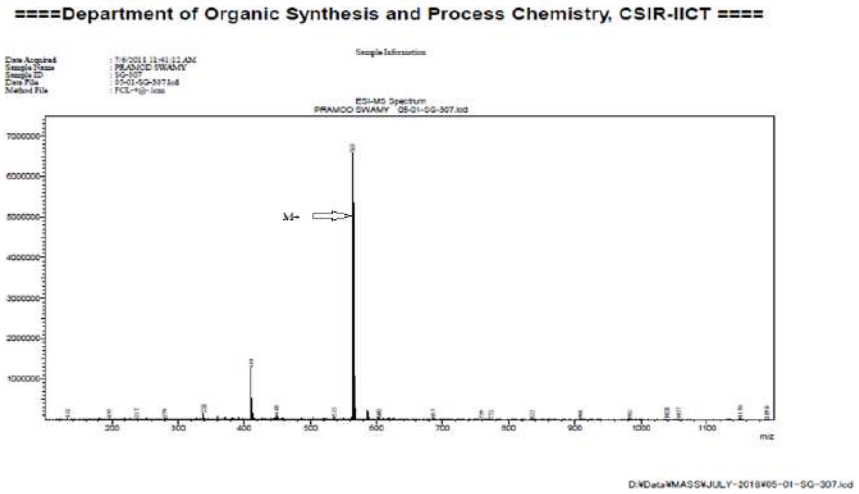
4.1 ^{1}HNMR Spectra



4.2 IR Spectra



4.3 Mass Spectrum

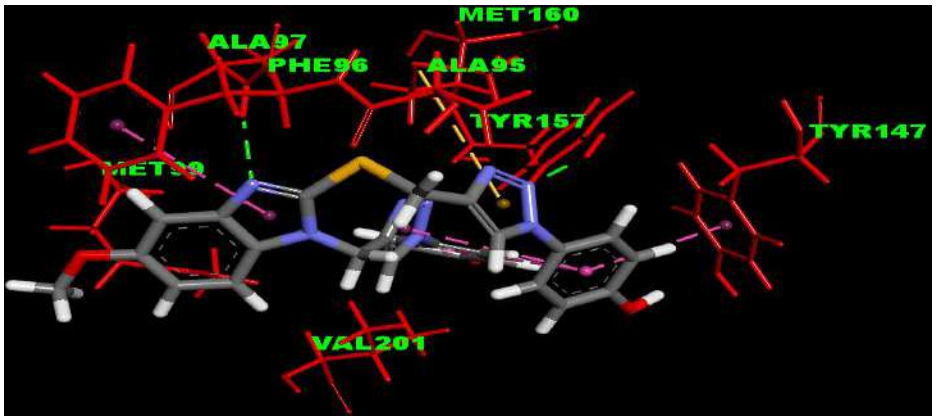


4.Antibacterial studies

	Plate 1 MIC against *Escherichia coli* in µg/ml	Plate 2 MIC against *Salmonella typhi* in µg/ml	Plate 3 MIC against *Pseudomonas aeruginosa* in µg/ml	Plate 4 MIC against *Staphylococcus aureus* in µg/ml
Ciprofloxacin	**121.41**	**105.69**	**158.28**	**117.25**
C1	**98.56**	**95.12**	--	**101.47**
C2	--	--	--	--
C3	--	--	--	--
C4	**103.56**	**121.08**	--	**85.63**
C5	--	--	--	--
C6	**105.67**	--	**102.57**	**123.57**
C7	**140.26**	**129.54**	--	**130.28**
C8	**68.74**	**61.78**	--	**58.78**
C9	**96.72**	**98.2**	**106.78**	**111.27**
C10	**99.04**	**93.25**	--	**112.85**
C11	**91.45**	**98.16**	**120.68**	**106.83**
C12	**118.46**	**121.67**	**146.59**	**83.47**

5.Molecular docking studies

Benzimidazole and triazole derivatives possess a wide range of pharmacological activities, and antimicrobial activity is one of the important activity among them.Few molecules embedded with 1,2,3 trizaole moiety have been reported as Enoyl-acyl carrier protein reductase (ENR). Enoyl-acyl carrier protein reductase (ENR) (EC 1.3.1.9), is a type II fatty acid synthesis (FAS) system that plays a key role in metabolism. Bacterial ENRs (Enoyl acyl carrier protein reductases) that are believed to be good specific targets for antibacterial agents development.



Conclusion

Imidazolones were already studied for their multifunctionality in heterocyclic chemistry.They were reported to exhibit various biological and pharmacological activites like CNS depressant, anticancer,anti-inflammatory etc., Inspired by the versatility, selectivity and high yields of click reactions that bridges gap between chemistry and biology, we have planned to synthesize novel 1,2,3-triazole as substructure of 2-mercaptobenzimidazole moiety.In the present work final compounds were designed to combine both benzimidazole-2-thiol and triazole moieties that were expected to have antimicrobial and anticancer activities.The most eye catching features of these compounds are, their utility in pharmaceutical industry and there is further scope for their exploration.
The focus on molecular docking is to computationally simulate molecular recognition process.The antimicrobial screening was carried by disc fusion method.Molecular docking was performed on Shrodinger suite 2010.

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High-Speed CMOS DD Amplifiers at Low Static Current Consumption

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Abstract

This paper presents design technique for linear operation range of CMOS differential difference amplifier with the primitive object of the Trans conductance on its Differential stage corner voltage (Vcn), is considered. The mathematical and comparative SPICE modelling results of typical CMOS Differential difference stage on the channel width of CMOS transistors at different static currents are presented using Mentor graphics 0.25micro Technology. The DDA can be reconfigured as an operational amplifier, this novel implementation brings significant reduction in static current to pace slew rate of the output voltage (SR).

Keywords—*CASCODE Current Mirror; Differential Difference Amplifier; Corner Voltage (Vcn); Unity Gain Buffer; Slew Rate.*

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Keywords—CASCODE current mirror;Differential difference amplifier; corner voltage (Vcn); unity gain buffer; slew rate.

I. INTRODUCTION

In recent years wireless communication systems dominated the telecommunication era. Consequently high speed, low power consumption, power delivered to the load and area efficient mixed/analog signal processing circuits became essential. Circuits like filters, mixers, registers and variable gain amplifiers are common parts in any communication system hardware. These blocks were realized using voltage op-amps. However, voltage op-amp based circuits cannot operate adequately for high frequency applications due to their constant gain bandwidth product. The development of new active blocks that consume less power and consumes small area in addition to their suitability for high frequency applications became a must. Research efforts were directed to two different method Differential stages. One method was to introduce low power current-mode active blocks suitable for high frequency applications like current conveyors. The other method was to modify the voltage op-amps structure in order to improve their frequency response and reduce the area of the overall system.

The classical operational amplifiers (Op-Amps) are well researched and are widely used for designing analog devices. However, due to a number of known limitations related to the characteristics of the Op-Amps architecture, today we are searching for other alternative analog active elements [1]. Among them is a Differential difference operational amplifier (DDOA) [2-3], which has a number of indisputable advantages in comparison with a typical Op-Amp.

The Differential difference operational amplifier (DDOA) is rather new functional assembly of analog micro circuitry [1] and has specific connection circuits. In spite of a number of the unique characteristics it is random used in instrument making. The designing of DDA based on the bipolar and field effect technological processes which provide the radiation hardness of the circuits at the absorbed dose up to 1millirad and neutron flux up to 1013 n/cm2 is of great Current interest.

One of the requirements for the input stages of Differential stage 1, differential stage2 DDOA Fig. 1 - extended range of linear operation[6] based on biasing. In this case, the corner voltage of the pass-through characteristic $I_{out} = f(V_{inp})$ of the input Differential Stage (V_{cn}) should be commensurate with the supply voltage. If this condition is not met, then the efficiency of the use of DDOA in analog interfaces deteriorates significantly. In this case, the basic equations DDOA [4] for linear operation are violated. This leads to Differential stage to the dependence of the effective voltage transfer coefficient in typical switching schemes from the signal amplitude and nonlinear distortions.

The purpose and novelty of this article is to develop recommendations for the design of a CMOS DDOA taking into account low static current consumption of input stages and parameters of CMOS field-effect transistor processes by 0.25micro CMOS, using SPICE environment.

II. EXISTING METHOD

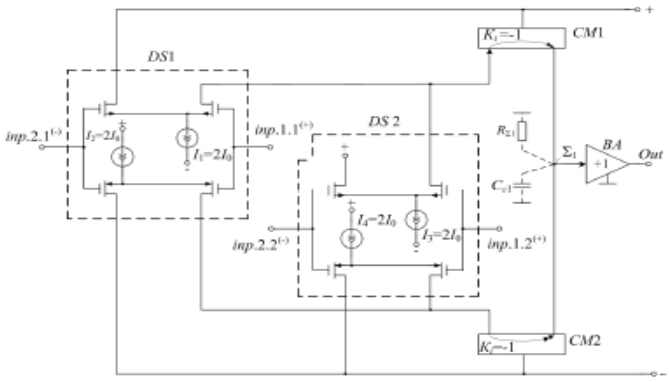

Fig.1.CMOS DDOA functional blocks

A. NONLINEAR MODE OF DDOA

We first obtain the basic equations for switching on the DDOA of Fig. 1 in the diagram of the instrumental amplifier Fig. 2 for large loop gain and 100% negative feedback, when resistor R1 = 0.

When input voltage vin.1 of Differential Stage1 relatively small ($V_{in1} < V_{cn}$) [6] based on biasing, in the circuit of Fig. 2 manifested all the advantages of the DDOA.

$$v_{out} = \frac{K_{BA} R_{\Sigma} g_{m1}}{1 + K_{BA} R_{\Sigma} g_{m2}} v_{in.1} \approx v_{in1}, \qquad (1)$$

Where KBA is the voltage transfer coefficient of the buffer amplifier BA; RΣ - equivalent resistance at the high impedance junction Σ1; gm1=gm2transmission conductivity Differential Stage1 and Differential Stage2, depending on the angle of Inclination of the flow characteristic i_{out} = f (VIN).

III. PRAPOSED METHOD

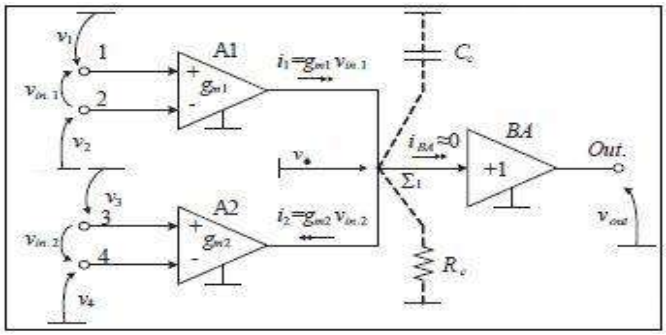

Fig.2. The functional Circuit of DDOA

In the circuit of Fig. 2 with the introduction of the feedback resistor (R1, R2) and KBARΣgm2>>1there is a possibility of digital control of the transmission coefficient, because,

$$v_{out} \approx v_{in}\left(1 + \frac{R_1}{R_2}\right). \qquad (2)$$

The Differential Stage1 is supplied with an input signal with large amplitude greater than Vcn (Vin1≥ Vcn)[6] based on biasing, the output voltage in the switching circuit Fig. 2 does not depend on the vin.1 and limited to level.

$$V_{out.max} \approx V_{lim}\left(1 + \frac{R_1}{R_2}\right). \qquad (3)$$

A. Computer simulation of DD amplifier using Mentor graphics.

Differential difference amplifier [4] comprised by 1.Current mirror,[4] 2.Diffrental amplifier (Differential Stage1), 3.Differential amplifier (Differential Stage2), 4.Buffer amplifier [4] (BA).

1.Current mirror is established to maintain current stability in whole circuit, it has MN1as source and MN2 as a mirror transistor and ammeter as a test point to measure mirror current, and which consumes less power because of its architecture nature.

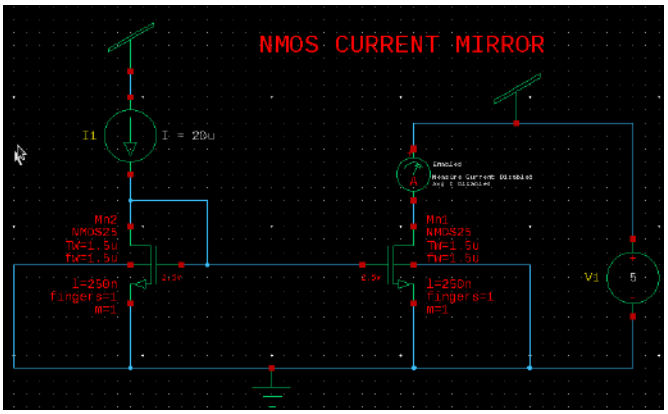

Fig.3. Current mirrors with 20µAms.

2. Differential amplifier

Basic building blocks of Differential Stage1 amplifier has MN3 as a Vin11,MN4 as aVin12, and Two MP1,MP2 are provided proper biasing for Differential Stage1,Which amplifies the difference of the input stages. Basic building blocks of Differential Stage2 amplifier has MN5 as a Vin21,MN6 as aVin22, and Two MP1,MP2 are provided proper biasing for Differential Stage2,Which amplifies the difference of the input stages.

In this architecture we are providing signals on Vin11 (Differential Stage1) and Vin21 (Differential Stage2) to make both amplifiers as inverting amplifiers.

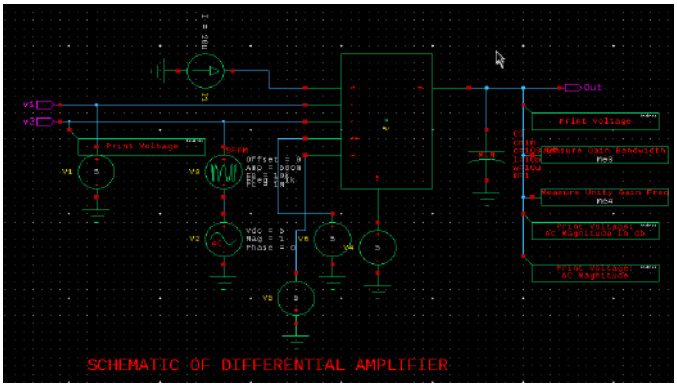

Fig.4. Differential Amplifiers.

The below figure shows the simulation results of Differential Stage1 producing gain of 23.76dB with output voltage of15.35 volts.

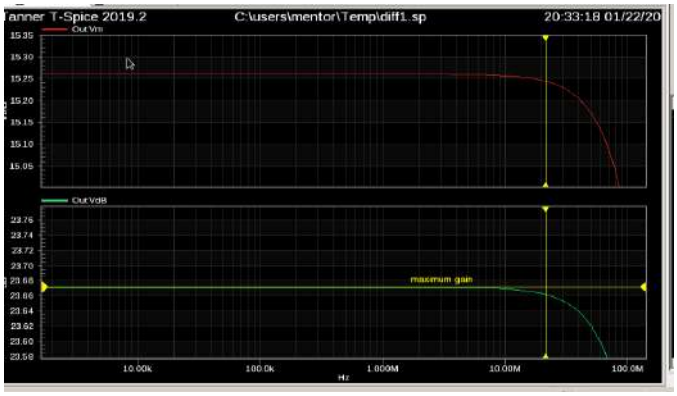

Fig.5. Differential amplifier gains with phase.

The below figure shows final DDOA with BA.BA stage constructed with common drain amplifier.

To get output simulation results we need to apply SPICE elements to the proper biased circuit, SPICE models are provides print voltage in magnitude, gain in dB, phase shift.

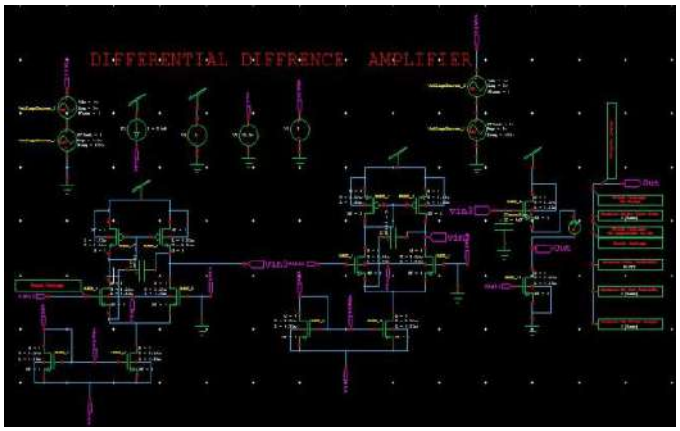

Fig.6. DDOA final schematic.

The below figure shows computer simulation results of DDOA in which static current measured with ammeter which is in mA range, when it is operated in linear region of operation.

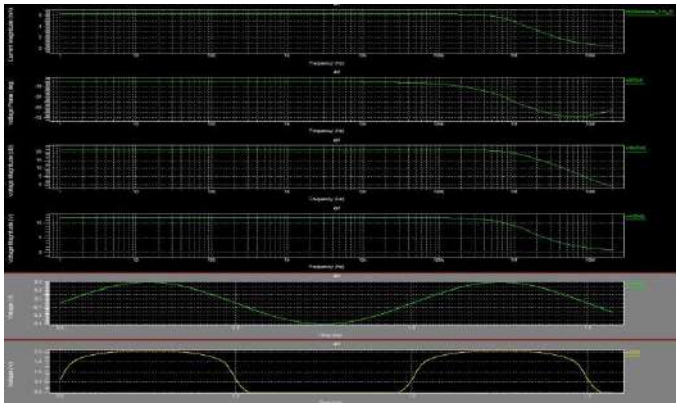

Fig.7. DDOA simulation results in linear region of operation.

The slew rate is depends on Differential stage on the changing of capacitor, the values shown in below Table.

Table.1. Capacitance V/s Slew rate

Capacitance of capacitor cc1	Previous -SR V/us	Present -SR V/us
1PF	46.5	1500
3PF	54.4	500
10PF	190	302
100PF	300	1683.3

IV. Design rules and layouts

As the length between the source and drain is 250nm or channel length, [5] we are using 250nm Technology.

Table.2. PMOS design rules.

PMOS			
S.NO	**FIELD COMPONENTS**	**LENGTH**	**WIDTH**
1.	N-WELL	2.995	4.110
2.	SUBSTRATE	1.050	1.050
3.	P IMPLANT	2.005	2.065
4.	GATE	2.100	0.250
5.	METAL	1.140	0.545
6.	GROUND	4.170	0.645

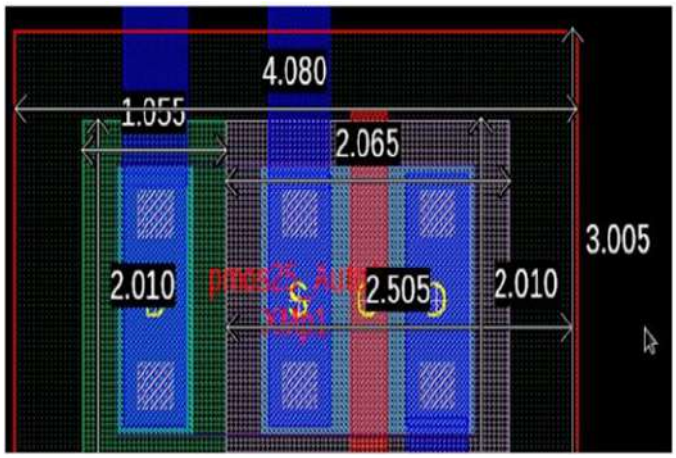

Fig.8. Design rules for PMOS

This based on the rules offered by mentor graphics 250nm technology libraries [5].

Table.3. Design rules for NMOS.

NMOS			
S.NO	**FIELD COMPONENTS**	**LENGTH**	**WIDTH**
1.	P-WELL	2.045	2.000
2.	SUBSTRATE	1.990	1.010
3.	N IMPLANT	1.550	1.495
4.	GATE	2.095	0.250
5.	METAL	3.710	0.625

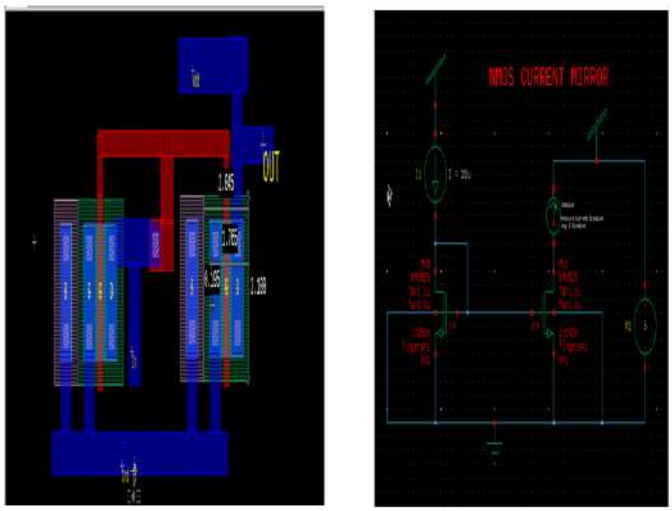

Fig.9. Design rules for NMOS and PMOS

The rules are based on the rules offered by mentor graphics 250nm technology libraries [5].

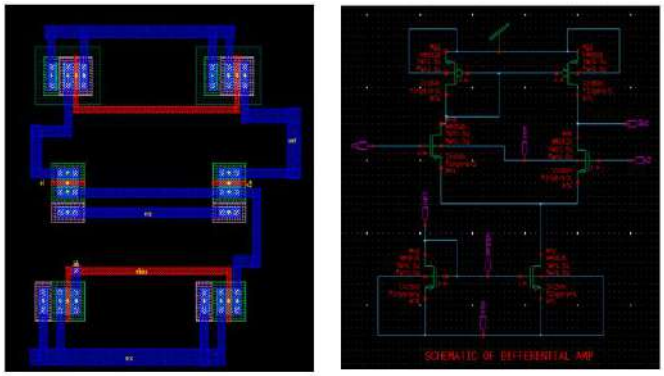

Fig.10. Design rules for Differential Stage1 or Differential Stage2.

NMOS and PMOS design rules based on the rules offered by mentor graphics 250nm technology libraries [5].

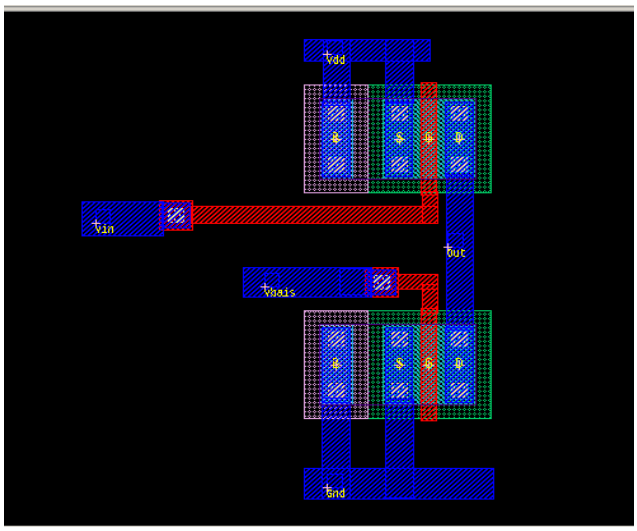

Fig.11. Design rules for Buffer Amplifier.

NMOS and PMOS layout rules based on the rules offered by mentor graphics 250nm technology libraries [5].

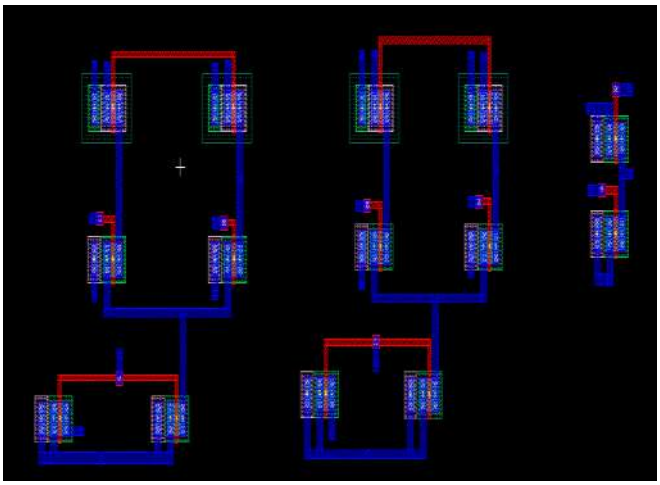

Fig.12. Design rules for DDOA.

NMOS and PMOS design rules based on the rules offered by mentor graphics 250nm technology libraries [5].

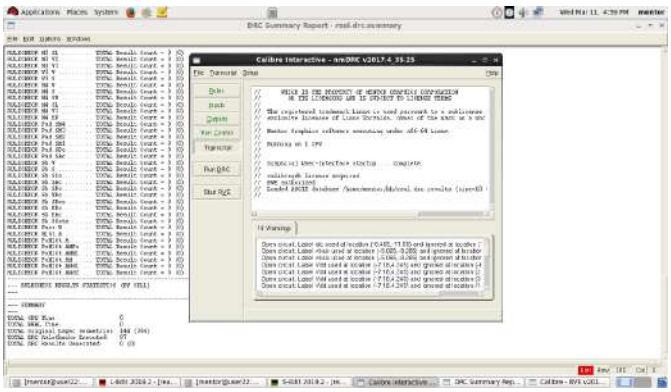

Fig.13.Design rule check (DRC) report by CALIBRE tool

V. Conclusion and to be Research

The apparent simplicity of construction and Application of DDOA is associated with the need to further improve their circuit design and exclude non-linear operating modes. When designing a CMOS DDOA, it is necessary to take into account the significant influence of the static mode, as well as the length and width of the channel of CMOS transistors on the range of linear operation of the input stages. The use of differentiation correction circuits in each input stage of the CMOS DDOA allows increasing the maximum slew rate of the output voltage of the DDOA with limitations on the static current of the input stages to analyses these we need apply fault injection at each stage. So to analyze CMOS DDOA further by injecting fault models and test their performance by IDDQ (current direct drain quiescent) and IDDT current direct drain transient) method Differential stage.

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ABOUT CONFERENCE

Online International Conference on "Smart Modernistic in Electronics and Communication" (ICSMEC-20) will be organized by St. Martin's Engineering College, Secunderabad, Telangana, India during 29th & 30th June, 2020. ICSMEC-20 will serve as a colloquy for sharing the proficiency among academicians, researchers, scientist and industrial personnel from all over the world in the areas of engineering and technology. All contributions should be of high quality, original but not published elsewhere or submitted for publication. All papers will be reviewed by eminent researchers and all accepted papers will be published in SCOPUS indexed and UGC CARE journals. All the abstracts will be published in conference proceedings with ISBN. Participants will present papers online.

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IoT Based Meteorological System by using Raspberry-Pi

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Abstract

The project aims at building a system which may be used on universally at any scale to watch the parameters during a given environment. Different physical and chemical factors, like temperature, ratio, and pollutants then on, can affect works of art on display. Each factor doesn't act individually, but its effect are often enhanced or accelerated by the presence of other factor. With the evolution of diminished sensor devices including wireless technologies it's possible to remotely monitor the parameters like temperature, humidity, smoke in air and lots of more .We are going to be using raspberry-pi 2 as main board and sensors like temperature humidity and smoke will collect all the important time information from environment and this real time information will be fetched by the online server and display it. User can access this data from anywhere through Internet. this will be checked via the phone application or by logging into the server to see the newest values updated within the database and compare those values with past values. thanks to unnatural and unpredictable weather farmers now days face large financial losses thanks to incorrect irrigation methods and wrong prediction of weather and therefore the amount of pesticides and insecticides used for crops. this technique provides genuine information to extend their crop production in agriculture field.

Key words: *Raspberry-Pi, Sensors, Web server, Weather.*

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IoT Based Meteorological system by using Raspberry-Pi

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Abstract -*The project aims at building a system which may be used on universally at any scale to watch the parameters during a given environment. Different physical and chemical factors, like temperature, ratio, pollutants then on, can affect works of art on display. Each factor doesn't act individually, but its effect are often enhanced or accelerated by the presence of other factor. With the evolution of diminished sensor devices including wireless technologies it's possible to remotely monitor the parameters like temperature, humidity, smoke in air and lots of more .We are going to be using raspberry-pi 2 as main board and sensors like temperature humidity and smoke will collect all the important time information from environment and this real time information will be fetched by the online server and display it. User can access this data from anywhere through Internet. this will be checked via the phone application or by logging into the server to see the newest values updated within the database and compare those values with past values. thanks to unnatural and unpredictable weather farmers now days face large financial losses thanks to incorrect irrigation methods and wrong prediction of weather and therefore the amount of pesticides and insecticides used for crops. this technique provides genuine information to extend their crop production in agriculture field.*

Key Words: *Raspberry-Pi, Sensors, Web server, Weather.*

1. Introduction

The advancement in wireless sensor networks are often utilized in monitoring and controlling various physical parameters within the agriculture field, meteorological observation post field. thanks to irregular and natural distribution of rain water it's very difficult to watch and control the distribution of water to agriculture field as per the need of the crop. There's no ideal and advanced irrigation plan for all weather, sort of crops cultures and soil structure. thanks to wrong prediction of weather and incorrect irrigation plan and therefore the amount of pesticides and insecticides used for crops Farmers suffer large financial losses. during this context, with the evolution of miniaturized sensor devices are including wireless technologies, it's possible remotely monitor physical parameters like temperature and humidity. Weather monitoring plays a crucial role in human life, in order that the gathering of data about the temporal dynamics of weather

1.1 Internet of Things (IOT)

Internet of Things (IoTs):The internet of things is that the inter-networking of physical devices, buildings, vehicles and other items embedded with electronics, software, sensors, actuators and network connectivity which enable these objects to gather and exchange that data. the web of Things (IOTs) are often described as connecting everyday objects like internet TVs, smart-phones, sensors and actuators online where the devices are wisely connected together enabling new sort of communication between things and other people , and between things themselves. Building IOTs has advanced significantly within the last few years .it has added a replacement dimension to the planet of data and communication technologies. it's expected that the amount of devices connected to the web will accumulate from 100.4 million in 2011 to 2.1 billion by the year 2021, growing at a rate of 36 percent per annum . within the year 2011 80% machine to machine (M2M) connections were remodeled 2G and 3G mobile networks and it's predicted that by 2021, this ratio will increase to 93% since the value related with M2M over mobile networks are generally cheaper. the event of internet of things will revolutionize variety of sectors from automation, transportation Energy, healthcare, financial services to nanotechnology IOTs technology also can be applied to make a replacement concept and wide development space smart homes to supply intelligence, comfort and to improve the standard of life.

1.2 Motivation

The motivation of project is in latest improvements in Wi-Fi and small sensor technological innovation have given base systems for considering enhancing effective modular systems. They offer the possibility of versatility in use, and system scalability. The Raspberry Pi has turned out to be ideal as the primary of such a system. There are many other realistic uses for the weather monitoring such as tracking of temperature range and humidity in a home, outbuilding, green house, or even an art gallery Although this has been designed for passive monitoring it would be possible to have this used for definitely informing someone of a heat range change, switching on warming.

2. WSN Using Raspberry-Pi

The systems described previously are taken part in gathering sensor physical information and saving them, they are doing have a couple of restrictions that are described during this project. for locating exclusions in indicator systems, creating groups of data and placing predicted information principles and evaluating them against obtained principles may be a great way of discovering defective indicator nodes and changing them, however, this project uses the in-built popular functions of MySQL web servers, namely Activates Delimiters, using these popular functions of MySQL, predicted information varies are often laid out in the info source table and any difference from this value will send a induce to aware the user that either an occasion went on or a node is broken. this will examined via the phone app or by signing into the server to see the newest principles modified within the data source and compare them with past principles.

2.1 Problem Statement

Design and Implementation of the matter (Raspberry-Pi Based Weather Monitoring System) which is interfaced with various sensors (temperature, humidity), Real-time

information are going to be gathered by all the receptors and can be fetched by the Web server. This information are often utilized by the buyer through browser.

3. SystemDesign

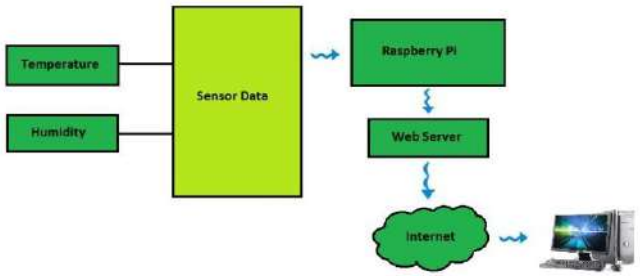


Fig-1*:* System Design

3.1 Hardware

3.1.1 Raspberry-Pi

The Raspberry Pi may be a credit- card scaled low cost computer that connects into a computer monitor or TV, and uses a typical key-board and mouse. it's a sequence of bank cards scaled single-board computers developed within the UK by the Raspberry Pi base to advertise the educating of basic information technology in educational institutions and creating countries. it's a able little device that permits people of all ages to know more about handling, and to find out the way to program in 'languages' like Python. It's ready to doing everything we've expect a private computer to try to to , from surfing round the internet and enjoying high-definition video, word-processing, to creating excel spreadsheets and playing games.

3.1.2.1 DHT11 Digital Humidity and

Temperature and Humidity Sensor:

The DHT11 may be a basic, ultra-low cost humidity and digital temperature sensor. It uses capacitive humidity and thermistor sensor to live the encompassing air, and spits out a digital signal on the info pin.

Features of DHT11:
-Full range Temperature Compensated
-Relative humidity and temperature measurement
-Calibrated digital signal
-Outstanding long-term stability
-Long transmission distance
-Low power consumption
-4Pins packaged and fully interchangeable

It's fairly simple to use, but requires careful timing to grab data. This sensor includes a NTC temperature measurement component and an resistive-type humidity measurement component and connects to a high performance 8-bit micro controller, offering excellent quality, fast response and price effectiveness.

Each DHT11 components totally adjusted within the lab that's incredibly accurate on humidity calibration. The calibration coefficients are stored as programs within the one –time programmable memory, which are employed by the sensor's internal signal detecting process the single-wire serial health applications. The averaging decimating filter provides optimization controls for limited range of frequency applications. an indoor clock drives the info sampling system, which fills the buffer memory for user access. the info capture function has three different trigger modes. the gathering of knowledge automatically allows for periodic wake-up and capture, supported a programmable duty cycle. The manual information capture mode allows the user to start out a knowledge capture, providing power and read-rate optimization. The event capture mode consistently up-dates the buffers and watches them for a preset trigger condition. This mode captures pre-event data and post-event information and generates an alarm signal for driving an interrupt. Interface makes system integration quick and straightforward.

Its small size, low power consumption and up to twenty mete single transmissions making it the simplest choice for various applications.

The DHT11 is 4 pin single row pin package.

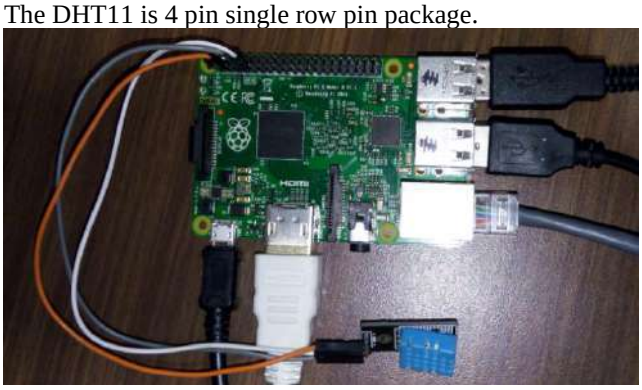


Fig-1. Rapberry Pi Interfacing with sensor

3.2. Software

Python: Python may be a general-purpose, high-level programming language. Its design emphasizes code readability and its syntax allows programmers to precise concepts in fewer lines of code than would be possible in languages like C++ or Java. The language provides constructs intended to enable clear programs on both little and enormous scale. Python supports multiple programming paradigms, including, imperative, object-oriented and functional programming or procedural styles .It features a dynamic type system and automatic memory management and features a comprehensive and enormous standard library.

3.2.2Thingspeak:

Open source data platform and API for the web of Things provides access to a broad range of embedded devices and web services. Thing Speak is an open data platform and API for the IoT that permits you to collect, store, analyze, visualize, and act on data from sensors or actuators, like Arduino®, Raspberry Pi™, Beagle Bone Black, and other components. for instance , with Thing Speak you'll make sensor-logging applications, location- monitoring applications, and a online community of things with position

up-dates, in order that you'll have your home temperature management itself supported your present place.

Fig-1: ThingSpeak

CHANNEL CREATION: ThingSpeak channels store datasent to them from apps or devices.

We have created our channel as Weather Monitoring system.

Fig-2: Channel Creation

API KEYS:

API keys enable you to write data to a channel or read data from a private channel. API keys are auto-generated when you create a new channel.

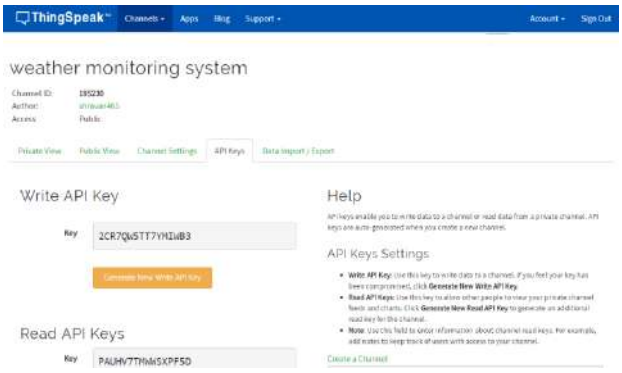


Fig-3:API Keys

4. Hardware and Software Specification

FOR COMPUTER:
Computer with Internet

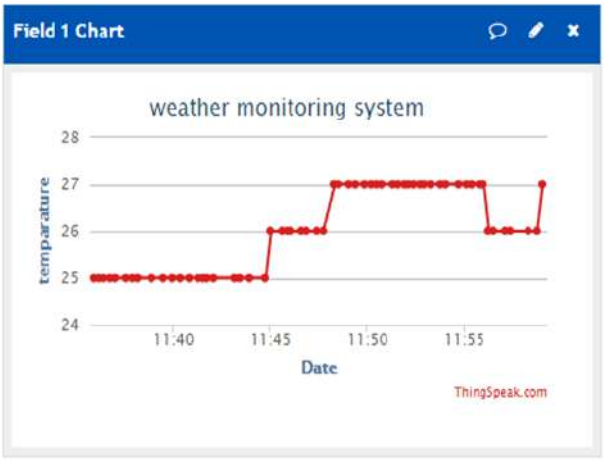
For Raspberry-pi

1) SD card of 4GB or 8GB.
2) HDMI/DVI monitor for display.
3) Ethernet cable for internet access or WIFI.
4) Mouse and Keyboard.
5) 5 v power supply.
6) Sensors.

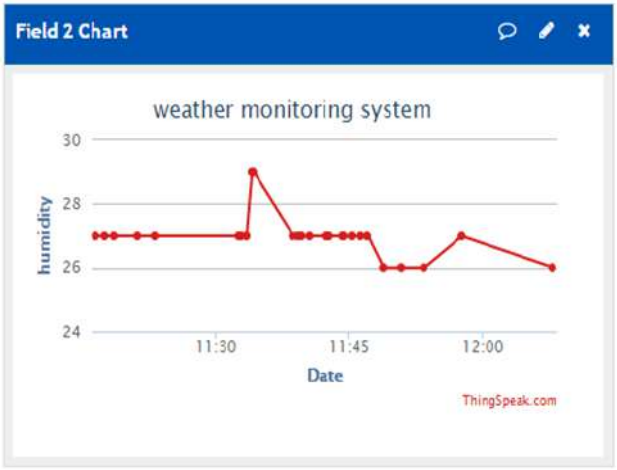
Software Specification:
Languages: Python
For Raspberry pi Board*:*
Operating system: RASPBIAN JESSIE WITH PIXEL

User interface:

For temperature



For humidity



5. Conclusion

We have implemented raspberry pi based weather monitoring system which may be wont to predict temperature, humidity within the weather. User can access this data anywhere through the web. This technique provides genuine information regarding temperature and humidity such farmers can increase their crop production.

6. Acknowledgement

I would like to take this opportunity to express our profound sense of gratitude to **Mr. Shivakumaraswamy (ECE-HOD)**, **Mr.R. Ashok kumar (COE-HEAD)**, Sphoorthy Engineering College, for their constant guidance, supervision, motivation and encouragement all the way during the project, their support and annotations are the key behind successful completion of this project work.

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https://www.element14.com/community/community/**raspberry-pi/raspberrypi2**

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Agricultural Field Motor Controlling Through IVR Service

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Abstract

Agricultural area is significant to the extent Indian resident's perspective. Profitability of agribusiness field's doesn't rely upon abundance of water sprinkled to the field, yet relies upon better coordinating of water flexibly with crop request and uniform ecological conditions that are reasonable for cultivating. Under water system or over-water system framework prompts unreasonable or less water flexibly which may cause more terrible outcomes for example yield decrease. The venture depends on initiation or deactivation of machines remotely, which is utilized by essential cell phones that incorporate a working framework. The IVR administrations assumes a urgent job in this venture where the rancher can comprehend the guidance by the language which he knew. In this undertaking Commands are given as voice guidelines to the portable utilized by individual, who will actuate or deactivate (or) Turn it on/off the water system engine and furthermore know the ebb and flow status of engine by the assistance of GSM module and Raspberry pi.

Keywords: *IVR services, Raspberry pi, Monitoring And Controlling System, GSM, AT commands, DTMF.*

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Design and Implementation of C.C.S.D.S Data Simulator in Altera VHDL

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Abstract

Space station receives data from different remote sensing satellite and process depends on user requirements. The data has to be frame synchronize with the hardware. Before launch of a satellite into its orbit, it is important to check all health parameters of ground station equipment are proper. To test hardware units developed for receiving satellite data and to maintain these hardware units, a standard format simulator is required which will generate data in satellite data format. Satellite launching involves huge cost designing of data format simulator importance is high. The project is implemented and tested using ALTERA EPM7160SLC84-7 EPLD. The required software has to be developed using the ALTERA VHDL language. Here we are developing in a CCSDS format. CCSDS means Consultative Committee for Space Data System. This is an organization officially established by the management of member space agencies. If satellite uses CCSDS format, data from satellite can be received by anyone who have compatible receiving hardware.

Keywords— *ALTERA,EPLD,CCSDS*

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Design and Implementation of C.C.S.D.S Data Simulator in Altera VHDL

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Abstract— **Space station receives data from different remote sensing satellite and process depends on user requirements. The data has to be frame synchronize with the hardware. Before launch of a satellite into its orbit, it is important to check all health parameters of ground station equipment are proper. To test hardware units developed for receiving satellite data and to maintain these hardware units, a standard format simulator is required which will generate data in satellite data format. Satellite launching involves huge cost designing of data format simulator importance is high. The project is implemented and tested using ALTERA EPM7160SLC84-7 EPLD. The required software has to be developed using the ALTERA VHDL language. Here we are developing in a CCSDS format. CCSDS means Consultative Committee for Space Data System. This is an organization officially established by the management of member space agencies. If satellite uses CCSDS format, data from satellite can be received by anyone who have compatible receiving hardware.**

Keywords— ALTERA,EPLD,CCSDS

I. INTRODUCTION

The data acquired from the satellite is in serial format. This serial data will be fed to front-end hardware, which will feed this data to PC. To take this front-end hardware, data will be generated in satellite data format by using Generic Data Simulator. Remote sensing satellites like IRS-1A, IRS-1B, IRS-1C, IRS-1D, IRS-P3, IRS-P4 send the data continuously covering the whole globe in some specified times, they send the particulars of any continent the weather information, sea particulars, degree of vegetation. They may scan the same area of the continent twice in a day. The information that is transmitted by the satellite will be received at the ground station.

A. Satellite Data Reception System:

As earth reflects sunlight, the reflected light energy will vary depending on the earth's characteristics like soil, water, rock. The satellites use photo detectors to detect this light they receive. The output of the photo detector is amplifies by photo-multipliers and fed to an analog to digital converter

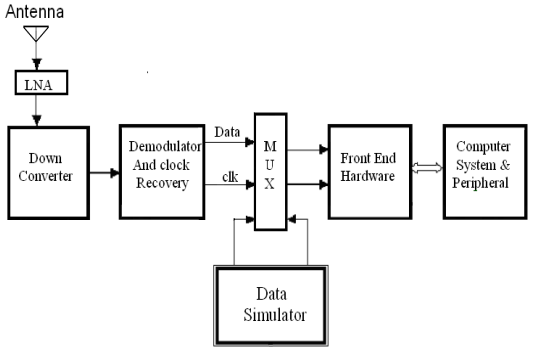

Fig 1-Typical satellite data reception system

The word size of this data will vary from satellite to satellite and can be of 8-bit, 12-bit width. This parallel data will be converted into serial data. The serial is modulated in (PCM) QPSK or BPSK and transmitted to earth with a carrier frequency (8 GHz, 4 GHz). The received signal at earth in converted to an intermediate frequency and then fed to a demodulator. To test the front end hardware, data will be generated in the satellite data format using Generic satellite Data simulator. The upcoming remote sensing satellites will come in a standard CCSDS format. This is a standard format which is getting implemented in different regions of India and foreign satellites. The design of data simulator depends on its

silent features. Data simulator will be designed in the CCSDS 131.B1 format.

B. Format Generation

Data is attached to the frame sync code which is fixed for every satellite and is known. This is to indicate start of the frame that consists of FSC, auxiliary data and video data. Line length of the frame will be specified according to CCSDS format. Line length gives us the information about the number of words (bytes) in the frame. It is impractical to handle data bit wise as the line length or the data format for satellite would be of the order of some 1024 bytes or even more. It is more preferable to handle it one byte at a time, for this purpose we make use of a word counter. Word counter counts the number of bits in the word.

C. Line Length Generation

Line length of the frame will be specified according to the CCSDS format. Line length gives us the information about the number of words (bytes) in the satellite data format.

D. Serialization

Since data coming from the satellite is in serial form, it is necessary to convert parallel data into serial data. To convert this parallel data into serial 8-bit parallel-in-Serial-out shift register is used.

E.Randomization

In order to maintain bit synchronization with the received communications signal, every data capture system at the receiving end requires that the incoming signal have a minimum bit transition density i.e. eliminating long sequence of ones and zeros to ensure accurate timing recovery without redundant line coding

II. BACK GROUND OF THE INVENTION

Data will be serially transmitted one bit at a time along a data transmission path. The serial data can be transmitted in groups of bits called frames. The frames are delimited by synchronization codes that identify the beginning or the end of each frame. The synchronization codes must be identified in the data stream before the significance of the data contained in the frame can be determined. When a synchronization code is identified, a signal can be generated to synchronize a data recovery circuit to the contents of the frame .The synchronization of the data recovery circuit to the frame is "FRAME SYNCHRONIZATION". Satellite stays only for 15 minutes at one location, it is important to check all health parameters of ground station equipment are proper, to test hardware units developed for receiving satellite data and to maintain these hardware units. A data simulator is required which will generate data in a specific format. The data from satellite comes in a serial form and now it is important to decide where a frame begins and where it ends and also where the desired auxiliary data and video data begin in a particular frame. For this the serial data coming from the satellite is stored in a shift register whose length is equal to the length of FSC. Before each shift, data in the register is compared with the known FSC using a comparator. If the FSC matches, a pulse is generated which indicates the start of valid data. The pulse thus generated also initiates a counter whose Mod value is equal to the frame size.

The detected FSC will be a valid one if it is repeated after each frame length. The detected data is sent for further processing.

A data simulator can be simply told as a virtual satellite. All the processing done in satellite for data generation, same are done in the data simulator and some specific data is generated and sent to the ground station for testing of its hardware equipment so as at the time of real time data receiving there won't be a loss of data due to damaged equipment of ground stations. The further designing will be explained in detail in chapter 6-DESIGN PHASE CCSDS is an organization officially established by the management of member space Agencies. Participation in the CCSDS is completely voluntary, the results of committee actions are termed recommendations and are not considered binding on any Agency.

The **Consultative Committee for Space Data Systems (CCSDS)** founded in 1982 by the major space agencies of the world, the CCSDS is a multi-national forum for the development of communications and data systems standards for spaceflight for governmental and quasi-governmental space agencies to discuss and develop standards for space data and information systems.

The CCSDS works to support collaboration and interoperability between member agencies through the establishment of data and system standards. The goal is to enhance governmental and commercial interoperability and cross-support, while also reducing risk, development time and project costs. The CCSDS has developed data standards and information system frameworks covering a variety of areas including data creation, transmission, management and preservation as well as the systems supporting that data. These include protocols and network notes for communication in space including contributions to Interplanetary Internet and Space Communications Protocol Specifications.

Members Agencies of CCSDS are NASA, CSA, NASDA, RSA and observer agencies are ASA, ISRO, SSC etc.. If a satellite uses CCSDS format, data from satellite can be received by anyone who have compatible receiving hardware. This is an advantage of CCSDS when compared with the previous technology. Data here is transferred in packets rather than continuous running data.

Functions for transferring Transfer Frames over space link:

I. Error –control coding;
II. Synchronization
III. Pseudo-randomizing.

The following is the flow chart which is to be followed in order to accomplish CCSDS recommendation:

At the sending end internal organization is as follows

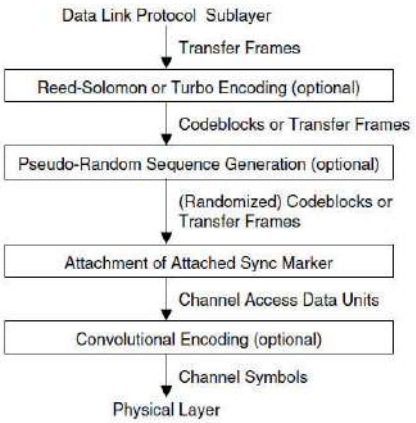

Fig: 2 operations at sending end

III. QUARTUS SOFTWARE TOOL

The ALTERA Quartus II design software provides a complete, multiplatform design environment that easily adapts to your specific design needs. It is comprehensive environment that easily adapts to your specific design needs. It is a comprehensive environment for system-on-a-programmable-chip (SOPC) design.

The Quartus II software includes solutions for all phases of FPGA and CPLD design.

The Quartus II software includes modular compiler. The compiler includes the following modules

- Analysis and synthesis
- Fitter
- Assembler
- Timing analyzer
- Design assistant*
- EDA net list writer*
- Compiler database interface*

Modules marked with * are optional during compilation, depending for your settings.

Converting MAX+PLUS II projects:

The convert MAX+PLUS II project command allows you to select an existing MAX+PLUS projects assignments & configuration file (.asf), or design file, and convert it into a new quartus II project that contains all supported assignments and constrains from the original MAX+PLUS II project, this command automatically imports the MAX+PLUS II assignments and constrains.

Quartus II software can be used to create a design in Quartus II block editor or use the Quartus II text editor or use the Quartus II text editor to create an HDL design using AHDL, Verilog HDL, or VHDL design languages.

Following design file types can be used to create a design in the Quartus II software or in EDA design entry tools

- Block design file.
- EDIF input file.
- Graphic design file.
- Text design file.
- Verilog design file.
- VHDL design file.
- Verilog Quartus mapping file.

A. Design Methodologies And Design Planning:

It is important to consider the design methodologies the Quartus II software offers, while creating a new design. In the top down design flow, there is only one output net list for the entire design, which allow you to perform optimization across design boundaries and hierarchies for entire design, and often simpler to manage.

In bottom-up design methodology, there are separate net lists for each design module. This functionality allows compiling each module.

- Block based design flow:

The general block-based design flow concepts can be used in modular, hierarchical, incremental, and team- based designs flows.

- Design portioning:

When creating a hierarchical design in Quartus II software or in other EDA tools, the design EDA tools, the design is portioned into separate modules. Factors under consideration are

- Where to partition the design.
- The number of clock and I/O connections between partitions.
- Placement of state machines.
- Separation of timing-critical functions from non-critical functions.
- Limiting the critical path in hierarchical modules.
- Registering the inputs and outputs of individual modules.

Analysis and synthesis is used to analyze and synthesis VHDL and Verilog HDLdesigns. It also includes integrated synthesis, which fully supports the VHDL and verilog HDL languages and provides options to control the synthesis process. Analysis and synthesis builds a single project database that integrates all the design files in a design entity or project hierarchy. It also examines the logical completeness and consistency of the project, and checks for boundary connectivity and syntax errors. The messages window and the messages section of the report window display any messages analysis & synthesis generates.

The status window records the time spent processing in analysis and synthesis during project compilation.

Controlling analysis & synthesis:

- Compiler directives and attributes.
- Quartus II logic options.
    - Quartus II synthesis net list optimization options.

Simulation:

Quartus II provides the following features for functional and timing simulation

- Integration with EDA simulation tools
- Functional and timing simulation libraries.
- Generation of output net list files.
- Power gauge power estimation.

- Generation of test bench template and memory initialization files.

The Quartus II software allows to simulate an entire design, or to simulate any part of a design. Before simulation, appropriate simulation net list must be generated by either compiling the design for timing simulation or choose to generate functional simulation net list command for functional simulation. The following steps describe the basic flow for performing either a functional or timing simulation in the Quartus II software:

- Specify simulator settings.
- If functional simulation is being performed, and then choose generate functional simulation net list command. If you are performing a timing simulation, compile the design.
- Create and specify a vector source file.
- Run the simulation using start > start simulation command (processing menu), the simulation tool window, or the quartus_sim executable.

B.Creating Waveform Files

The Quartus II waveform editor allows create and edit input vectors for simulation in waveform or text format. Using the waveform editor, input vectors can be added to waveform file that describes the behavior of the logic in the design.

C.Timing Analysis

The quartus II timing analyzer allow you to analyze all performance of logic in design and helps to provide fitter to meet timing requirements in the design. By default the timing analyzer runs automatically as a part of a full compilation to analyze and report timing information. The information generated by it can be used to analyse debug and validate the timing performance of the design. It allows you to specify the desired speed performance for entire project and specific design entities.

- Specifying project wide timing settings
- Performing a timing analyses
- Viewing timing analyses results

D.Debugging

Quartus II signal tap logic analyzer and signal probe feature analyse internal device nodes and I/O pins while operatimg in a system. The signal tap II logic analyzer uses an embedded logic analyzer to route signal data through the JTAG port to either signal tap or the logic analyzer.

IV.DESIGN PHASE

A. Data Simulation Procedure

The aim of this project is to design a Data Simulator for testing the hardware units designed for receiving data from the Remote Sensing Satellites. The data simulator is designed to generate the data in a specific format for a given satellite.
For every particular frame specified as per the C.C.S.D.S format, out of the 2400 bytes in each band (by IRS-P5) the first 32 bits are called as frame sync codes. These codes are essential in synchronization i.e. they indicate the beginning of data. The word size of the data satellite is 8 bit. The FSC and data are stored into an array. As handling bit by bit is a lengthy procedure, we will handle the data word by word. For this we will generate a word clock from the master clock. The frequency of the clock will be $1/8^{th}$ of the master clock frequency. After every 8 clock cycles, a load pulse is generated to count the no. of words in a data format a line length counter is used which will count from 0 to frame length and repeat. Depending on the count and clock signals, the data is obtained in parallel form, which is 8 bit size. All the lines contain similar data continuously except line count values. For selection of line generation, a reset pulse is used. When reset is in high mode will be incremented and line length is chosen. We have generated two line lengths for FSC generation with two different modes of operations. Every satellite has fixed FSC code. This FSC should be transmitted without errors, it transmitted then error should be detected and hence we should be aware of bit error tolerance and the detector side.

B.Frame Synchronizing

The randomized data is received by earth stations. This incoming data is taken for FSC detection process. The synchronization codes must be identified in the data before the significance of the data contained in the frame can be determined. When a synchronization code is identified, a signal can be generated to synchronize a data recovery circuit to the frame is “FRAME SYNCHRONIZATION”. For the serial data coming from the satellite is stored in the shift register whose length is equal to the length of FSC. Before each shift data in the register is compared with the known FSC using correlator. If a maximum match occurs, a pulse is generated which indicates the start of all valid video data. The detected FSC will be valid one if it is repeated after each frame length.

Frame synchronous code:

1A CF FC 1D – for 32 bit FSC for CCSDS data simulator

First bit (0)

↓

0 0 0 1 1 0 1 0 1 1 0 0 1 1 1 1 1 1 1 1 1 1 0 0 0 0 0 1 1 1 0 1

Last bit (31)

Since data coming from satellite is in serial form it is necessary to convert parallel data into serial data, for which we require a 8 bit PISO shift register. The inputs to shift register are master clock, load pulse and parallel data. The operation of shift register depends on the load signal. Load pulse is generated after every 8 clock pulses. When load is high parallel data is loaded into Shift register and it performs shift operation when load signal becomes low. Data is shifted

by bit by bit serially in synchronization with master clock. Thus it generates serial data. The serial data is then randomized with specific pseudo random bit sequence to avoid any synchronization problems. For this purpose PN sequence generator is used. The PN sequence shall be generated using the following polynomial.

h(x)=x^7+x^5+x^3+1

This sequence begins at the first bit of the code block and repeats after 255 bits, continuing repeatedly until the end of the clock block. The sequence generator is initialized to the all-ones state at the start of code block and sequence will be continued by the implementation of the polynomial. The inputs to this PN generator are master clock, seed word. The output of the shift register is a Pseudo Random Bit Sequence (PRBS). The frame sync code is sent at the starting which should not be randomized. Randomization is done by EX-oring the serial out and PRBS sequence. This is synchronized with master clock before sending to the output. Since data coming from satellite is in serial form it is necessary to convert parallel data into serial data, for which we require a 8 bit PISO shift register. The inputs to shift register are master clock, load pulse and parallel data. The operation of shift register depends on the load signal. Load pulse is generated after every 8 clock pulses. When load is high parallel data is loaded into Shift register and it performs shift operation when load signal becomes low. Data is shifted by bit by bit serially in synchronization with master clock. Thus it generates serial data. The serial data is then randomized with specific pseudo random bit sequence to avoid any synchronization problems. For this purpose PN sequence generator is used. The PN sequence shall be generated using the following polynomial

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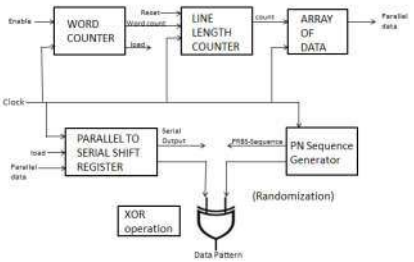

Fig: 3 Block diagram of data simulator

The main parts are

- Clock Generator
- Word counter
- Line length counter
- Serial data generator
  a) Parallel –to-Serial converter
  b) PN sequence generator
  c) Randomizer

The basic clock is obtained from a 105MHZ crystal controlled oscillator at ECL levels. The 105MHZ clock is divided by 2 to get 52.5MHZ at ECL levels. This signal level is converted to TTL since the EPLDs operate at TTL LEVELS. The data format of the satellite IRS-P5 is (the satellite transmits data in a particular format) 2400bytes. It is impractical to handle this data bit wise. It is more preferable to handle one byte at a time. To this purpose, we make use of word counter. The word counter is a 3-bit or 8-state counter that can count from 000 to 111. The word counter is used as a divide-by-8-counter**.** The line length counter is utilized to count the number of words in the satellite data format. Line length of frame will be specified according to the CCSDS format. Line length gives us the Information about the number of words (bytes) in the satellite data format. Depending on the signals 'clock' and 'count', an 8 bit parallel data is obtained. In this the parallel data is converted into serial data and the randomized. Randomization or scrambling is a method to achieve DC balance and to eliminate long sequence of '0's or '1's to ensure accurate timing recovery without reluctant line coding. Scramblers use maximum length shift registers on the input bit stream to 'randomize' or 'whiten' the statistics of data making it look more random. To achieve this, a PN-Sequence is generated and is XORed with the serial data obtained from the Parallel-to-Serial-converter.

The PN sequence generator generates a pseudo random bit sequence (PRBS).

Sequence**:** The first 40 bits of the pseudo-random sequence from the generator are shown below. The leftmost bit is the first bit of the sequence to be exclusive-ORed with the first bit of the Code block or Transfer Frame; the second bit of the sequence is exclusive-ORed with the second bit of the Code block or Transfer Frame, and so on.

1111 1111 0100 1000 0000 1110 1100 0000 1001 1010 . . . .

Logic Diagram:

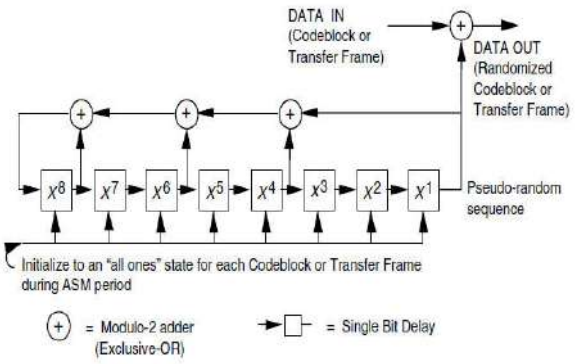

Fig 4. PN Sequence generator

Fig. represents a possible generator for the specified sequence (Pseudo-Randomizer Logic Diagram)

C.Randomiser

The serial data is randomized by modulo-2 summing of PRBS and serial output data. The randomized data is synchronized with the master clock before being sent out.

IV. OUTPUT WAVEFORMS

1) At the beginning -showing FSC and 1st data

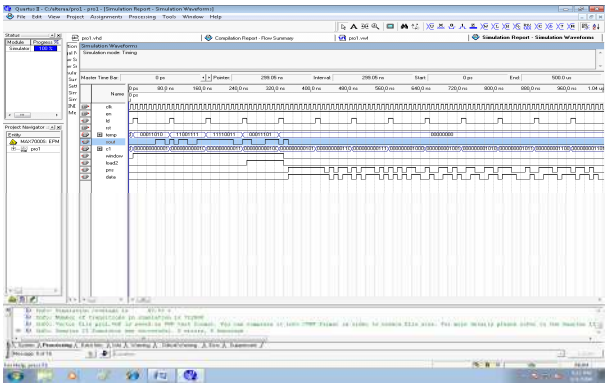

Fig.5

2) After all zeros data, at next data sequence as shown below

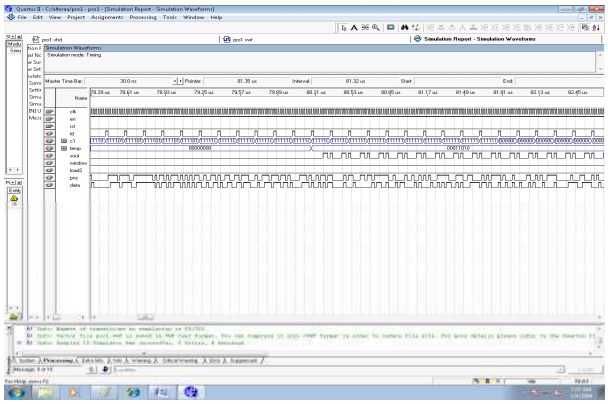

Fig.6

3) Next sequence data starting

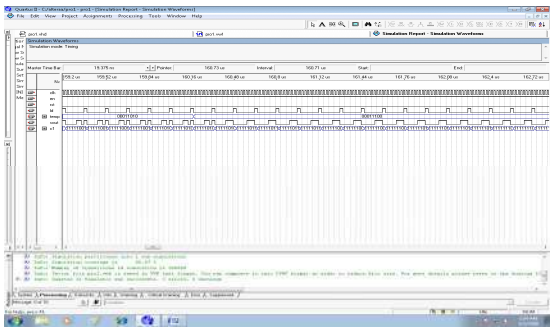

Fig.7

4) After ending of all data bytes-showing again start of FSC (showing it as a loop)

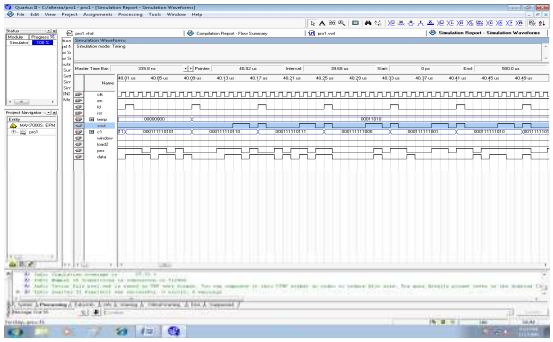

Fig.8

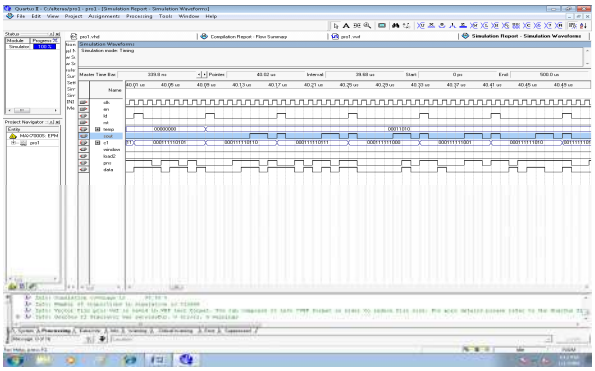

Fig.9

V. SIMULATED WAVEFORMS

when mode is 00

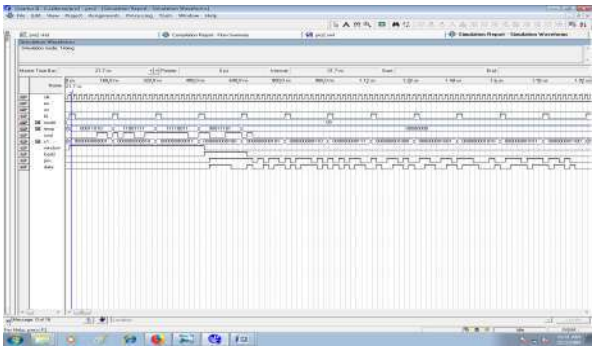

Fig.10

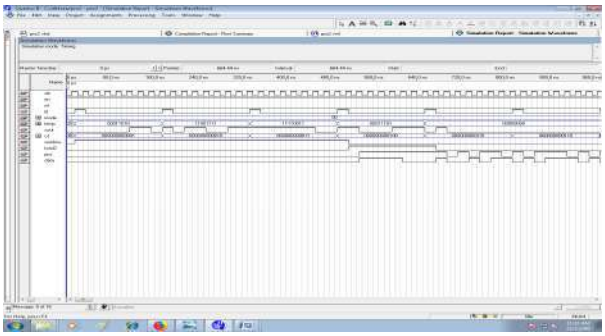

Fig.11

VII.CONCLUSION

All the possible steps of CCSDS format design of data simulator was generated and implemented using ALTERA, EPLD, EPM 7160SLC84-10. Simulation was carried out on ALTERA Quartus II software using VHDL language.

VIII.APPLICATION

Generic satellite data simulator has two applications:
I.PRE LAUNCH:
It will be used for design development and testing of the front end hardware, before launching of the satellite.
II.POST LAUNCH:
It will be used for maintenance of the front end hardware after launching of the satellite. It will be used to test the functionality of front end hardware and the system interface every day to ensure that the satellite data will be received and achieved properly.

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Advanced Memory Management Unit for 3-D Network on Chip

Publisher: IEEE

Kumar K. Ashok ; V. Karunakar Reddy All Authors

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Future generation chip multiprocessor (CMP) contains thousands of cores to increase performance the system. Network on Chip (NoC) is new paradigm for the intercommunication of System on Chip (SoC). 3-D NoC is the new way of improvement in NoC fabric to achieve high performance. One of major drawbacks of NoC is memory unit and it is proportionally increases in 3-D NoC. A first in first out (FIFO) is conventionally placed in NoC router to store data packet temporarily. The memory is critical issue for NoC based SoC because of size and cost of device. Advanced memory architecture presented to optimize the performance of NoC router. This paper proposes a random access memory (RAM), which is a bridge between input ports and crossbar switch. This technique is simulated in Xilinx 14.7 ISE and implemented in Vertex-6 FPGA device.

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Contents

I. Introduction

Network on Chip (NoC) is one of the optimized solutions for issues of intercommunication in System on Chip (SoC). As technology improves, a lot of improves observed at architecture of NoC that is 3-D NoC. To improve the performance of SoC, number of Processing Elements (PE) are added to the single die. The PEs is connected vertically and horizontally in 3-D NoC thereby achieving higher performance than 2-D NoC within same die. PEs are able communicate data among them in case of heavy traffic thereby reducing the latency and power consumption. Memory is the critical problem when PEs is active or idle during data transmission from source to destination. Hence, highlighting the memory management block during data packet transfer will avoid the performance degradation. Conventionally, NoC is composed with number of routers and PEs to obtain parallel communication among PEs [1]. The router is a unit which realizes with number of input and output ports and also crossbar switch. Arbiter is used to resolve arbitration among the ports with efficient scheduling algorithms [2]. Each port is realized with memory unit to store the data packet and its controller unit to control data transfer. Typically, First in First out (FIFO) is used as memory management unit and the size of FIFO depends on the size of data packet because of easy to implement data transfer operations. However, FIFO has several disadvantages like synchronization and also depth of queue leads to penalty in terms of both latency and energy. According to Moore's law, the number of devices on single die is double for every eighteen months. Hence, designing of low latency and power efficient chip is critically complex As computational power consumption is exponentially increases than dynamic power consumption, hardware efficient processor is preferred to trade off between performance and power consumption thereby spreading the tasks to the multiple PEs. An individual PE is to off/on when it is idle and also run its own with optimized supply voltage to save power consumption. A one of the fundamental problems lies in SoC is memory management unit because of optimized data transfer from and to memory interface devices. In future, using of memory management units in NoC is not only increases delay but also rises the issues in terms of scalability and portability. The memory units are critically complex in NoC based SoC designs because of it is increased in number and also distributed in nature. Fig. 1 shows typical memory management unit for entire PE in SoC design which is shared memory interface unit. The shared memory interface unit is used to data transfer in general purpose PE in the FPGA based multiprocessor system. The shared memory architecture is also known as Connected RAM (CoRAM) which is capable of reconfigurable both standalone and heterogeneous fabric. The reconfigurable logic is existed from and to storing of data through memory interface units in NoC with boundaries of linear address. The implementation of CoRAM is simple which is made up of wire level SRAM thereby distributing spatially to obtain higher bandwidth than conventional designs. However, data packet of each CoRAM is controlled by FSM controller thereby deviating drastically. In any SoC fabric, the operation of FIFO is executed using shift register where requirement of storage is limited otherwise embedded RAM is utilized for large requirements. The typical

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Advanced Memory Management Unit for 3-D Network on Chip

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***Abstract*—Future generation chip multiprocessor (CMP) contains thousands of cores to increase performance the system. Network on Chip (NoC) is new paradigm for the intercommunication of System on Chip (SoC). 3-D NoC is the new way of improvement in NoC fabric to achieve high performance. One of major drawbacks of NoC is memory unit and it is proportionally increases in 3-D NoC. A first in first out (FIFO) is conventionally placed in NoC router to store data packet temporarily. The memory is critical issue for NoC based SoC because of size and cost of device. Advanced memory architecture presented to optimize the performance of NoC router. This paper proposes a random access memory (RAM), which is a bridge between input ports and crossbar switch. This technique is simulated in Xilinx 14.7 ISE and implemented in Vertex-6 FPGA device.**

Keywords— ***Memory Management Unit; FIFO; NoC; SoC; FPGA***

I. INTRODUCTION

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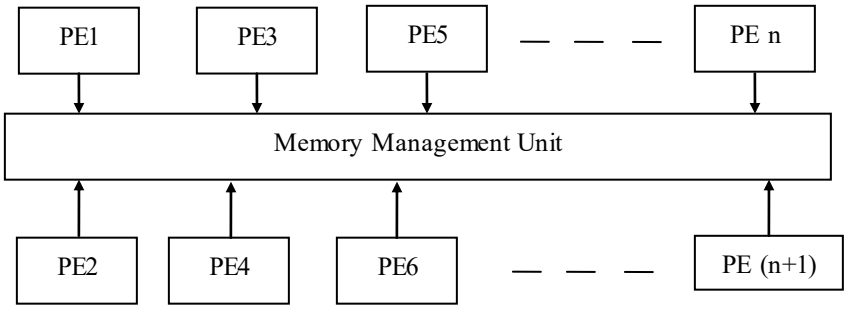

Fig.1 Shared memory architecture for FPGA based Multiprocessor

Considering above drawbacks, this paper is focusing mainly on the static memory management units especially on FIFO designs. In order to obtain high performance, the buffer is implemented with distributed manner with virtual cut through packet switching. The remaining paper discussed as follows: section-II presented related work and section-III explained the distributed MMU architecture and also presented the improved design of NoC fabric. Section-IV propounded results and discussion and finally, section-V concludes the paper.

II. RELATED WORK

3-D NoC is one of major improvements in the NoC based SoC fabric to achieve high performance. Memory Management Unit (MMU) plays an important role for managing FIFO based buffer of each port. Shibata et. al. [3] proposed a new architecture to reduce power consumption in terms of address pointer of shift registers. A swapped two-port memory cell with bit line/word line configuration is proposed to obtain low power and high speed. The experimental results are proven that the speed of operation is massively increased. However, the power consumption is also increased at higher operating frequencies. Chen, X [4] propounded a shred memory with microcoded controller to the hardware module thereby connecting each node to the memory module or core of the network. The microcode is the one of the oldest technology to compensate both performance and flexibility of the network. Hence, the dual microcoded controller is proposed to utilize various functions efficiently. The DMC has mainly two processors which are able to handle the requests from local PE and also remote PE of the network. Though the DMC provided efficient delay and optimized solution for hardware, still flexibility of DMC in network is complex problem. To provide bridge between internal FIFO and external memory modules, Chung et. al. [5] proposed a connected RAM (CoRAM). In addition to bridge, the CoRAM structure provides virtualized memory units for obtaining improved efficiency and performance. The CoRAM is composed with reconfigurable logic which is integrated with LUT based modules to access of virtual address space. The experimental results are proven that the CoRAM is presented high performance, low power consumption and less area utilization. However, it increases the design time and also raises the issues in scalability and portability. To support ultra low power (ULP) processors, Jang et.al. [6] proposed memory management unit with embedded NoC (MMNOC). Due to area, latency and power, integrating typical MMU to NoC is complex. Therefore isolating MMU from hardware and integrating to local PE of source router. Hence, providing a direction to the researchers to embedded MMU to lightweight ULP processors. The simulation results are shown that the almost 50% required gate count of core interface is reduced than Microcoded controller [4]. Because of dual processors involved in MMNOC, the chip area utilization and power consumption is overhead than recent designs. Gordon-Ross et. al. [7] proposed an efficient structure of synchronous FIFO to enhance the memory management in NoC based systems. The synchronous FIFO design uses two phase clock that avoids the race around condition between the data operation and addresses. It incorporates advantages of two port SRAM memory cell to improve speed of data operations. This design simplifies the circuit which uses empty/full flag to record of maximum address of FIFO. The results are presented that the speed of data operation is highly increased and power consumption is reduced. Though, there is problem for optimizing of performance and flexibility. To optimize utilizations of resources, Siast et.al. [8] presented a new scheme that is RingNet. The RingNet uses a distinctive feature that is data operations are conducted on centrally placed memory which supports preventing of data congestions thereby requiring less network buffer for NoC fabric. The design of RingNet exhibits two different properties which are responsible for controlling of the traffic and also data communication through the FIFO buffers of the system. The RingNet provides low cost and lower resource utilization because of resources is shared among the PEs. Therefore, utilization of resources is proportional to the number of PEs involved in the data operation. Apart this, the However, the system latency is increased because of centrally placed memory.

From the literature, memory management unit is plays vital role in NoC based SoC and it critically important to achieve high performance. This paper has proposed the distributed memory management unit in place centrally located memory. These distributed MMU is supported virtual address space therefore compatible for less resource utilization. To optimize performance and flexibility, NoC is proposed with virtual cut through packet switching.

III. DISTRIBUTED MMU ARCHITECTURE

A design of central located memory unit and implementation for NoC is simple therefore most of the designs are composed with it [9]. However, it is not suitable for the future generations therefore this paper proposes distributed memory units. Fig.2 shows structure of the centralized MMU where entire PEs are connected with centralized memory.

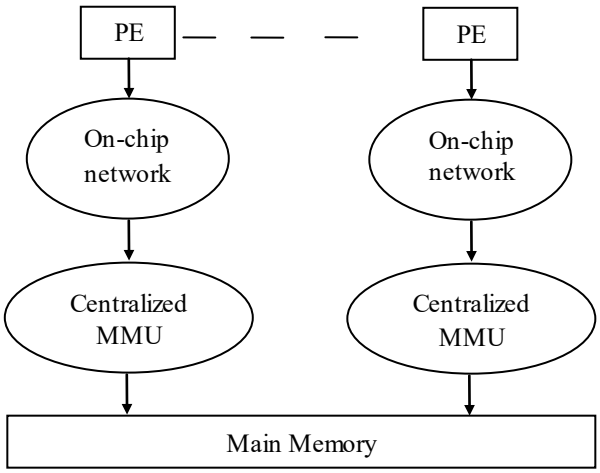

Fig.2 Structure of centralized Memory Management Unit

The problem of centralized MMU is higher network latency because of too many requests are hitting the main memory and also on-chip network which is placed between PE and centralized memory is another major issue thereby raising issues with scalability. To prevent these bottlenecks and to handle memory access requests in NoC, this paper proposes the distributed MMU which requires more number of MMUs. With proper placement of MMUs, improved NoC is showed the high bandwidth utilization and less traffic.

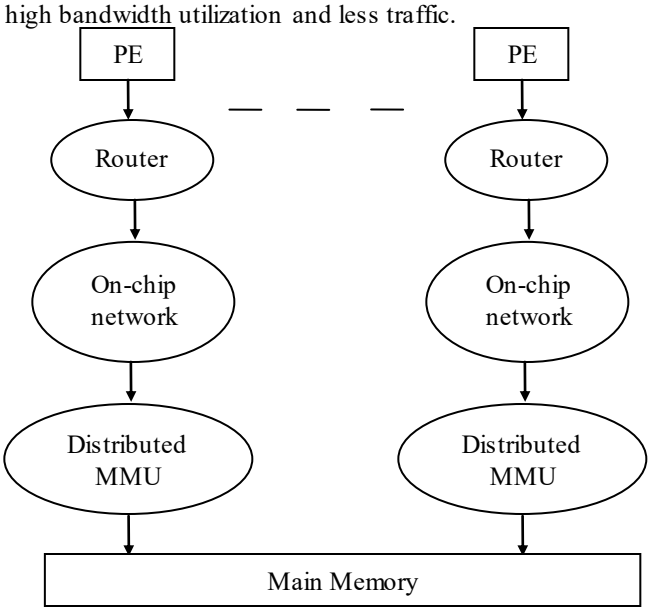

Fig. 3 Structure of Distributed MMU

Fig. 3 shows the structure of distributed MMU which accesses the memory request separately through virtual address. The PE requests main memory channel through distributed MMU based on routing tables. These routing tables are updated every clock cycle thereby assigning request to the idle MMU. The current router is controlled the memory request and its distributed MMU thereby accessing main memory in case of availability otherwise assigning to another MMU. This paper considers 7X7 mesh based 3-D NoC therefore requiring 6-memory channels to access main memory for the entire network. Each distributed MMU is dedicated to memory request of respective PE and in case unavailability or overloaded, assigning to another dedicated MMU. When MMU receives a request to access memory, it decodes the address and give the access if it is available therefore injects the data packets into the network. A one bit flag is set once the request is closed otherwise the flag reset which is not shown figure. The empty/full flag bit detects reads and write operation using D-flip flop (DFF) circuitry which is connected serially.

The structure of empty/full flag is as shown fig.4. The read and write operations are done using address-pointer which is operated with two serially connected DFFs. The DFFs are initiated with '10' mode and XNORed for read-write operations. When the values of address pointer and serially connected DFFs are equal then empty flag is set to high. The full flag asserted high when the value of address pointer is equal where as DFFs are not equal. The advanced distributed MMU is incorporated in each NoC therefore implementing 7X7 mesh based 3-D NoC [10]. The 3-D NoC is upgraded structure of 2-D NoC in terms of performance and flexibility and it is shown fig.5. The 3-D NoC composed of typical design parameters which is same as 2-D NoC [11]. The extra ports (up and down) are added to the router apart from the conventional NoC router. A round-robin arbiter is implemented for resolving the arbitration among the ports. The routing controlling unit is responsible for routing algorithm and data switching [12]. A minimal adaptive routing algorithm is used to data transfer between the source port and the destination port. The virtual cut through (VCT) packet switching is used to transfer of data packet from source to destination [13]. The data packet is divided many small packets that is flites and transferred entire data packet virtually [14, 15]. The amount of transferring time of both VCT and wormhole switching same whereas required storage of data packet is very less in VCT thereby reducing data packet latency and data storage also.

IV. RESULTS AND DISCUSSION

In order to support proposed design, the experiments are conducted on Xilinx 14.7 ISE and synthesis results are presented using Vertex-6 FPGA device. The proposed design is analyzed in terms of area utilization (number of slices), latency (delay), power consumption, memory and throughput while implemented on FPGA device. The FPGA is used as end device for VLSI technology because of flexibility and easy to prototype.

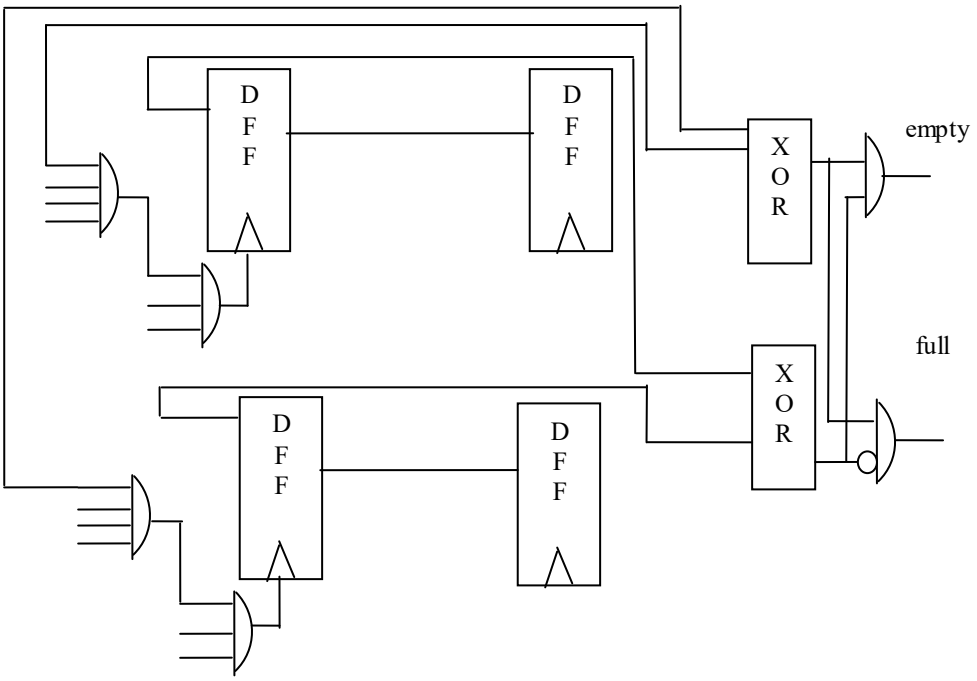

Fig.4 Structure of empty/full circuit

The performance of distributed MMU based NoC is evaluated in terms of area utilization, latency, power consumption and throughput. This work is assumed that each router has equal capability in terms of data packet storage therefore identifying the impact of distributed MMU. Though considering equal capability, obtaining the performance of busy routers is crucially complex.

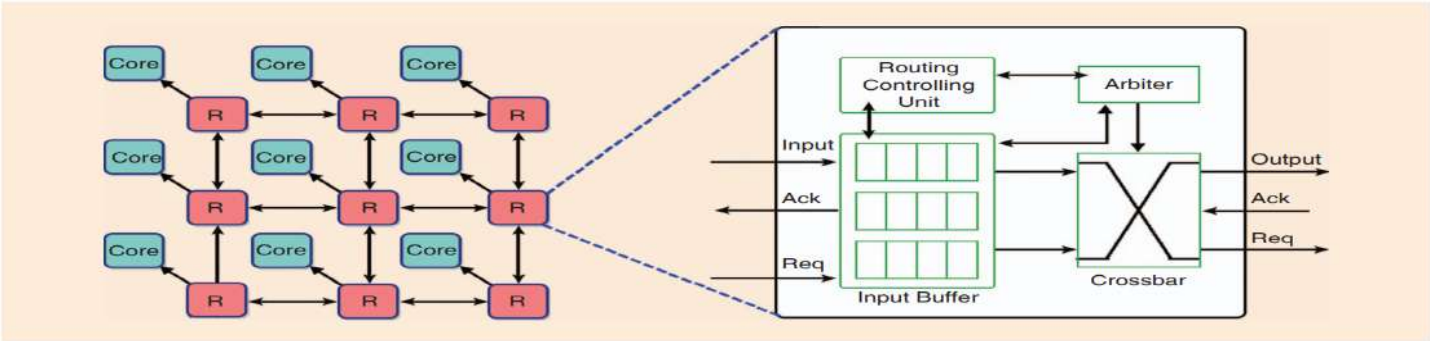

Fig.5 Architecture of 3X3mesh based NoC

The simulation environment to evaluate the performance of distributed MMU based NoC given in Table.1. The other parameters of NoC are considered as same as conventional NoC thereby justifying the comparison.

Table 1 Simulation Environment

Simulation Parameter	Specification
Topology	Mesh
Arbiter	Round-Robin
Crossbar switch	Mux-Demux
Routing Algorithm	Minimal Adaptive
FIFO	Distributed MMU
Packet injection rate	0.01
Packet size	2 flits
Data switching	Virtual cut Through

The simulation results of distributed MMU based NoC router is presented in Fig.6. The empty/full flag is indicated with all possibilities and verified in the simulation. The FIFO is initialized with empty flag and asserted full flag when it is full. The required clock cycles for write lesser than read operation because of verification of write operation requires more clock cycles.

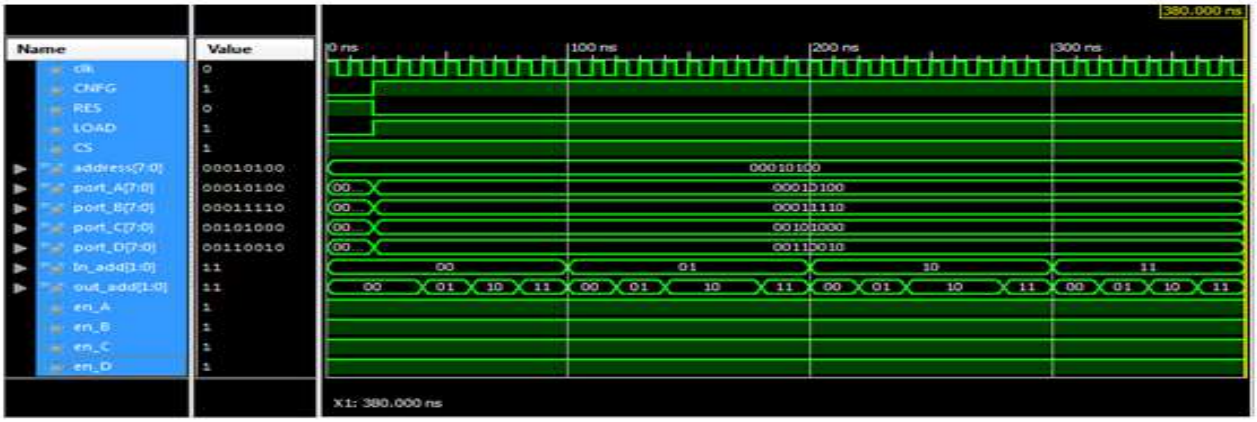

Fig.6 Simulation results of distributed MMU based NoC router

The synthesis results are presented in table.2 in terms of area utilization, latency (delay) and power consumption and storage unit of single NoC router.

Table 2 comparison of different techniques with distributed MMU based NoC

NoC	Resources per PE (LUTs)	Number LUT-FF pairs	Clock frequency (MHz)	Power consumption (mW)	Storage Unit (KB)
RingNet [8]	344	4541	392	15.2	4
One Cycle FIFO [7]	461	3957	565	7.8	2
Distributed MMU based 3-D NOC	390	3582	742	12.7	4

From Table 2, it is inferred that the distributed MMU based 3-D NoC is presented better performance than recent work because of distributed manner of MMU for FIFO based storage and also 3-D structure for NoC. Though the requirement of storage unit of this work and RingNet [8] same but the operating frequency is better because of the empty/full flags that reduces the delay.

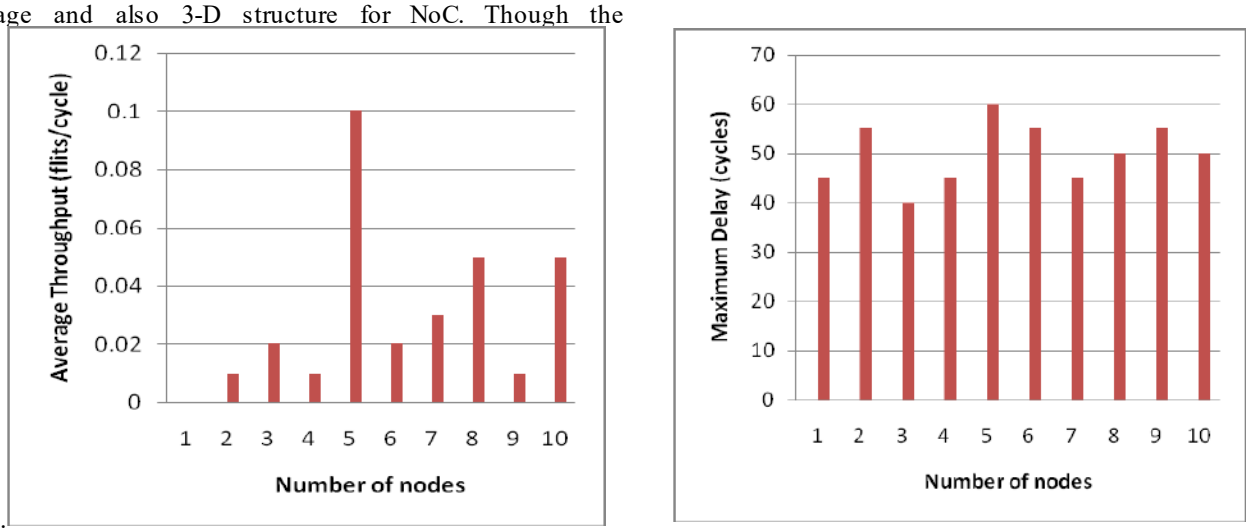

Fig.7 Average throughput and Maximum delay of 3X3 mesh based 3-D NoC

The number of experiments is conducted to obtain exact performance in terms throughput and delay. An average throughput and maximum delay of 3X3 mesh based NoC is presented in fig.7. From figure, it is clear that the average

throughput is constantly increasing whenever less number of distributed MMU is involved. The maximum throughput is presented when no MMU is involved for data transfer same way throughput low when more MMU are involved. The maximum delay is observed when less number of MMUs is used for data transfer.

V. CONCLUSION

This paper presented an advanced Memory Management Unit of FIFO for 3-D NoC based SoC that is distributed MMU based FIFO. The virtual cut through data switching is used to compatible for this work. By taking an advantage of empty/full flags, the distributed MMU is showed more efficient and flexible than recent works. The experimental work proves that advanced distributed MMU based 3-D NoC is showed both throughput and delay are improved when compared with other works.

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Smart College Chatbot using ML and Python

Publisher: IEEE

Hrushikesh Koundinya K. ; Ajay Krishna Palakurthi ; Vaishnavi Putnala ; Ashok Kumar K. All Authors

Abstract: The days of solely engaging with a service through a keyboard are over. Users interact with systems more and more through voice assistants and chatbots. A chatbot is a co... **View more**

Metadata

Abstract:
The days of solely engaging with a service through a keyboard are over. Users interact with systems more and more through voice assistants and chatbots. A chatbot is a computer program that can converse with humans using Artificial Intelligence in messaging platforms. Every time the chatbot gets input from the user, it saves input and response which helps chatbot with little initial knowledge to evolve using gathered responses. With increased responses, precision of the chatbot also gets increases. The ultimate goal of this project is to add a chatbot feature and API for Matrusri Engineering College. This project will investigate how advancements in Artificial Intelligence and Machine Learning technology are being used to improve many services. Specifically it will look at development of chatbots as a channel for information distribution. The program selects the closest matching response from closest matching statement that matches input utilizing WordNet, it then chooses response from known selection of statements for that response. This project aimed to implement online chatbot system to assist users who access college website, using tools that expose Artificial Intelligence methods such as Natural Language Processing, allowing users to communicate with college chatbot using natural language input and to train chatbot using appropriate

Machine Learning methods so it will be able to generate a response. There are numerous applications that are incorporating a human appearance and intending to simulate human dialog, yet in most part of the cases knowledge of chatbot is stored in a database created by a human expert.

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***Abstract*-The days of solely engaging with a service through a keyboard are over. Users interact with systems more and more through voice assistants and chatbots. A chatbot is a computer program that can converse with humans using Artificial Intelligence in messaging platforms. Every time the chatbot gets input from the user, it saves input and response which helps chatbot with little initial knowledge to evolve using gathered responses. With increased responses, precision of the chatbot also gets increases. The ultimate goal of this project is to add a chatbot feature and API for Matrusri Engineering College. This project will investigate how advancements in Artificial Intelligence and Machine Learning technology are being used to improve many services. Specifically it will look at development of chatbots as a channel for information distribution. The program selects the closest matching response from closest matching statement that matches input utilizing WordNet, it then chooses response from known selection of statements for that response. This project aimed to implement online chatbot system to assist users who access college website, using tools that expose Artificial Intelligence methods such as Natural Language Processing, allowing users to communicate with college chatbot using natural language input and to train chatbot using appropriate Machine Learning methods so it will be able to generate a response. There are numerous applications that are incorporating a human appearance and intending to simulate human dialog, yet in most part of the cases knowledge of chatbot is stored in a database created by a human expert.**

***Keywords*- Chatbot; Artificial Intelligence; Machine learning; WordNet; Natural Language Processing**

I. INTRODUCTION

The improvements in the fields of inter-networking and information technology have been intricate in executing an Artificial Intelligent (AI) systems. These systems are drawing nearer of human activities, for example, choice emotionally supportive networks, robotics, natural language processing, and so forth. Indeed, even in the artificial intelligent fields, there are some hybrid strategies and adaptive techniques that make increasingly complex techniques. That, yet these days there are additionally several Natural Language Processing (NLP) [1] and intelligent systems that could comprehend human language. Artificial intelligent systems learn themselves and retrieve insight by perusing required electronic articles that have been existed on the web.

A chatbot (otherwise called a chatterbox, Bot, or Artificial Conversational Entity) is an AI program [2] that copies human discussions including content and communication in natural language utilizing artificial intelligence methods, for example, Natural Language Processing (NLP), picture and video processing, and voice analysis. Chatbot for college management system has been created utilizing artificial intelligence algorithms that examine the user queries. This chatbot system is an internet application that gives an answer to the broken down queries of an user. Users simply need to choose the classification for inquiries and afterward ask the question to the bot that utilizes for noting it. Artificial intelligence has been incorporated to respond to the user's inquiries. Then the user can procure the fitting solutions to their inquiries.

The appropriate responses are given utilizing artificial intelligence algorithms. Users won't need to go actually to the college or college website for requests. Users need to enlist to the system and needs to login to the system. After login users can get to the different helping pages. There will be different helping pages through which users can chat by asking questions related with college activities. The system answers to users' queries with the assistance of effective Graphical User Interface (GUI). The user can question about the college related activities with the assistance of this web application. College related activities, for example, admissions, academics, Intake, and other social activities. It will support the undergraduates/other user to be refreshed about the college activities. A chatbot is an Artificial Intelligence program that can converse with people in natural language, the manner in which we collaborate with one another. It can trade a human for some undertakings of replying inquiries. A chatbot is a specialist that assists users in utilizing natural language. It was worked as an endeavor to trick people. A few uses of chatbots, for example, User care, customer support and so on utilizes Artificial Intelligence Markup Language (AIML) [3] to visit

with users. One of the foremost objectives of chatbots is to take after a smart human and entangle the recipient of the discussion to comprehend the genuine working along with different designs and abilities for their use has generally widened. These chatbots can demonstrate adequate to trick the user to believe that they are "talking" to an individual, however, they are limited in improving their insight base at runtime, and have typically next to zero methods for keeping track of all the discussion information. Chatbots utilize AI to arrive at counterfeit intelligence helping them to comprehend the user question, what's more, give a suitable reaction. The chatbots are created utilizing the Artificial Intelligence Markup Language (AIML) for imparting or cooperating with the user. This comprises software that will be made up of utilizing Artificial Intelligence and will assist the user in chatting with a machine. The user can ask the systems like typically did to other humans.

The remaining of paper as follows: section-II provides literature survey and section-III presents proposed system with methodology. Section-IV propounds results and discussion and finally, section-V concludes the paper.

II. LITERATURE SURVEY

By utilizing the field of Artificial Intelligence, one can develop numerous applications one of that is mentioned in this paper is a college chatbot system. In spite of the fact that chatbot can be deployed in various fields like marketing, education, banking, clinical and finance. Research is being done in making the regular rule based chatbots to be informative, responsive and complete the correspondence in a conversational human language. This requires the incorporation of Natural Language Processing (NLP) and Machine Learning (ML) technologies into the college chatbot system. There are various approaches to do as such. Selecting a fitting technique depends on the area of the chatbot, the functionalities it expects to give, the language of correspondence, the end client, and so forth. Some of the approaches are versed in this literature survey.

Michael Maudlin created "Chatter Bot Algorithm" in 1994 and published in the book Julia and was used to answer the queries. Taking this initial idea, further projects were developed to create a chatbot system. The user need to login to Chat-Bot application. At exactly that point the user is permitted to submit complaints and queries. When user query is submitted to the bot, context of the query is recognized and NLP is applied. WordNet calculation [4] and grammatical forms labeling are utilized to distinguish the feeling of the words. User questions are checked in the knowledge database. If the appropriate response is discovered, at that point that answer is sent to that user. If a particular query isn't found in the database such inquiries are replied by administrator. When the administrator answers the query, at exactly that point the appropriate response is sent to the user. Question alongside answer is put in database so that at whatever point such inquiries will be posed with the intention that they get addressed legitimately from the database. Because of this administrator doesn't have to address same query physically any longer. Different algorithms such as Porter Stemmer Algorithm [5] is used for expelling suffixes from words in English. Word request vector process is used for estimating word request closeness between two sentences. Sentences with precisely same words yet in different order may bring about altogether different meaning. The user is permitted to ask any number of questions with respect to institution. Chatbots after receiving query from user checks confidence [6] score and gives legitimate response to the user question. The keyword match calculation is done where the user inquiry went through 3 keyword matching algorithm [7]. If this matching of keywords fails then at that point query is sent through 2 and 1 keyword matching with the database. Even then if the query doesn't get the right keyword match, at that point the chatbot application sends No Answer Found as a reply.

The utilization of logic adapters to choose a response is another algorithm used for chatbot applications. The aim of an input adapter is to get input from bot source, and then convert it into a format that makes chatbot understand. The chatbot system uses a special logic adapter that allows to pick the fitting response from all the responses. The Multi Logic Adapter is used to choose a single response from the responses returned by all of the logic adapters that the chat bot has been configured to use. Preprocessing of information is done by word embedding. Here each word is mapped to a vector and the vector structure is spoken to in one-hot encoded structure [8] which implies 1 represents the presence of word and 0 for everything else. Natural Language ToolKit (NLTK) is a python library which offers assistance for Natural Language Processing (NLP). NLTK [9] has inbuilt tokenizers. The NLTK incorporates a wide scope of tokenizers which are as per the following norm, letters, path, words, keywords, class, N-gram, pattern and so on. The most usually utilized tokenizer is the word-punkt tokenizer [10] which parts the sentences at the blank spaces. The precision, speed and effectiveness of the NLTK tokenizers is exemplary. Administrator signs in to the portal and can perform activities like erase invalid answer or to include explicit answer of a specific inquiry. With the assistance of computerized reasoning, the chatbot application answers the question asked by the users.

III. PROPOSED SYSTEM

This College Chatbot System is a web based application which gives responses to the user queries. The system architecture of the chatbot system is shown in the Fig. 1. Firstly, Chatbot responds to the user by greeting him/her and then asks user to login into the system by providing his/her mail. Then the user finds the buttons in the UI which corresponds to the different categories of the college. After going through the buttons the chatbot system asks the user, is it helpful in giving the response. If the user is not able to find the required response he/she can continue the chat with the college chatbot system by briefly elaborating their queries. Then chatbot system applies Machine Learning algorithms to the break down the user queries.

Once the user asks query, the keywords in the query is detected using WorldNet Algorithm. As the query description can change from one person to another person. The same query may be asked in a different ways by the users. One user asks a query so simply and clearly while another user may request same query in a completely different manner. So it is required to find what is the exact information user seeks to know and to find a correct response for the corresponding user query. The chatbot system firstly removes the stop words from the user input, if they are present in the queries asked by the user. After removing the stop words from the user queries, tokenization and lemmatization [11] process are done.

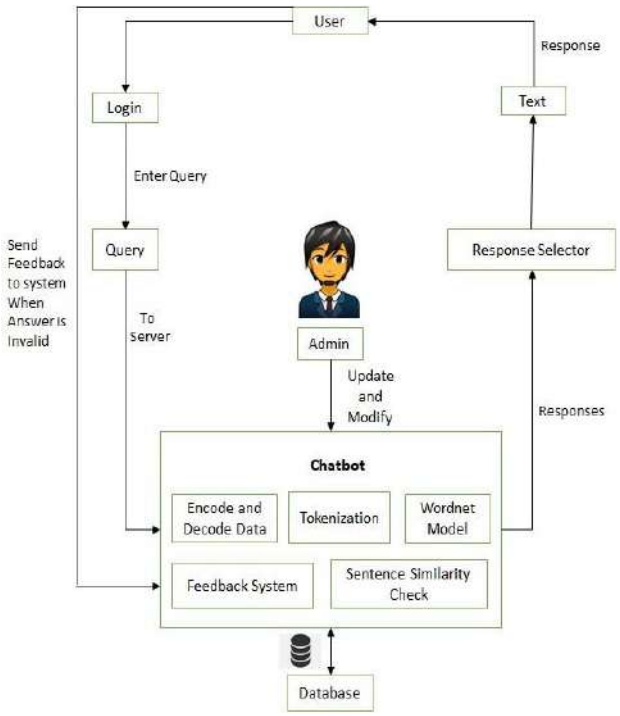

Fig. 1. College Chatbot system architecture

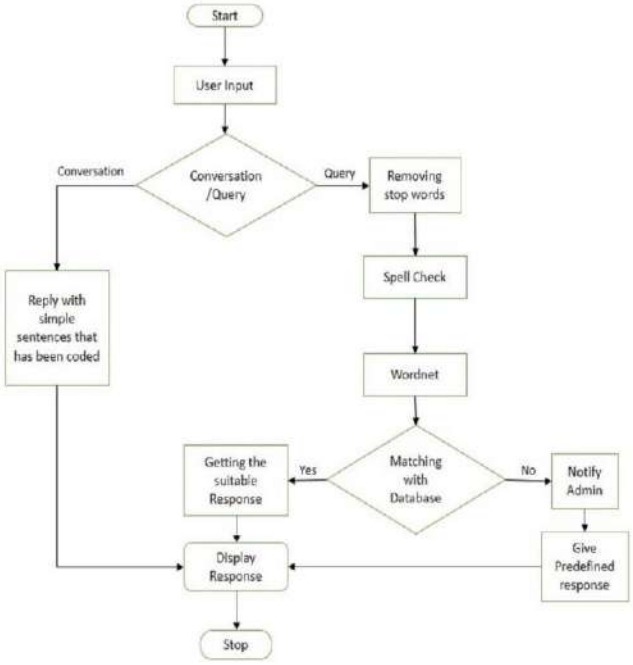

Fig. 2. Flowchart for User Module

Tokenization is a process of taking a set of text or text and breaking it up into its individual words or sentences. Lemmatization is the process of gathering the different inflected forms of a word so they can be dissected as a solitary item and is a variation of stemming. From there spell checker [12] is used to identify and rectify spelling mistakes present in the query, then by using the sentence similarity and WordNet Algorithm [13] a suitable response is explored in the knowledge database [14]. WorldNet is a semantic and lexical database for the English language. It is used to group English words into the set of synonyms called synsets [15], it gives short definitions and utilization models, and records various relations among these synonym sets or their individuals. If the response is found in the database it is displayed to the user, else the system notifies the admin about missing response in the database and gives a predefined response to the user. Admin can write the missing response into the database by logging into the admin block in website so that if the user asks the same query next time, he/she may get the suitable response. At the end of conversation the college chatbot system collects the feedback from users to improve the system efficiency.

The functions of the user are to ask queries, provide feedback and so on. All the functions to be performed by the user are outlined below in detail as shown in Fig. 2.

a. Login: After clicking on the chatbot provided in the college website. The chatbot system greets the user and requests the user to provide the mail id. After which the chatbot starts chatting with the user.

b. Botindex: When the user proceeds to choose chatbot to get an answer to his/her query, the chatbot displays a page to select few options regarding college and identifies his/her category of query. If the user gets his query cleared then the task of chatbot is completed.

c. Asking Queries: If the user is not satisfied with rule based response, then the chatbot system requests to enter his/her query in words and the suitable response is given by the chatbot. User's query is first checked in database. If the query is valid then suitable response is given to the user. If the query is invalid then chatbot requests user to ask queries regarding the college.

d. Providing feedback: After the chat, the chatbot takes feedback from the user. Feedback is taken in order to know the users experience with the chatbot. If the user gives feedback positively then the bot thanks the user and provides a box to enter any further queries. If the user gives feedback negatively then bot asks the user to elaborate his/her query in order to respond. Username of the user is also stored and helps admin to track user actions.

At the other end, admin who is responsible for maintaining the college chatbot system up to date has several functions to perform such as add the query to the database, modify the data, delete the data, and view feedback given by user and so on. All the functions to be performed by the admin are outlined below in detail as shown in Fig. 3.

a. Login: System has only one admin (there is no registration for admin). Admin has to login by providing his/her username and password entered password is encrypted using SHA-256 Encryption algorithm. The login details are validated against the username and password which are stored in the database and are encrypted using SHA-1 Encryption algorithm. If the details provided are matching with the database then the admin can get the access of college chatbot system.

b. Add query: If admin proceeds to add dataset, then the chatbot allows to add the query in three options that is addition of question, addition of answer and selecting the respective category into which dataset is added.

c. View dataset: If admin proceeds to view dataset, then the chatbot allows to view the dataset category wise. The chatbot also gives an additional two options that is delete the dataset and modify the dataset.

d. Delete query: If admin proceeds to delete query, then the chatbot allows to delete the query from view page itself by selecting respective category.

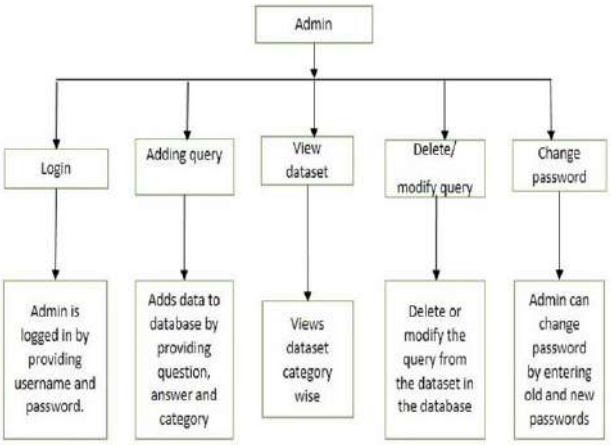

Fig. 3. Flowchart for Admin Module

e. Modify query: If admin proceeds to modify existing query, then the chatbot allows to modify the query from view page itself by selecting respective category.

f. Change password: If admin wants to change the password, then the chatbot allows to change the password. To change the password, admin must provide old password, new password and re-enter the new password in the change password webpage. Thus creating a new password which is encrypted and stored in the code.

g. Viewing invalid dataset: If admin proceeds to view invalid dataset, then the chatbot allows to view the dataset category wise. The invalid data is the data which the user has given negative feedback or the queries for which the chatbot is unable to respond. The chatbot also gives an additional two options that is delete and modify corresponding query.

h. Edit Static answers: The text displayed when user selects buttons in GUI of the chatbot system can be updated or modified by the admin. The admin can update the information which is obtained by selecting the button in the webpage or can change the function of the button by rewriting it in the database.

All the functions permit the administrator to perform any action through the website without going through the database.

IV. RESULTS AND DISCUSSION

Chatbot system is implemented to meet academic requirements of the users. Simulation or Generating response from a chatbot is a knowledge-based one. Wordnet is responsible for retrieving the responses and in this case, it contains all logics that is triggered whenever the user context is matched. When a user begins asking queries in the chatbot Graphical Use Interface (GUI). The query is searched in the database. If the response is found in the database it is displayed to the user else the system notifies the admin about the missing response in the database and gives a predefined response to the user.

Admin can write the missing response into the database by logging into the admin block in website. The chatbot is based on AIML language which is type of Extensible Markup Language (XML). This helps the different type of user to get the information like latest news, university rank holders, timetables, updates regarding college exams and activities and other academic information. Some pictures of the proposed chatbot system is shown in Fig.4, 5 and 6 respectively. By giving choices users can discover their answers in a single click.

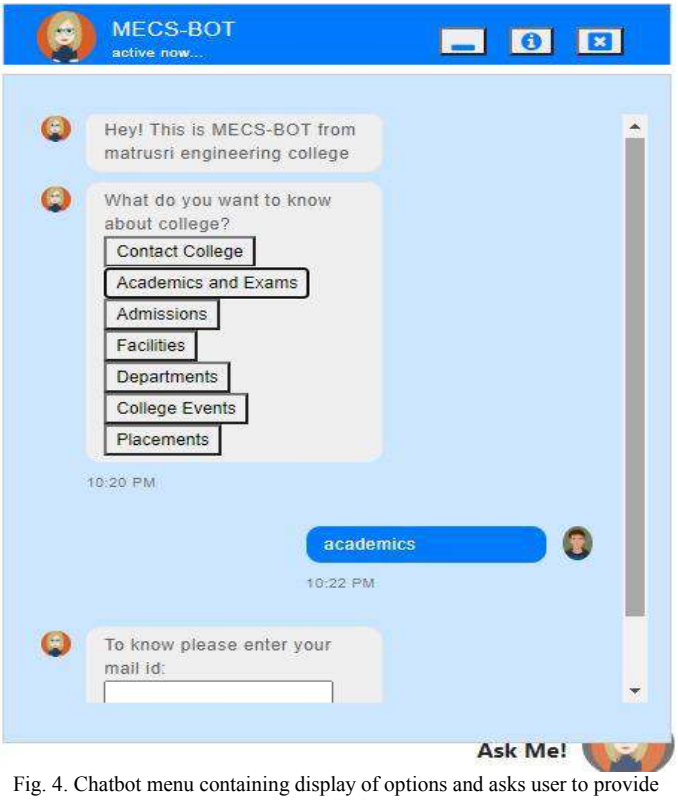

Fig. 4. Chatbot menu containing display of options and asks user to provide mail id

As soon as user chooses a particular category, the chatbot collects user mail id. If the users query is not solved by options then chatbot system gives additional dialogue box to write his/her question regarding college. User can ask any number of queries to chatbot system regarding college. Some sample queries asked by the user are shown in Fig. 5. Chatbot system answers all the queries of users without any delay.

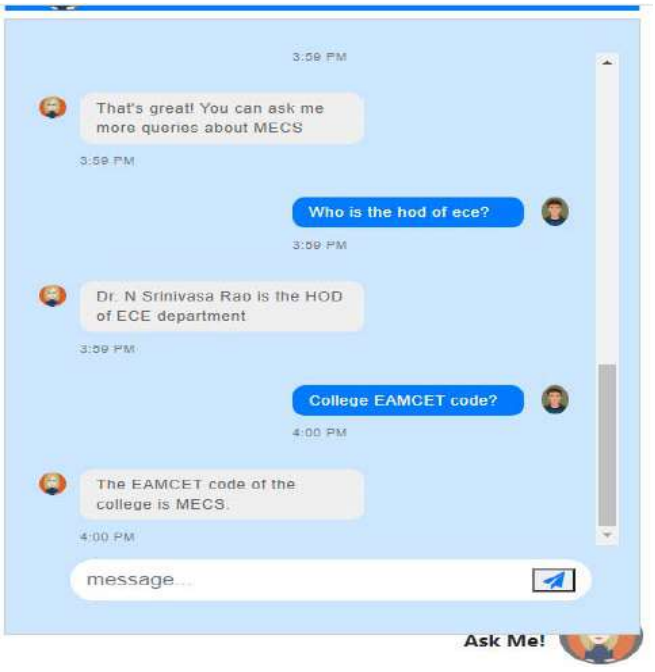

Fig. 5. Chatbot answering queries of users

After the chat, chatbot system asks user to provide feedback as shown in Fig. 6. This feedback system is employed to know whether the user is satisfied with the

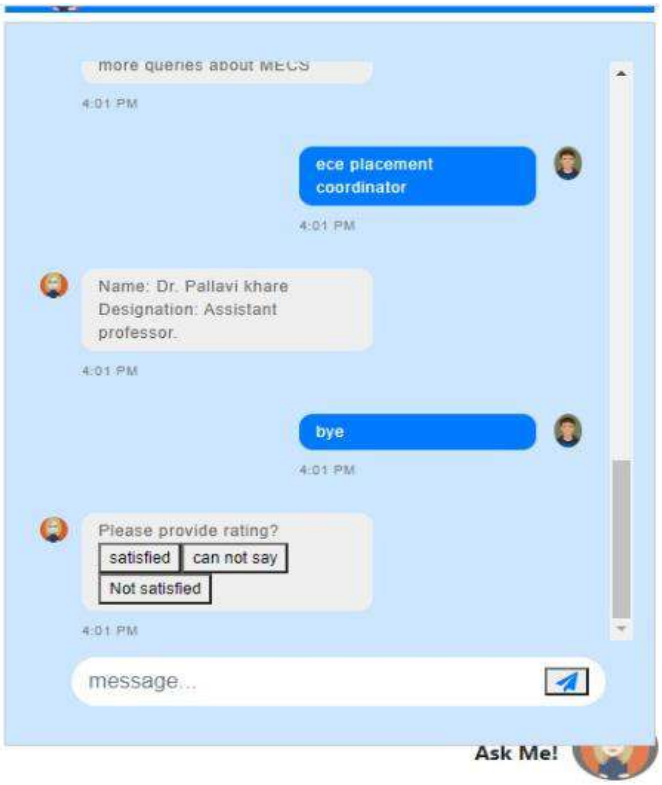

Fig. 6. Feedback System

chatbot response to the user queries. This feedback is stored in the database which can be used by college to know how efficiently chatbot is answering user queries.

Admin need to provide username and password in order to login. Only with proper authentication, admin is allowed to go into the database. After admin provides proper username and password, admin gets logged into admin menu page as shown in Fig. 7. Where admin can perform operations such as add data to dataset, modify the existing data set, view all invalid queries, edit the predefined data, view user feedback, delete the existing data and change password of admin module. All the changes made here are directly changed in database.

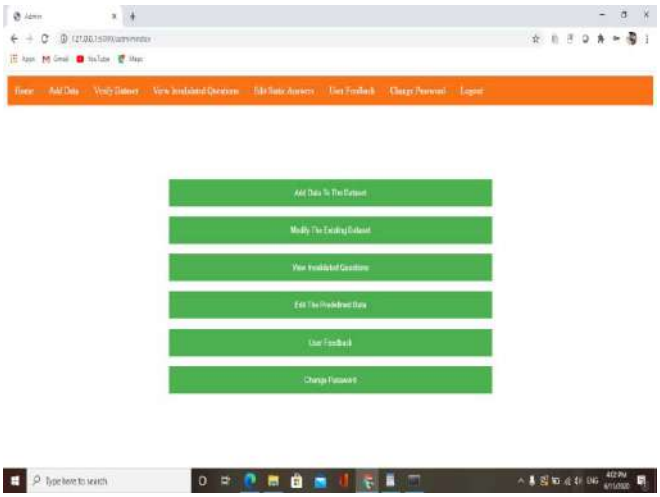

Fig. 7. Admin menu page

If the user is not satisfied with the chatbot responses then he/she gives negative feedback. If admin finds the questions to be valid then admin can add answer to the particular query. If not then admin can delete the question, just by a single click.

V. CONCLUSION

In this project we made a college specific chatbot system that can be custom fitted to education domain chatbot, the addition of this chatbot system in the college website will make the webpage more user interactive as it responds to the user queries very accurately as it is a domain specific chatbot system, and furthermore we had investigated our college chatbot system design stages and a few different techniques by which the precision of the chatbot system can be made much better. To make the responses given by the chatbot system more meaningful and accurate the administrator has to train the chatbot system with more information regarding to college and increase the scope of knowledge base. Nevertheless, gathering feedback from the potential user can be helpful in developing the college Chatbot system, ultimately servicing the user queries.

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Advanced Memory Management Unit for 3-D Network on Chip

Publisher: IEEE

Kumar K. Ashok ; V. Karunakar Reddy All Authors

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Contents

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Network on Chip (NoC) is one of the optimized solutions for issues of intercommunication in System on Chip (SoC). As technology improves, a lot of improves observed at architecture of NoC that is 3-D NoC. To improve the performance of SoC, number of Processing Elements (PE) are added to the single die. The PEs is connected vertically and horizontally in 3-D NoC thereby achieving higher performance than 2-D NoC within same die. PEs are able communicate data among them in case of heavy traffic thereby reducing the latency and power consumption. Memory is the critical problem when PEs is active or idle during data transmission from source to destination. Hence, highlighting the memory management block during data packet transfer will avoid the performance degradation. Conventionally, NoC is composed with number of routers and PEs to obtain parallel communication among PEs [1]. The router is a unit which realizes with number of input and output ports and also crossbar switch. Arbiter is used to resolve arbitration among the ports with efficient scheduling algorithms [2]. Each port is realized with memory unit to store the data packet and its controller unit to control data transfer. Typically, First in First out (FIFO) is used as memory management unit and the size of FIFO depends on the size of data packet because of easy to implement data transfer operations. However, FIFO has several disadvantages like synchronization and also depth of queue leads to penalty in terms of both latency and energy. According to Moore's law, the number of devices on single die is double for every eighteen months. Hence, designing of low latency and power efficient chip is critically complex As computational power consumption is exponentially increases than dynamic power consumption, hardware efficient processor is preferred to trade off between performance and power consumption thereby spreading the tasks to the multiple PEs. An individual PE is to off/on when it is idle and also run its own with optimized supply voltage to save power consumption. A one of the fundamental problems lies in SoC is memory management unit because of optimized data transfer from and to memory interface devices. In future, using of memory management units in NoC is not only increases delay but also rises the issues in terms of scalability and portability. The memory units are critically complex in NoC based SoC designs because of it is increased in number and also distributed in nature. Fig. 1 shows typical memory management unit for entire PE in SoC design which is shared memory interface unit. The shared memory interface unit is used to data transfer in general purpose PE in the FPGA based multiprocessor system. The shared memory architecture is also known as Connected RAM (CoRAM) which is capable of reconfigurable both standalone and heterogeneous fabric. The reconfigurable logic is existed from and to storing of data through memory interface units in NoC with boundaries of linear address. The implementation of CoRAM is simple which is made up of wire level SRAM thereby distributing spatially to obtain higher bandwidth than conventional designs. However, data packet of each CoRAM is controlled by FSM controller thereby deviating drastically. In any SoC fabric, the operation of FIFO is executed using shift register where requirement of storage is limited otherwise embedded RAM is utilized for large requirements. The typical

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Advanced Memory Management Unit for 3-D Network on Chip

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***Abstract*—Future generation chip multiprocessor (CMP) contains thousands of cores to increase performance the system. Network on Chip (NoC) is new paradigm for the intercommunication of System on Chip (SoC). 3-D NoC is the new way of improvement in NoC fabric to achieve high performance. One of major drawbacks of NoC is memory unit and it is proportionally increases in 3-D NoC. A first in first out (FIFO) is conventionally placed in NoC router to store data packet temporarily. The memory is critical issue for NoC based SoC because of size and cost of device. Advanced memory architecture presented to optimize the performance of NoC router. This paper proposes a random access memory (RAM), which is a bridge between input ports and crossbar switch. This technique is simulated in Xilinx 14.7 ISE and implemented in Vertex-6 FPGA device.**

Keywords— ***Memory Management Unit; FIFO; NoC; SoC; FPGA***

I. INTRODUCTION

Network on Chip (NoC) is one of the optimized solutions for issues of intercommunication in System on Chip (SoC). As technology improves, a lot of improves observed at architecture of NoC that is 3-D NoC. To improve the performance of SoC, number of Processing Elements (PE) are added to the single die. The PEs is connected vertically and horizontally in 3-D NoC thereby achieving higher performance than 2-D NoC within same die. PEs are able communicate data among them in case of heavy traffic thereby reducing the latency and power consumption. Memory is the critical problem when PEs is active or idle during data transmission from source to destination. Hence, highlighting the memory management block during data packet transfer will avoid the performance degradation. Conventionally, NoC is composed with number of routers and PEs to obtain parallel communication among PEs [1]. The router is a unit which realizes with number of input and output ports and also crossbar switch. Arbiter is used to resolve arbitration among the ports with efficient scheduling algorithms [2]. Each port is realized with memory unit to store the data packet and its controller unit to control data transfer. Typically, First in First out (FIFO) is used as memory management unit and the size of FIFO depends on the size of data packet because of easy to implement data transfer operations. However, FIFO has several disadvantages like synchronization and also depth of queue leads to penalty in terms of both latency and energy. According to Moore's law, the number of devices on single die is double for every eighteen months. Hence, designing of low latency and power efficient chip is critically complex. As computational power consumption is exponentially increases than dynamic power consumption, hardware efficient processor is preferred to trade off between performance and power consumption thereby spreading the tasks to the multiple PEs. An individual PE is to off/on when it is idle and also run its own with optimized supply voltage to save power consumption. A one of the fundamental problems lies in SoC is memory management unit because of optimized data transfer from and to memory interface devices. In future, using of memory management units in NoC is not only increases delay but also rises the issues in terms of scalability and portability. The memory units are critically complex in NoC based SoC designs because of it is increased in number and also distributed in nature. Fig.1 shows typical memory management unit for entire PE in SoC design which is shared memory interface unit. The shared memory interface unit is used to data transfer in general purpose PE in the FPGA based multiprocessor system. The shared memory architecture is also known as Connected RAM (CoRAM) which is capable of reconfigurable both standalone and heterogeneous fabric. The reconfigurable logic is existed from and to storing of data through memory interface units in NoC with boundaries of linear address. The implementation of CoRAM is simple which is made up of wire level SRAM thereby distributing spatially to obtain higher bandwidth than conventional designs. However, data packet of each CoRAM is controlled by FSM controller thereby deviating drastically. In any SoC fabric, the operation of FIFO is executed using shift register where requirement of storage is limited otherwise embedded RAM is utilized for large requirements. The typical FIFO composed as three stages: Address pointer stage, Address decoder stage and isolate stage. The address pointer stage produces address pointers to trace out data and the address decoder stage originates the word line of memory. The isolate stage separates remaining two stages therefore achieving the power efficient design. One of the major drawbacks of typical memory management unit is requiring large number of registers for isolating and increase in number to ensure accurate memory. Another important drawback is controlling the delay in address decoder stage with compensation circuit.

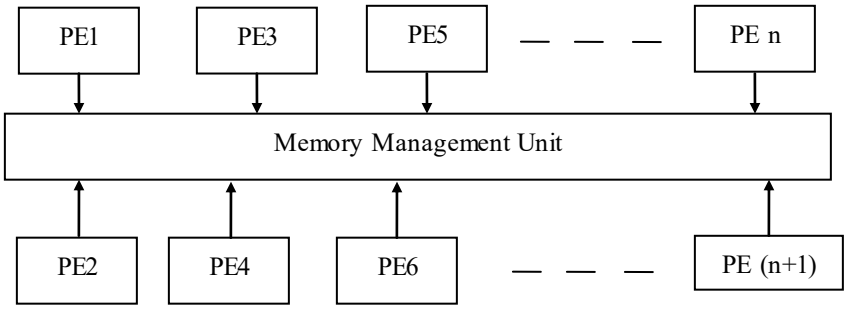

Fig.1 Shared memory architecture for FPGA based Multiprocessor

Considering above drawbacks, this paper is focusing mainly on the static memory management units especially on FIFO designs. In order to obtain high performance, the buffer is implemented with distributed manner with virtual cut through packet switching. The remaining paper discussed as follows: section-II presented related work and section-III explained the distributed MMU architecture and also presented the improved design of NoC fabric. Section-IV propounded results and discussion and finally, section-V concludes the paper.

II. Related Work

3-D NoC is one of major improvements in the NoC based SoC fabric to achieve high performance. Memory Management Unit (MMU) plays an important role for managing FIFO based buffer of each port. Shibata et. al. [3] proposed a new architecture to reduce power consumption in terms of address pointer of shift registers. A swapped two-port memory cell with bit line/word line configuration is proposed to obtain low power and high speed. The experimental results are proven that the speed of operation is massively increased. However, the power consumption is also increased at higher operating frequencies. Chen, X [4] propounded a shred memory with microcoded controller to the hardware module thereby connecting each node to the memory module or core of the network. The microcode is the one of the oldest technology to compensate both performance and flexibility of the network. Hence, the dual microcoded controller is proposed to utilize various functions efficiently. The DMC has mainly two processors which are able to handle the requests from local PE and also remote PE of the network. Though the DMC provided efficient delay and optimized solution for hardware, still flexibility of DMC in network is complex problem. To provide bridge between internal FIFO and external memory modules, Chung et. al. [5] proposed a connected RAM (CoRAM). In addition to bridge, the CoRAM structure provides virtualized memory units for obtaining improved efficiency and performance. The CoRAM is composed with reconfigurable logic which is integrated with LUT based modules to access of virtual address space. The experimental results are proven that the CoRAM is presented high performance, low power consumption and less area utilization. However, it increases the design time and also raises the issues in scalability and portability. To support ultra low power (ULP) processors, Jang et.al. [6] proposed memory management unit with embedded NoC (MMNOC). Due to area, latency and power, integrating typical MMU to NoC is complex. Therefore isolating MMU from hardware and integrating to local PE of source router. Hence, providing a direction to the researchers to embedded MMU to lightweight ULP processors. The simulation results are shown that the almost 50% required gate count of core interface is reduced than Microcoded controller [4]. Because of dual processors involved in MMNOC, the chip area utilization and power consumption is overhead than recent designs. Gordon-Ross et. al. [7] proposed an efficient structure of synchronous FIFO to enhance the memory management in NoC based systems. The synchronous FIFO design uses two phase clock that avoids the race around condition between the data operation and addresses. It incorporates advantages of two port SRAM memory cell to improve speed of data operations. This design simplifies the circuit which uses empty/full flag to record of maximum address of FIFO. The results are presented that the speed of data operation is highly increased and power consumption is reduced. Though, there is problem for optimizing of performance and flexibility. To optimize utilizations of resources, Siast et.al. [8] presented a new scheme that is RingNet. The RingNet uses a distinctive feature that is data operations are conducted on centrally placed memory which supports preventing of data congestions thereby requiring less network buffer for NoC fabric. The design of RingNet exhibits two different properties which are responsible for controlling of the traffic and also data communication through the FIFO buffers of the system. The RingNet provides low cost and lower resource utilization because of resources is shared among the PEs. Therefore, utilization of resources is proportional to the number of PEs involved in the data operation. Apart this, the However, the system latency is increased because of centrally placed memory.

From the literature, memory management unit is plays vital role in NoC based SoC and it critically important to achieve high performance. This paper has proposed the distributed memory management unit in place centrally located memory. These distributed MMU is supported virtual address space therefore compatible for less resource utilization. To optimize performance and flexibility, NoC is proposed with virtual cut through packet switching.

III. DISTRIBUTED MMU ARCHITECTURE

A design of central located memory unit and implementation for NoC is simple therefore most of the designs are composed with it [9]. However, it is not suitable for the future generations therefore this paper proposes distributed memory units. Fig.2 shows structure of the centralized MMU where entire PEs are connected with centralized memory.

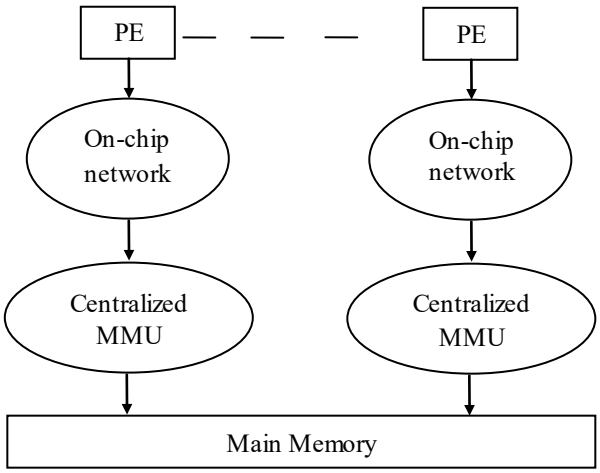

Fig.2 Structure of centralized Memory Management Unit

The problem of centralized MMU is higher network latency because of too many requests are hitting the main memory and also on-chip network which is placed between PE and centralized memory is another major issue thereby raising issues with scalability. To prevent these bottlenecks and to handle memory access requests in NoC, this paper proposes the distributed MMU which requires more number of MMUs. With proper placement of MMUs, improved NoC is showed the high bandwidth utilization and less traffic.

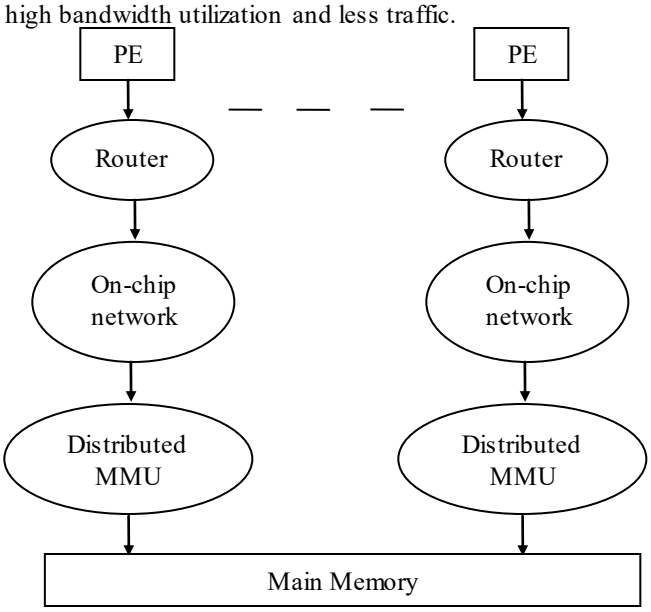

Fig. 3 Structure of Distributed MMU

Fig. 3 shows the structure of distributed MMU which accesses the memory request separately through virtual address. The PE requests main memory channel through distributed MMU based on routing tables. These routing tables are updated every clock cycle thereby assigning request to the idle MMU. The current router is controlled the memory request and its distributed MMU thereby accessing main memory in case of availability otherwise assigning to another MMU. This paper considers 7X7 mesh based 3-D NoC therefore requiring 6-memory channels to access main memory for the entire network. Each distributed MMU is dedicated to memory request of respective PE and in case unavailability or overloaded, assigning to another dedicated MMU. When MMU receives a request to access memory, it decodes the address and give the access if it is available therefore injects the data packets into the network. A one bit flag is set once the request is closed otherwise the flag reset which is not shown figure. The empty/full flag bit detects reads and write operation using D-flip flop (DFF) circuitry which is connected serially.

The structure of empty/full flag is as shown fig.4. The read and write operations are done using address-pointer which is operated with two serially connected DFFs. The DFFs are initiated with '10' mode and XNORed for read-write operations. When the values of address pointer and serially connected DFFs are equal then empty flag is set to high. The full flag asserted high when the value of address pointer is equal where as DFFs are not equal. The advanced distributed MMU is incorporated in each NoC therefore implementing 7X7 mesh based 3-D NoC [10]. The 3-D NoC is upgraded structure of 2-D NoC in terms of performance and flexibility and it is shown fig.5. The 3-D NoC composed of typical design parameters which is same as 2-D NoC [11]. The extra ports (up and down) are added to the router apart from the conventional NoC router. A round-robin arbiter is implemented for resolving the arbitration among the ports. The routing controlling unit is responsible for routing algorithm and data switching [12]. A minimal adaptive routing algorithm is used to data transfer between the source port and the destination port. The virtual cut through (VCT) packet switching is used to transfer of data packet from source to destination [13]. The data packet is divided many small packets that is flites and transferred entire data packet virtually [14, 15]. The amount of transferring time of both VCT and wormhole switching same whereas required storage of data packet is very less in VCT thereby reducing data packet latency and data storage also.

IV. RESULTS AND DISCUSSION

In order to support proposed design, the experiments are conducted on Xilinx 14.7 ISE and synthesis results are presented using Vertex-6 FPGA device. The proposed design is analyzed in terms of area utilization (number of slices), latency (delay), power consumption, memory and throughput while implemented on FPGA device. The FPGA is used as end device for VLSI technology because of flexibility and easy to prototype.

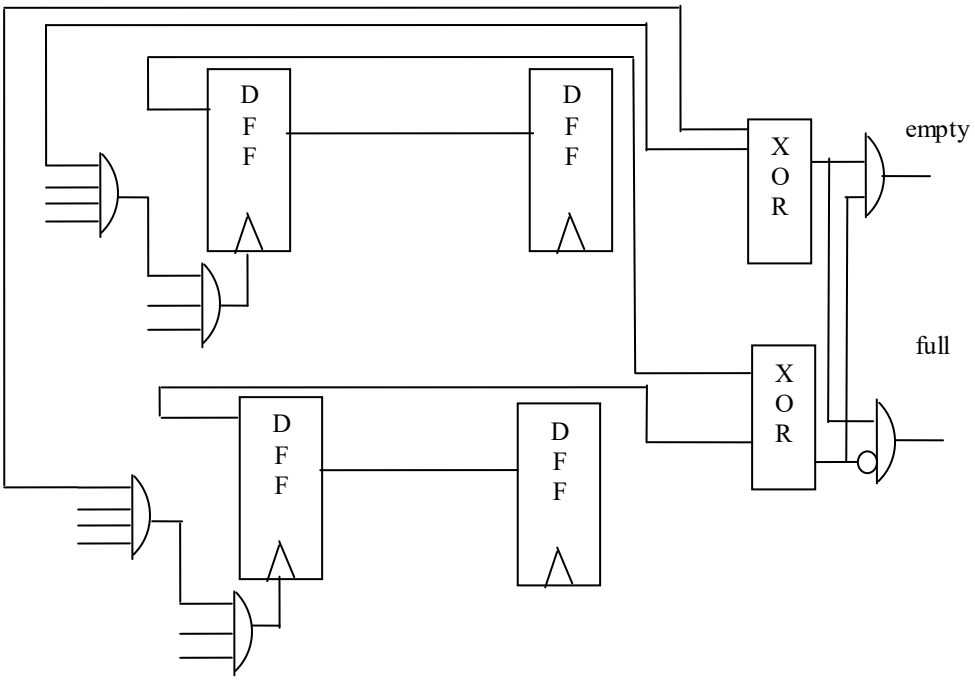

Fig.4 Structure of empty/full circuit

The performance of distributed MMU based NoC is evaluated in terms of area utilization, latency, power consumption and throughput. This work is assumed that each router has equal capability in terms of data packet storage therefore identifying the impact of distributed MMU. Though considering equal capability, obtaining the performance of busy routers is crucially complex.

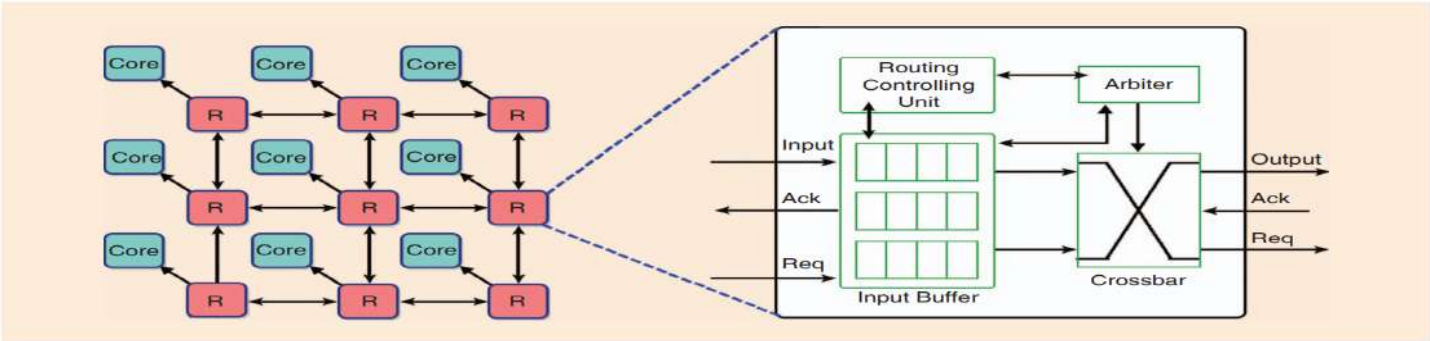

Fig.5 Architecture of 3X3mesh based NoC

The simulation environment to evaluate the performance of distributed MMU based NoC given in Table.1. The other parameters of NoC are considered as same as conventional NoC thereby justifying the comparison.

Table 1 Simulation Environment

Simulation Parameter	Specification
Topology	Mesh
Arbiter	Round-Robin
Crossbar switch	Mux-Demux
Routing Algorithm	Minimal Adaptive
FIFO	Distributed MMU
Packet injection rate	0.01
Packet size	2 flits
Data switching	Virtual cut Through

The simulation results of distributed MMU based NoC router is presented in Fig.6. The empty/full flag is indicated with all possibilities and verified in the simulation. The FIFO is initialized with empty flag and asserted full flag when it is full. The required clock cycles for write lesser than read operation because of verification of write operation requires more clock cycles.

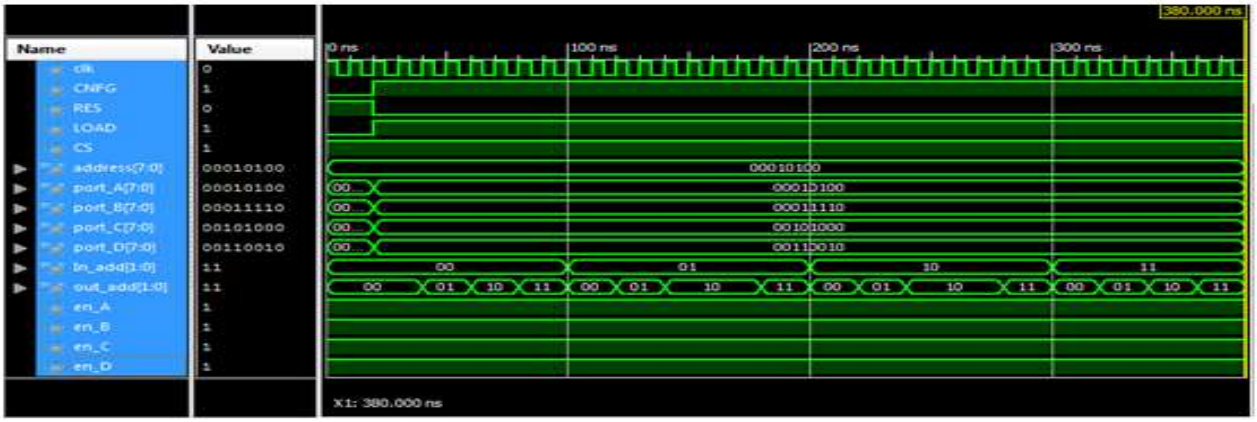

Fig.6 Simulation results of distributed MMU based NoC router

The synthesis results are presented in table.2 in terms of area utilization, latency (delay) and power consumption and storage unit of single NoC router.

Table 2 comparison of different techniques with distributed MMU based NoC

NoC	Resources per PE (LUTs)	Number LUT-FF pairs	Clock frequency (MHz)	Power consumption (mW)	Storage Unit (KB)
RingNet [8]	344	4541	392	15.2	4
One Cycle FIFO [7]	461	3957	565	7.8	2
Distributed MMU based 3-D NOC	390	3582	742	12.7	4

From Table 2, it is inferred that the distributed MMU based 3-D NoC is presented better performance than recent work because of distributed manner of MMU for FIFO based storage and also 3-D structure for NoC. Though the requirement of storage unit of this work and RingNet [8] same but the operating frequency is better because of the empty/full flags that reduces the delay.

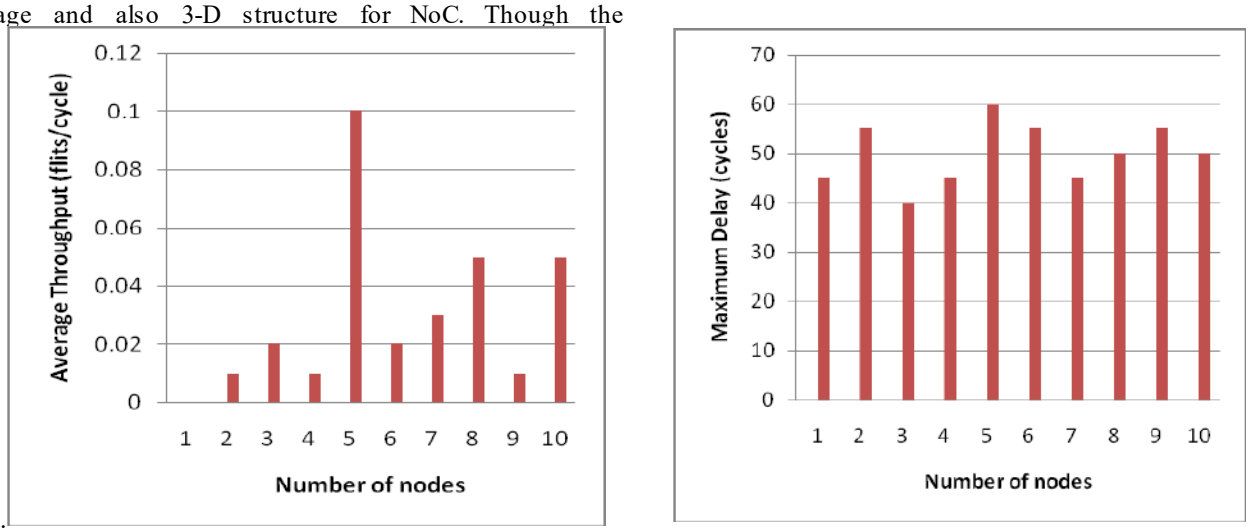

Fig.7 Average throughput and Maximum delay of 3X3 mesh based 3-D NoC

The number of experiments is conducted to obtain exact performance in terms throughput and delay. An average throughput and maximum delay of 3X3 mesh based NoC is presented in fig.7. From figure, it is clear that the average

throughput is constantly increasing whenever less number of distributed MMU is involved. The maximum throughput is presented when no MMU is involved for data transfer same way throughput low when more MMU are involved. The maximum delay is observed when less number of MMUs is used for data transfer.

V. CONCLUSION

This paper presented an advanced Memory Management Unit of FIFO for 3-D NoC based SoC that is distributed MMU based FIFO. The virtual cut through data switching is used to compatible for this work. By taking an advantage of empty/full flags, the distributed MMU is showed more efficient and flexible than recent works. The experimental work proves that advanced distributed MMU based 3-D NoC is showed both throughput and delay are improved when compared with other works.

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Implementation of the Standard Floating Point DWT Using IEEE 754 Floating Point MAC

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Abstract

This work concentrates mainly for the implementation of Standard DWT using IEEE 754 floating point format. Currently, in the signal processing, for audio purpose the fixed point DWT is used as audio CODEC [1]. The main bottleneck of the fixed point

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Implementation of the Standard Floating Point DWT Using IEEE 754 Floating Point MAC

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Abstract. This work concentrates mainly for the implementation of Standard DWT using IEEE 754 floating point format. Currently, in the signal processing, for audio purpose the fixed point DWT is used as audio CODEC [1]. The main bottleneck of the fixed point DWT or the traditional DWT is the speed because at the input of the fixed point DWT the over-sampled ADC which is the Sigma-Delta ADC is used. The Sigma-Delta ADC can't give the speed more than 1 MHz because as the sampling rate increases, the step size decreases so that it takes more time to follow the analog signal which causes the limitation of the speed. Due to the speed limitation of ADC, the whole audio CODEC system which was designed by the fixed point DWT becomes slow even it has the capability to operate with a better speed. Hence, to optimize the system the FIR filters which are used to constitute the standard floating point DWT have been implemented in VLSI.

Keywords: DWT · IEEE 754 floating point · Audio CODEC · Sigma-Delta ADC

1 Introduction

To overcome the limitation of the speed of Sigma-Delta ADC, it has to be replaced by the logical connection instead of the physically connected Sigma-Delta ADC between the audio source and the fixed point DWT. The logical connection is provided through the development of user defined float point package using IEEE 754 standard and compile with IEEE standard library of digitally define tool. DWT designed in this manner is called Standard floating point DWT. To such floating point DWT, the audio source which is in the form of analog is converted into IEEE 754 standard and applied at the input using a test-bench. This floating point DWT be designed with floating point FIR filters. The floating point FIR filters are designed by floating point MAC [1]. Such MAC is designed by the floating point adder and floating point multiplier along with shifter. These floating point arithmetic operators are designed by the user defined

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floating point library package [2]. With all such topics, this chapter explains the complete implementation issues of the Standard floating point DWT using IEEE 754 format. At the end of the work, various results of the standard floating point DWT are also illustrated.

2 Traditional 3-Stage DWT and Its Limitations

Traditional fixed point DWT functions with fixed-point MAC and its MAC has been designed through fixed point adder and multiplier along with a shifter. Because, it operates along with the sigma-delta analog to digital converter and digital to analog converter at the input side and output side of the fixed point DWT correspondingly, the first drawback of the traditional DWT is speed [3]. The sigma-delta analog to digital converter is used to alter the analog signal to the digital signal. Sigma-delta operates with oversampling rate which means that the sampling rate is more than twice to that of the maximum frequency component of the signal. When it is oversampled, the number of step sizes are more which will take more time to follow the analog signal. Likewise the speed will be less [4].

The second bottleneck of the traditional DWT is, db4 co-efficients are actually in floating point hence these should be transformed into the fixed point using various scale parameters before and after the computation. At the end the results are scaled down by the same parameter [5], due to which the system may obey the non-linear property and hence there may be a chance to decrease the system stability.

3 Realization of Standard Floating Point DWT for 3 Stage Using Filter Bank Approach

The primary objective of this research is to design the 3-stage floating point audio CODEC using floating point DWT. As the floating point DWT is constituted by the filter bank and it has been implemented by the sub-band coding advance as given in the following sections [6].

3.1 Sub-Band Coding

Sub-band coding can be explained with the successive decomposition of input signal through filter bank. The discrete wavelet transform crumbles a signal to a set of dissimilar resolution sub-signals correspond to the different frequency bands. It results in a multi-resolution representation of signals with localization in both the spatial and frequency domains [7]. It is attractive in the case of signal compression, but it is not possible in the case of Fourier Transform which gives good localization in one domain at the expense of other. Sub-band coding is a process in which the input signal is divided into various frequency bands. The filter bank is a compilation of filters which are having a similar node either at output or input. If filters have a common node (N) at the output, they form the synthesis bank and when they share a common node (N) at the input, they form the analysis bank which is shown in Fig. 1. The fundamental concept of filter bank is divide a signal equally at the frequency domain [8, 9].

3.2 Perfect Reconstruction Filters

The above Fig. 1 shows the two-band analysis cum synthesis filter bank system. In the analysis bank $H_0(z)$ and $H_1(z)$ are the low pass and high pass FIR filters respectively. Similarly, in the synthesis filter bank $F_0(z)$ and $F_1(z)$ are the low pass and high pass FIR filters respectively. From the above Fig. 1 the final output X(Z) is given by

$$\begin{aligned} X(Z) &= 1/2[H_0(Z)F_0(Z) + H_1(Z)F_1(Z)]X(Z) \\ &\quad + 1/2[H_0(-Z)F_0(Z) + H_1(Z)F_1(Z)]X(-Z) \end{aligned} \tag{1}$$

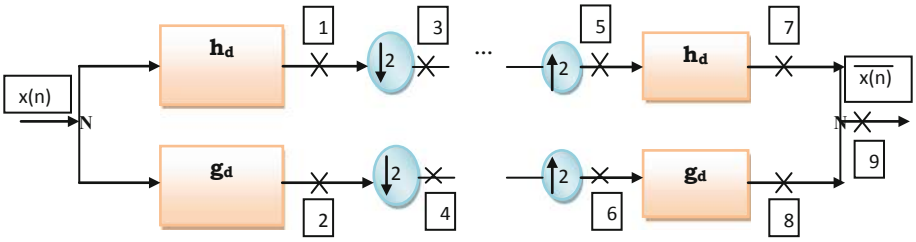

Fig. 1. A two band analysis cum synthesis filter bank system

Alias can be cancelled by choosing the filters such that the quantity in Eq. 6.9, $H_0(-Z)\ F_0(Z) + H_1(-Z)\ F_1(Z)$ is zero [9].

Thus the following choice cancels aliasing.

$$\begin{aligned} F_0(Z) &= H_1(-Z) \\ F_1(Z) &= -H_1(-Z) \end{aligned} \tag{2}$$

For the $H_0\widehat{(z)}$ and $H_1(z)$ it is possible to completely cancel the aliasing by the choice of synthesis filters [10].

In the matrix form expression1 can be written as –

$$z.\ \widehat{x(z)} = [x(z)\ .\ x(-z)\ ] \underbrace{\begin{bmatrix} H0(Z) & H1(Z) \\ H0(-Z) & H1(-Z) \end{bmatrix}}_{H(z) = \text{Alias component matrix}} \begin{bmatrix} F0(Z) \\ F1(Z) \end{bmatrix}$$

The matrix H(Z) is called the aliasing component (A.C) matrix. The term which contains X(−Z) originates because of the decimation. On top of the unit circle, $X(-z) = X\left(e^{j(w-n\square)}\right)$ which is a right shifted version of $X(e^{jw})$ by an amount of $\prod$. This term takes into account aliasing due to the decimators and imaging due to the expanders [11]. It could be referred this just as the alias term or alias component.

3.3 Elimination of Aliasing Effect

When the input signal to the decimator is not band-limited, then the spectrum of decimated signal has aliasing. Hence, the input signal should be band-limited to π/D, where D is the decimator.

3.4 FIR Filters

For the multi-rate signal processing, FIR filters are chosen than IIR filters because

(1) FIR filters are stable
(2) FIR filters can be designed with exactly linear phase
(3) Limit cycles are not produced in the FIR filters since these filters are not having feedback [12].

FIR filters can be designed using three techniques i.e.,

(1) Fourier series technique
(2) Frequency sampling technique
(3) Window technique

Because, in this research Daubechies-4 window which is suitable for audio applications is used, the design of FIR filter using window technique is illustrated here.

3.4.1 FIR Filter Using Window Technique

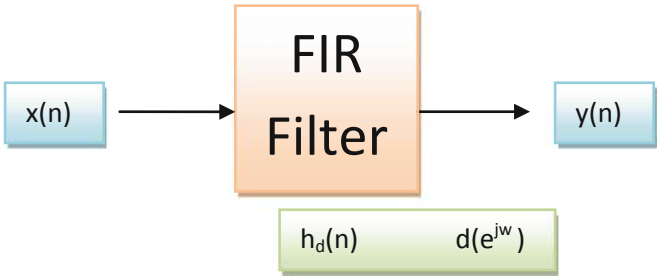

Fig. 2. FIR filter

The above Fig. 2 shows the FIR filter. In Fig. 2

$$\begin{aligned} h_d(n) &= \text{Fourier coefficients having infinite length} \\ &= 1/2\pi \int_{-\pi}^{\pi} H\left(e^{jw}\right) \cdot e^{jwn} dw \end{aligned} \tag{3}$$

$$\begin{aligned} H_d(n) &= \text{Fourier series representation of } h_d(n) \\ &= \sum_{n=-\infty}^{\infty} hd(n) \cdot e^{jw} \end{aligned} \tag{4}$$

3.4.2 Daubechies Wavelet Co-efficients

Because of the 3-stage Standard floating point audio CODEC is to be implemented by DWT using multi-rate analysis, the window size is not fixed which means that analysis is to be done for different frequency bands by the high pass and low pass filters with the different resolutions by the decimators. As the specifications are changed window to window, a superior exercise is required to find the resultant filter co-efficients. After a lot of exercise, Prof. Ingrid Daubechies, had invented the low pass and high pass filter co-efficients for various applications and released for the public domain. It is important to note that the objective of this research is not to introduce the wavelet concepts starting from the scratch, but to present the application of wavelet in the field of signal compression such as in audio applications. But, in general to find the order of the filter (N); the transition frequency (Δf), sampling rate (fs), pass band attenuation ($\square_p$), stop band attenuation ($\square_s$) are required. If the response of the low pass filter is considered with various specifications as given below,

f_s = sampling rate
Δf = transition frequency
$\square_p$ = pass band attenuation
$\square_s$ = stop band attenuation

The order of the filter (N) could be found with the empirical relation as given below:

$$\begin{aligned} &\Delta f_{min} = f_s/N \text{ or} \\ &\Delta f \approx f_s/N * [\text{Atten(db)} - 8]/14 \text{ or} \\ &N = f_s/\Delta f * [\text{Atten(db)} - 8]/14 \end{aligned} \tag{5}$$

There are different mother wavelets like db2, db4 and db6 etc., which are invented by Prof. Ingrid Daubechies and for each one, there is a specific application. Some of the basic wavelets are explained as given below.

db2 Wavelet

db2 wavelet is also called Haar wavelet. It has 2 vanishing movements.

db4 Wavelet

As the name itself, db4 is having the four vanishing movements. It is specified for the audio applications. The filter co-efficients are extracted from the Matlab command as given below:

?[L.H] = orthfilt(dbwavf('db4'))

$$L = -0.1294 \quad 0.2241 \quad 0.8365 \quad 0.4830$$
$$H = -0.4830 \quad 0.8365 \quad -0.2241 \quad -0.1294$$

db6 Wavelet

It has 6 vanishing movements. It is used for C.T scan to identify the tumors by EEG and ECG.

3.4.3 Stage Standard Floating Point DWT Implementation

This section illustrates the implementation of the Standard floating point DWT decomposer and the DWT re-constructor.

Standard DWT Decomposer and Re-constructor

Figures 3 and 4 show the 16 bit floating point Standard DWT decomposer and re-constructor respectively. Its operation is explained in the below sub-sections.

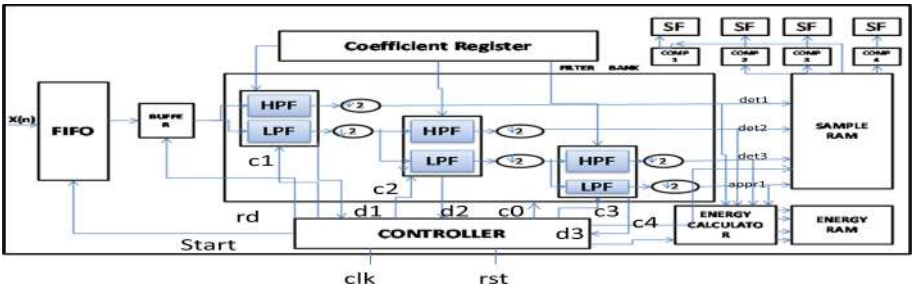

Fig. 3. 16-bit floating-point decomposer

The proposed 16-bit Standard floating-point DWT consists of various modules [5]. Each module can be explained in the below sub-sections.

FIFO

This module takes the signal sample and stores in the memory location. Once the FIFO module gets filled up the stored data is approved to the input buffer module. The FIFO module accepts the data when start signal goes high and passes data out to the input buffer module under read signal going high. The FIFO consists of 16 locations and passes out parallelly 16 samples of data at a time to the buffer module.

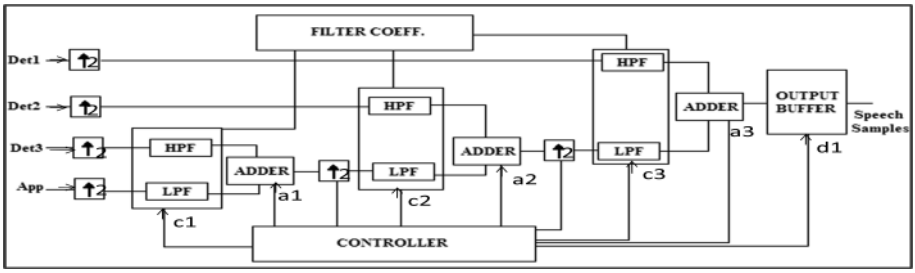

Fig. 4. 16 bit floating point re-constructor

Input Buffer

The module takes the data from the FIFO unit and packetizes the data and passes to the filter bank module. On every system clock the module passes out four samples each to the data transfer to attain synchronization between the data received and the filter bank operation.

Filter Bank

The Standard floating point DWT design consists of the core unit as the filter bank, which contains three banks of high-pass and low-pass filters. The filters decompose the input-signal samples into various sub bands depend upon the filter co-efficients sent to it.

Filter Stack

The filter stacks are the sub-modules of the filter bank where a pair of high-pass and low-pass filters are embedded into it. The high pass filter performs convolution operation between the input signal and the filter co-efficient passed from the co-efficient register. The convolution operation is carried out by the implementation of a floating point multiplier and a floating point adder module followed by shifting operation.

The high pass filter extracts the upper frequency components from the signal that get decimated by 2. The obtained samples are then passed down to SRAM unit where the samples get stored into the memory unit. The high pass unit gives the detail co-efficients and the low pass filter gives the approximate co-efficients which get further decomposed into its individual components. The low pass filter carries out the operation similar to high pass filter.

Controller

The controller is the control unit of the standard DWT design. It generates the control signals to different modules for its proper functionality. The controller reads the status of the filter stack as d1, d2 and d3 signal and generates appropriate control signals to the filter stack for its proper functioning. The controller gives the start signal to the FIFO unit when the system is reset and on the completion of FIFO filling generates a control signal to energy RAM and sample RAM to store the obtained samples and their energy.

Co-efficient Register
This unit holds the filter co-efficients for the filter unit and passes the co efficients to the filter bank for its operation.

Sample RAM
The detail and approximate co-efficients obtained from the filter bank are stored into the sample RAM unit. Sample RAM unit consists of 9 × 4 memory location to store the sub band samples. Each band is stored separately in sequence in the memory location.

Energy RAM
This module calculates the energy of each sample unit. The energy of a sample is calculated as square of the magnitude sample.

Comparator
The comparator module compares the obtained detail co-efficients and approximate co efficient elements in each sub band and finds the highest value in every sub band. The obtained value is the scale-factor for that sub band stored as Sfac1, Sfac2, Sfac3 and Sfac4.

Operation
The samples of the speech or audio whichever is to be processed that should be applied at the input of the FIFO of Fig. 3. As soon as controller sends the start signal to FIFO, it commences to accept the samples from the input. Because, FIFO length is 16 × 16, it stores the maximum of sixteen samples with the 16-bit length of each. Whenever FIFO is filled by the 16 samples it sends the first 4 samples to the buffer. From the buffer, the four samples are applied to the first section of the high pass filter and low pass filter of the filter bank. The low-pass and high-pass filters perform convolution operation between the input samples which come from the buffer and the high pass filter co-efficients from the co-efficient register. After convolution, HPF sends its output to the decimator. The decimator reduces the number of samples by 2 and then sends its output to the sample RAM. The components stored in this manner in sample RAM through the first section of the HPF are called detail1 components or det1. In the similar way, the convolution operation is carried out by the first section of the LPF between the samples come from the buffer and the low pass co-efficients from the co-efficients register. The output of the LPF is sent to the decimator for the decimation process. It reduces the number of samples to the half and sends its output to both HPF and LPF of the second section. After convolution, the outputs of the HPF which are called detail2 (det2) components, stored in the sample RAM and the outputs of the LPF are applied to the decimator. After decimation process, these will be applied to the third section of the HPF and LPF. The HPF performs the convolution operation and sends the detail3 (det3) components to sample RAM and the output of the LPF which are approximate components (appr1) are also sent to store in sample RAM at the end.

The comparator (comp) compares the respective detail and approximate components and sends the maximum component to the scale factor (SF) section. The reconstructor reads the detail components and approximate component from the scale factor section of the 16-bit floating point decomposer of Fig. 4. In the reconstructor side interpolators are used to obtain the samples which were dropped by the decimator during transmission. In the same way, adders are used to reconstruct the high pass and low pass filters' output. The reconstructor operation is exactly vice-versa to the decimator operation. At the output of reconstructor, the same signal of x(n) which was applied near the input of decomposer could be observed.

4 Results

This part presents the simulation and synthesis outcome of Standard floating point DWT.

Standard Floating-Point DWT
The simulation for the Standard-floating point DWT design is carried-out by the Modelsim 10.3cl. Since, the Modelsim has not the floating point packages, the customer defined floating point library packages are implemented and added with the standard library of the Modelsim tool. Now by porting the 16-bit floating point values using the testbench, the output would be obtained as shown in Fig. 5.

Simulation Results
Table 1 shows the simulation results of the Fig. 5 at particular instant of time t1 in binary. For easy understanding the same Table 1 was shown in Table 2 in decimal which states that the error is zero between the transmitted (input) and the received (output) values.

Table 1. Using floating-point binary values

Figure	At time	Input value (Binary)	Output value (Binary)	Error
5	t1	1000010000110110	1000010010110110	Zero

Table 2. Using floating point decimal values

Figure	At Time	Input value (Decimal)	Output value (Decimal)	Error
5	t1	$-7.6444 * 10^{-06}$	$-7.6444 * 10^{-06}$	Zero

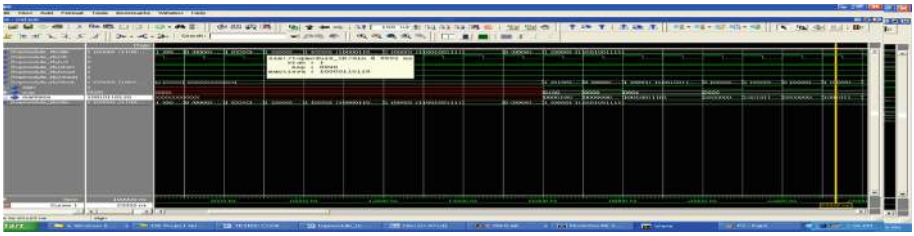

Fig. 5. The input and output values of the standard floating point DWT at particular instant of time say t1

Synthesis Results

The synthesis is developed by Xilinx Synthesis Technology (XST) tool. The chosen hardware device is Xc2s50e-ft256-6. The speed rating is −6. In this machine, the maximum number of IOs are 182 and the maximum number of BELs are 1728.

Figure 6a shows the top module of the Standard floating point DWT with pins from 0 to 15 among which 0 to 10 range is for the mantissa, 0 to 3 range is for exponent and 1-bit for sign. Figure 6b shows that internal RTL structure between FIFO and buffer. Figure 6c–d show the overall RTL diagrams of the Standard floating point DWT.

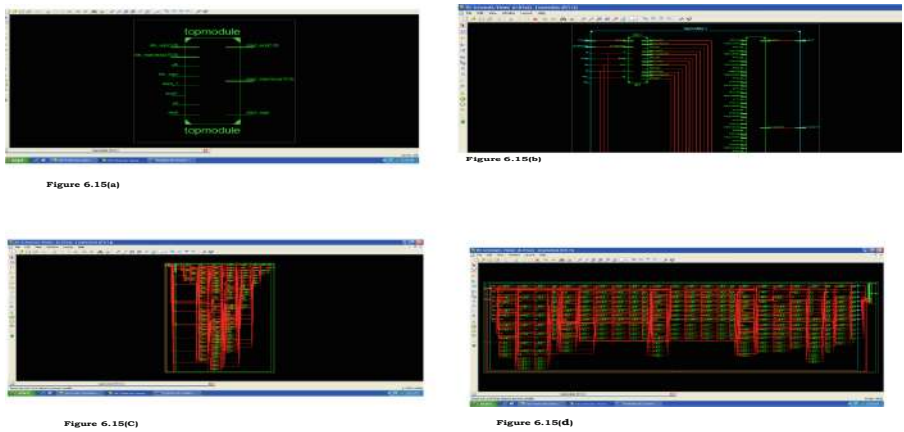

Fig. 6. RTL diagrams of standard-floating-point DWT

Synthesis Details

By the Table 3, it is known that the attained speed of the Standard floating-point DWT is 377.501 MHz through the power utilization and delay of 38.64 mw plus 2.649 ns respectively. The hardware resources that were taken by the Standard floating point DWT be 57% of IOs and 11.8% of BELs.

Table 3. Synthesis results for Standard floating-point DWT

Hardware parameters	Standard DWT
No. of IOs	105 out of 182 (57%)
No. of BELs	205 out of 1728 (11.8%)
Min. period	2.649 ns
Maximum speed	377.501 MHz
Power utilization	38.46 mW

5 Conclusion

The Standard floating-point DWT had been realized here is by the consumer defined floating-point – library-package with IEEE 754 standard. In the fixed-point DWT, the ADC and DAC need to be used physically but by develop the user defined floating-point package, a logical link had been given between source and DWT instead of physically connected data converters. To the Standard floating point DWT half precision is used; in which 1 bit is used for sign, 4-bits are used for the exponential and 11 bits are allotted for the mantissa.

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Design and Analysis of Koch Snowflake Geometry with Enclosing Ring Multiband Patch Antenna Covering S and L Band Applications

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Abstract

This chapter discusses the advancement in the performance of the Koch snowflake fractal antenna's behavior when it is enclosed in a circle. This design using the fractal geometry properties results in an antenna that resonates at multiple frequencies that are 2.141 GHz, 3.352 GHz, 4.260 GHz, 4.622 GHz, 5.161 GHz, 5.462 GHz and 6.910 GHz and the bandwidth at the resonant frequencies are 115.6 MHz, 60.2 MHz, 102.1 MHz, 139.2 MHz, 115.6 MHz, 102 MHz and 140.1 MHz, respectively. On comparing, this modified design of fractal antenna provides better results in S11 parameter than basic Koch snowflake design.

Keywords

Component Formatting Style Styling Insert (keywords)

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Personalised recommendations

Fast turbo codes using sub-block based interleaver

Publisher: IEEE

V. V. Satyanarayana Tallapragada ; Jaya Krishna Sunkara ; K.L. Narasihimha Prasad ; D. Nagaraju All Authors

Abstract: Information theory provides fundamental benchmarks based on which different communication systems can be compared. Given the channel model and transmission constraints, t... **View more**

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Abstract:
Information theory provides fundamental benchmarks based on which different communication systems can be compared. Given the channel model and transmission constraints, the information theory enables to compute rate at which reliable communication is possible. Once this rate or in other words the channel capacity is calculated, it is the task of system engineer to devise coding schemes that approach this capacity. Though the Shannon theory appears to be computationally feasible, still it was not practically implementable. The invention of turbo codes was established as an approach of reaching close to Shannon limit. The performance of turbo code depends largely on the design of interleaver. The bit error rate and delay incurred in encoding and decoding are highly influenced by the interleaver. In this paper, sub-blocking based interleaver architecture is proposed which can be extended to any existing interleaver structure. The advantage of sub-blocking the input frames is that the complexity of the interleaver reduces and consequently the execution time will be reduced drastically. In addition, a simultaneous processing of interleaving and de-interleaving can be achieved. In this paper, the said architecture is verified for block and 3GPP interleavers with

different combinations. It is shown that a reasonable BER is achieved in very less time compared to all existing interleavers.

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Contents

Design of a channel code has to consider both the bandwidth efficiency and energy efficiency. Usually, the coding techniques with less coding rate can be used to correct more number of errors as these codes have more number of additional bits which can track errors. When more number of errors could be cleared, system can work using less power and antennas with less height. Hence, the coding scheme becomes better energy efficient. At the same time, the coding schemes with lower coding rates consume more bandwidth. Code length or the coding rate has a severe effect on complexity of decoding. The complexity of decoding increases with the coding length. As per Viterbi, this is the central problem of channel coding: encoding is easy but decoding is hard [1]. For a specific channel, given bandwidth W, signal strength (or power) S and expected noise strength N there is an upper limit on rate of transmission R at which noise-free transmission may be attained. The relation that relates these terms is known as Shannon channel capacity theorem [2]. The mathematical relation is given below.

$$R < W \log_2\left(1 + \frac{S}{N}\right) (bits/\text{second}) \qquad (2)$$

DESIGN OF FPGA BASED BLOCK CIPHER CLEFIA FOR FEISTEL NETWORK

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Abstract-Data security is one of the important aspects because of hackers are easily steal the personal data thereby losing of privacy in modern days. Though number of security algorithms are presented, personal data is not secured because of hackers are decoding security code. Hence, this paper is proposed an efficient cryptography algorithm to improve security of personal data. A block cipher is used for encrypt data based on fixed length of bits which is clefia algorithm. As security is depended on number of rounds involved in key, the 128 bits of key in clefia algorithm is divided into number of rounds in feistel network. The simulation and implementation results clearly showed an improvement when compared with existing algorithms.

Keywords: security, encrypt, decrypt, cipher, feistel network

I. INTRODUCTION

In modern era, the digital data is transmitted through free channels like air. With respect to the privacy and also access management at the transmission media, a variety of security algorithms are presented. A ciphering algorithm is needed to employ when transferring of sensitive information through the public channels. Ciphering algorithm has been using for a long time because of more efficiency than other algorithms. However, there is need for dedicated secure algorithms because of the continuous growing of digital equipment and also bandwidth for digital communication channels. The cryptography algorithms are divided in to two classes that are asymmetric and symmetric. The asymmetric algorithm is used different keys for encryption and decryption and also involved complex mathematical modeling thereby increasing the processing time and reducing the speed of algorithm where as symmetric algorithm is used only one that is secret key for encryption and decryption and also involved byte substitution, bit permutation and basic arithmetic operations thereby processing the large amount of data in small amount of time. A, the novel symmetrical block ciphering algorithm that is clefia algorithm presented and developed by SONY Corporation specially focused for Digital Rights Management (DRM) purpose.

The word clefia is derived from French word “clef” and block size is 128 bits where as key size is 128,192 and 256 bits. The clefia algorithm improves security of encryption by using of diffusion switch mechanism that is consisted of diffusion matrices in predetermine order. To present immunity against differential and linear attacks, whitening keys and combining data with some portion of key before and after encryption of clefia algorithm. The clefia algorithm is interfaced with advanced encryption standard (AES) with block size of 128 bits and key size is 128, 192 and 256 bits. The clefia cipher is efficiently designed to concentrate state-of-the-art cryptography techniques thereby achieving the sufficient immunity against known cryptanalytic attacks. One of the key advantages is to enhance efficiency for both software and hardware implementation. The clefia algorithm is able to provide advanced capabilities in smart cards and mobile devices. This paper is proposed an efficient clefia algorithm and realized with diffusion matrixes and also substitution box(S-box). The key scheduling part is utilization of a generalized Feistel structure, and also possibility for sharing to data processing parts. Double Swap function is implemented to enable efficient round key generation in encryption and decryption. The remaining paper as follows: section-II presented as related work of clefia algorithm and section-III propounded proposed clefia algorithms to improve the efficiency for both hardware and software. Section-IV is presented results and discussion and finally, concludes the paper in section-V.

II. RELATED WORK

The clefia is realized by harmonizing conventional design methods and also presented new design techniques. The 4-branch is generalized Feistel structure of network enables to implement F-functions compactly for both in hardware and software. Aoki et al. [1] presented that the camellia algorithm is provided high security and privacy against differential and linear cryptanalyses. The Camellia algorithm is consisted only 8-by-8-bit s-boxes and logical operations thereby implementing

efficiently on different platforms. The comparison is provided in terms of implementation speed and occupied gates. The camellia algorithm is showed better results than different version of AES. Biham, E et al. [2] proposed cryptanalytic technique based on impossible differentials. A new variant of differential cryptanalysis and use it to analyze Skipjack. The proposed algorithm is recovering keys of Skipjack reduced from 32 to 31rounds thereby enhancing the performance faster than exhaustive search. Biryukov and Wagner [3] describe a new generic algorithm known as plaintext attack on product ciphers which is independent of the number of rounds of a cipher. The several block ciphers are analyzed that are decompose into r iterations of a single key-dependent permutation Fi thereby illustrating the power results for the block ciphers. Mozaffari-Kermani & Azarderakhsh [4] derived formulations of parity-prediction for both linear and non-linear block ciphers thereby utilizing for fault diagnosis. By using parity-prediction approach, the error detection is obtained almost 100% with respect of injected faults. The efficiency and overhead are observed at both of ASIC and FPGA target devices. Roy et al. [5]proposed a novel framework called SAFARI to synthesize the fault attack resistant implementations of block ciphers automatically. It detects the vulnerable locations and applies countermeasure based requirements thereby synthesizing protected code with RTL for block cipher. The performance of SAFARI is evaluated and compared with existing block ciphers such as AES, CAMELLIA and CLEFIA in terms of design overhead and fault coverage.

In this paper, a novel design approach of clefia is presented with F-functions that employ DSM. To observe efficiency, the proposed approach analyzed with different diffusion matrices, and two different S-boxes for stronger immunity against a certain class of attacks. Consequently, the required number of rounds can be reduced thereby enhancing the security than existing approaches.

III. PROPOSED WORK

The Clefia block cipher is used a 4-branch and type-2 feistel network structure because of F-functions is processed with high speed than traditional networks and parallel processing enabled in case of more processors. Fig.1 depicts the block diagram of clefia block cipher which has size of 128-bits. The 128-bit of plain text is encoded with same size of key thereby obtaining clefia block cipher in transmitter side. In receiver side, the same cipher is decoded with same key thereby obtaining of original plain text. The clefia block cipher is used different diffusion matrices and two different S-boxes for enhancing the speed of cipher by reducing number of rounds. The two S-boxes are implemented based on the various algebraic functions that are to increase the immunity. To increase the security of advanced clefia block cipher, the compact key scheduling design and double swap function are used. The key scheduling part is used a generalized feistel structure thereby sharing for data processing parts. The double swap function of clefia block cipher is efficiently implemented for key generation of encryption and decryption. Feistel cipher is a symmetric structure used in the construction of bock ciphers and it is advantage that the same key used for both encryption and decryption. The operation of encryption and decryption are same and also identical. As requiring reversal of key for identical operation of both encryption and decryption with rotation, the required circuitry is half than other conventional circuits for generating cipher. Fig.2 depicts an optimized asynchronous encryption padding (OAEP) which is used a simple feistel network to obtain randomize block cipher for asymmetric key algorithms. For instance, MISTY1 is a feistel block cipher which is three round feistel networks with rotation. From fig.2, it is understood that the generating of cipher by dividing plain text in to two parts that is left and right thereby adding key to the feistel network. The number of rounds of rotation is depended on the length of plain text.

(a) S-box

A substitution box(S-box) is typically is used for block ciphers to obtain synchronization between key and cipher text based on confusion law of Shannon's. S-box conventionally has 'm' number of inputs and 'n' number of outputs where 'm' is not equal to 'n'. For each size of $m \times n$ S-box is produced 2^m words where size of each word is equal to length of n. Table 1 presented the S-box size of 6×4 which is implemented with Shannon's confusion law. The 6-bit input is given as rotation based to S-box. The 4-bit output is generated by selecting a row of outer two bits that are first and last bits. For instance, an input of "011011" is outer bits are "01" and inner bits are "1101" hence the output is "1001". For any S-box, the output bits are selected with applying bent function for the inputs.

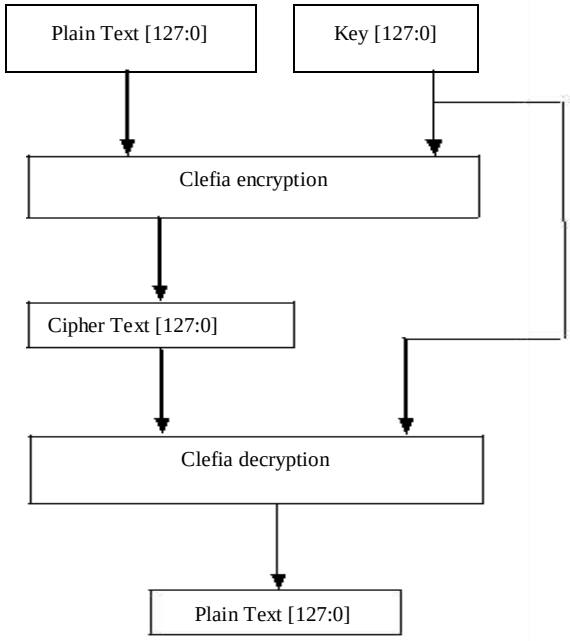


Fig.1 Block diagram of clefia block cipher

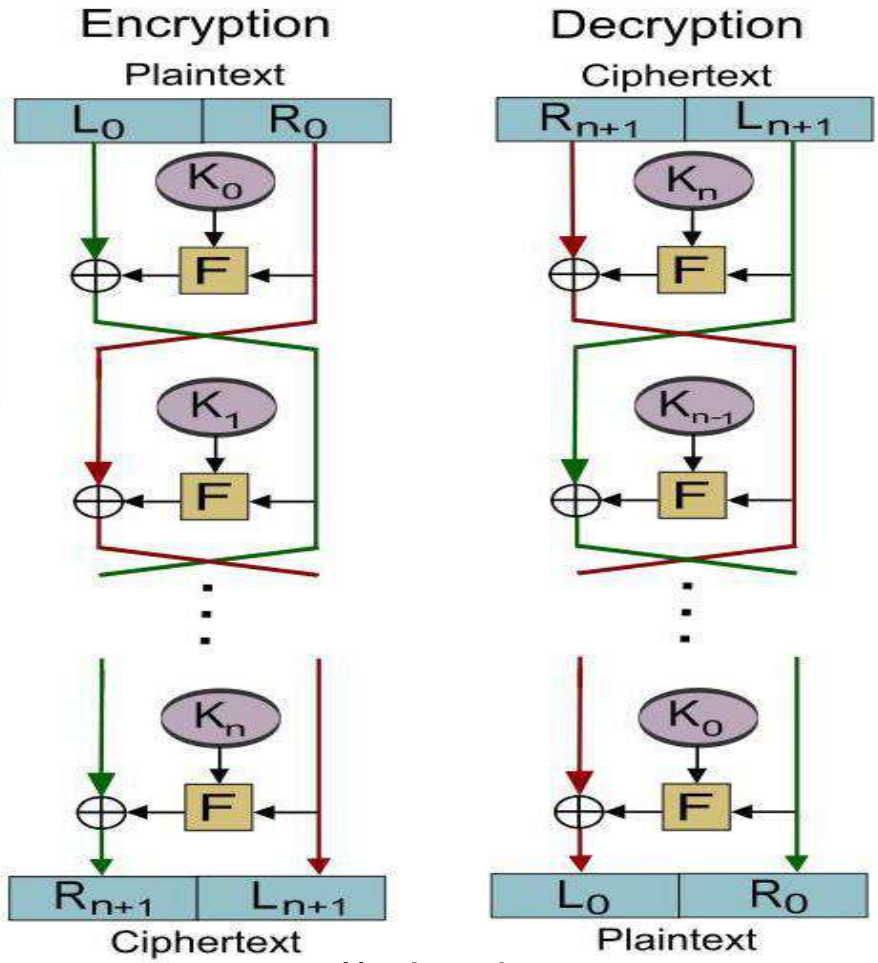


Fig.2 structure of feistel network

(b) Diffusion Switching Mechanism

One of the novel approaches for clefia block cipher is diffusion switching mechanism (DSM) by employing different diffusion matrices to achieve high immunity algorithm against differential and linear cryptanalysis. The S-box of clefia block cipher is employed two different algebraic structures thereby increasing the algebraic immunity. This structure is facilitated easy analysis, strong security against attacks. With DSM, the clefia block cipher is generated key by applying two matrices and also 4-branch network for generalized feistel.

Table 1 Implementation of 6×4 S-box

S_5		Middle 4 bits of input															
		0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
Outer bits	00	0010	1100	0100	0001	0111	1010	1011	0110	1000	0101	0011	1111	1101	0000	1110	1001
	01	1110	1011	0010	1100	0100	0111	1101	0001	0101	0000	1111	1010	0011	1001	1000	0110
	10	0100	0010	0001	1011	1010	1101	0111	1000	1111	1001	1100	0101	0110	0011	0000	1110
	11	1011	1000	1100	0111	0001	1110	0010	1101	0110	1111	0000	1001	1010	0100	0101	0011

(c) Key Management Interoperability Protocol

Key management is one of the major concerns for keys at the user level either between the users or the systems. In contrast, key scheduling is typically referred to the internal handling of keys within the operation of a cipher. A Key Management System (KMS) is also known as the Cryptographic Key Management System (CKMS), which is an integrated approach for generating and distributing and managing cryptographic keys for devices and applications. The KMS is included a backend functionality to generate the key, distribution, and replacement thereby functioning of the client in terms of injecting keys, storing and managing keys on devices. The Key Management Interoperability Protocol (KMIP) is allowed to create keys and also distribute among the various systems. It is provided full key life cycle for both cryptographic algorithms in terms of various formats and Meta data based keys.

IV. RESULTS AND DISCUSSION

The proposed design is implemented in Xilinx ISE 14.6 software and performance is analyzed in terms of synthesis results that are occupied area, latency and power consumption. The simulations of proposed design are conducted in Modelsim and synthesis results are obtained with implementation of Spartan 3E (3s50vq100-4) FPGA device.

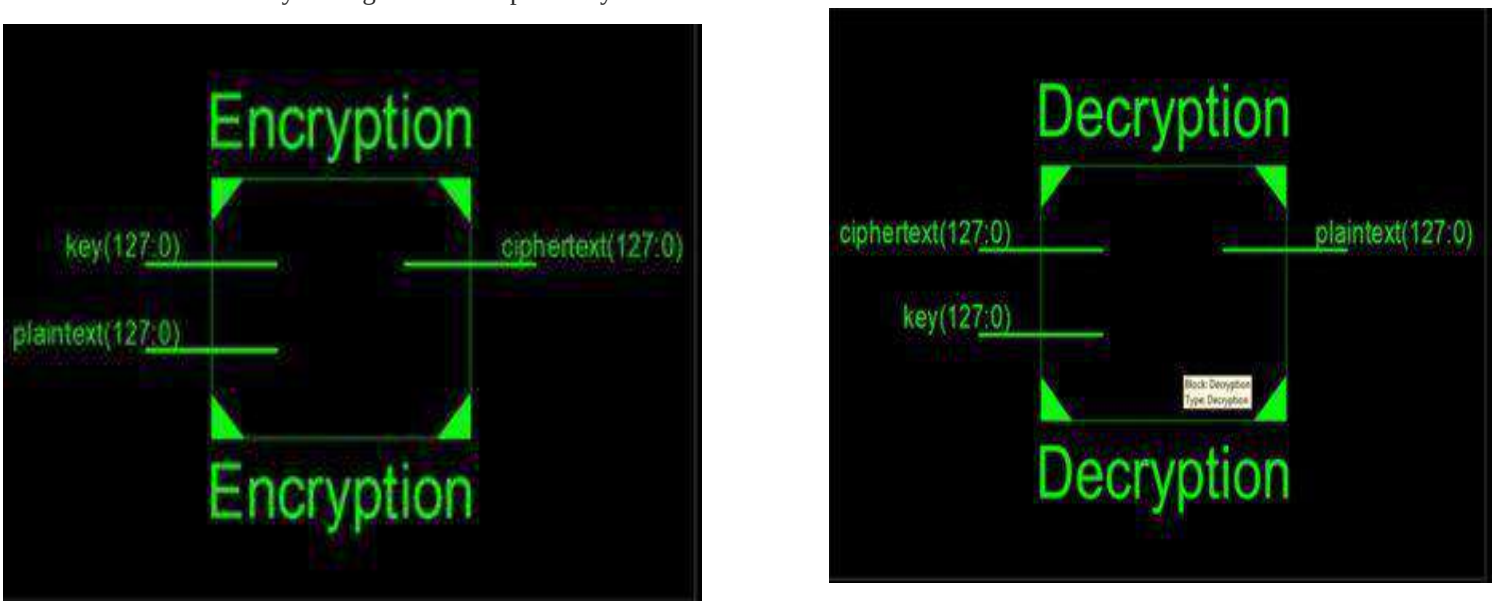


Fig. 3 RTL schematic of top module for encryption and decryption

The proposed block cipher of encryption and decryption is implemented separately thereby combining entire design as single module. The 128-bit clefia block this is encrypted and decrypted in feistel network. The top level RTL structure is shown in fig.3 which is represented encryption and decryption separately.

Fig.4 depicts internal RTL structure of 128-bit clefia block cipher that is implemented with verilog HDL in Xilinx software.

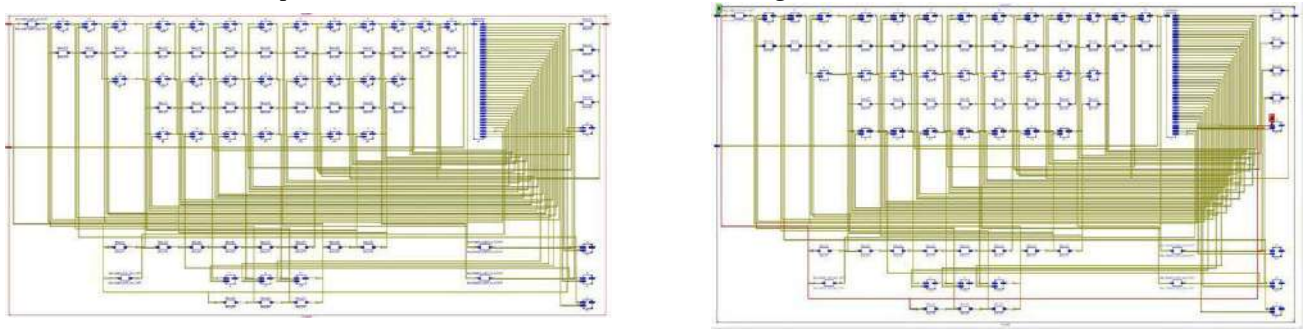
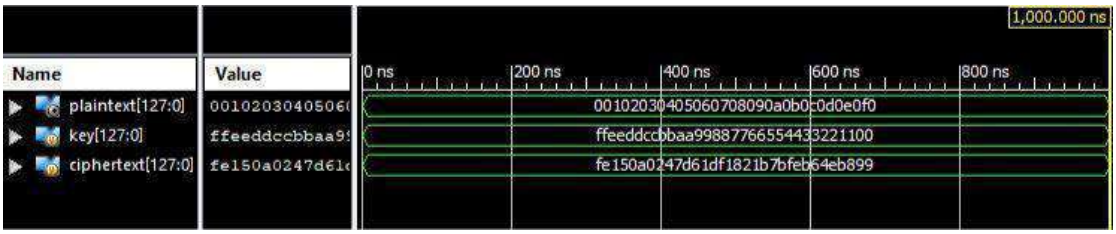


Fig.4 RTL internal schematic of encryption and decryption for block cipher

From fig.4, it is clear that the 128-bit block cipher is efficiently implemented in FPGA target device and also analyzes the performance of clefia block cipher in terms of resource utilization, delay and power consumption.The 128-bit simulation results are presented in fig.5 that is encryption and decryption processes are presented with cither text. From fig.5, it inferred that the advanced clefia block cipher for feistel network is worked accurately thereby proving of high security for personal data even when public channels are used.

(a)



(b)

Fig.5 128-bit clefia block code (a) encryption (b) decryption

The synthesis results for 128-bit clefia block cipher are presented in table.1 in terms of occupied slices, LUT-FF pairs and IOBs. From table.2, it is clears that the area utilization of 128-bit clefia block cipher in feistel network is less because of advanced method for implementing block cipher that is whitening of keys.

Table 2 Area utilization of 128-bit advanced clefia block cipher in feistel network

128-bit CLEFIA	Utilized	Available	Percentage of utilization
No. of Slices	19373	768	2524% (*)
LUT-FF pairs	37904	1536	2470% (*)
IOBs	384	63	609% (*)

*indicates more than 100% of device resources are used

Table 3 is presented delay and power consumption of 128-bit clefia block cipher. From table.3, it is cleared that the speed of encryption and decryption techniques are high and power consumption is also less because of reduced number of rounds for generating key for cipher.

Table 3 Delay and power consumption results of 128-bit advanced clefia block cipher

128-bit CLEFIA	
Delay (ns)	336.727
Power consumption (mW)	18.74

Clefia is achieved 1.60 Gbps with 6K gates in hardware using 0.09 µm CMOS ASIC library and also 13 cycles/byte, 1.48 Gbps on 2.4 GHz AMD Athlon 64 processor in software. Hence, Clefia is an efficient block cipher in security and also performance is more than advantageous among other block ciphers especially in terms of hardware.

V. CONCLUSION

A clefia is implemented with 4-branch generalized Feistel structure which is enabled F-functions for both in hardware and software. In this paper, the advanced CLEFIA block cipher is employed Diffusion Switching Mechanism that is ensured the immunity against major attacks. The advanced clefia is simulated and synthesized on Xilinx ISE 14.6 software. The 128-bit block cipher CLEFIA is improved the security of encryption with

the use of techniques such as Diffusion Switch Mechanisms in feistel network thereby obtaining the enough immunity against major attacks. Hence, the design of advanced clefia is efficient for implementation of open network environments. In future, the clefia block cipher is to test with Advanced Encryption Security for compatible using pipelining technique.

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DESIGN OF FPGA BASED BLOCK CIPHER CLEFIA FOR FEISTEL NETWORK

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Abstract-Data security is one of the important aspects because of hackers are easily steal the personal data thereby losing of privacy in modern days. Though number of security algorithms are presented, personal data is not secured because of hackers are decoding security code. Hence, this paper is proposed an efficient cryptography algorithm to improve security of personal data. A block cipher is used for encrypt data based on fixed length of bits which is clefia algorithm. As security is depended on number of rounds involved in key, the 128 bits of key in clefia algorithm is divided into number of rounds in feistel network. The simulation and implementation results clearly showed an improvement when compared with existing algorithms.

Keywords: security, encrypt, decrypt, cipher, feistel network

I. INTRODUCTION

In modern era, the digital data is transmitted through free channels like air. With respect to the privacy and also access management at the transmission media, a variety of security algorithms are presented. A ciphering algorithm is needed to employ when transferring of sensitive information through the public channels. Ciphering algorithm has been using for a long time because of more efficiency than other algorithms. However, there is need for dedicated secure algorithms because of the continuous growing of digital equipment and also bandwidth for digital communication channels. The cryptography algorithms are divided in to two classes that are asymmetric and symmetric. The asymmetric algorithm is used different keys for encryption and decryption and also involved complex mathematical modeling thereby increasing the processing time and reducing the speed of algorithm where as symmetric algorithm is used only one that is secret key for encryption and decryption and also involved byte substitution, bit permutation and basic arithmetic operations thereby processing the large amount of data in small amount of time. A, the novel symmetrical block ciphering algorithm that is clefia algorithm presented and developed by SONY Corporation specially focused for Digital Rights Management (DRM) purpose.

The word clefia is derived from French word “clef” and block size is 128 bits where as key size is 128,192 and 256 bits. The clefia algorithm improves security of encryption by using of diffusion switch mechanism that is consisted of diffusion matrices in predetermine order. To present immunity against differential and linear attacks, whitening keys and combining data with some portion of key before and after encryption of clefia algorithm. The clefia algorithm is interfaced with advanced encryption standard (AES) with block size of 128 bits and key size is 128, 192 and 256 bits. The clefia cipher is efficiently designed to concentrate state-of-the-art cryptography techniques thereby achieving the sufficient immunity against known cryptanalytic attacks. One of the key advantages is to enhance efficiency for both software and hardware implementation. The clefia algorithm is able to provide advanced capabilities in smart cards and mobile devices. This paper is proposed an efficient clefia algorithm and realized with diffusion matrixes and also substitution box(S-box). The key scheduling part is utilization of a generalized Feistel structure, and also possibility for sharing to data processing parts. Double Swap function is implemented to enable efficient round key generation in encryption and decryption. The remaining paper as follows: section-II presented as related work of clefia algorithm and section-III propounded proposed clefia algorithms to improve the efficiency for both hardware and software. Section-IV is presented results and discussion and finally, concludes the paper in section-V.

II. RELATED WORK

The clefia is realized by harmonizing conventional design methods and also presented new design techniques. The 4-branch is generalized Feistel structure of network enables to implement F-functions compactly for both in hardware and software. Aoki et al. [1] presented that the camellia algorithm is provided high security and privacy against differential and linear cryptanalyses. The Camellia algorithm is consisted only 8-by-8-bit s-boxes and logical operations thereby implementing

efficiently on different platforms. The comparison is provided in terms of implementation speed and occupied gates. The camellia algorithm is showed better results than different version of AES. Biham, E et al. [2] proposed cryptanalytic technique based on impossible differentials. A new variant of differential cryptanalysis and use it to analyze Skipjack. The proposed algorithm is recovering keys of Skipjack reduced from 32 to 31rounds thereby enhancing the performance faster than exhaustive search. Biryukov and Wagner [3] describe a new generic algorithm known as plaintext attack on product ciphers which is independent of the number of rounds of a cipher. The several block ciphers are analyzed that are decompose into r iterations of a single key-dependent permutation Fi thereby illustrating the power results for the block ciphers. Mozaffari-Kermani & Azarderakhsh [4] derived formulations of parity-prediction for both linear and non-linear block ciphers thereby utilizing for fault diagnosis. By using parity-prediction approach, the error detection is obtained almost 100% with respect of injected faults. The efficiency and overhead are observed at both of ASIC and FPGA target devices. Roy et al. [5]proposed a novel framework called SAFARI to synthesize the fault attack resistant implementations of block ciphers automatically. It detects the vulnerable locations and applies countermeasure based requirements thereby synthesizing protected code with RTL for block cipher. The performance of SAFARI is evaluated and compared with existing block ciphers such as AES, CAMELLIA and CLEFIA in terms of design overhead and fault coverage.

In this paper, a novel design approach of clefia is presented with F-functions that employ DSM. To observe efficiency, the proposed approach analyzed with different diffusion matrices, and two different S-boxes for stronger immunity against a certain class of attacks. Consequently, the required number of rounds can be reduced thereby enhancing the security than existing approaches.

III. PROPOSED WORK

The Clefia block cipher is used a 4-branch and type-2 feistel network structure because of F-functions is processed with high speed than traditional networks and parallel processing enabled in case of more processors. Fig.1 depicts the block diagram of clefia block cipher which has size of 128-bits. The 128-bit of plain text is encoded with same size of key thereby obtaining clefia block cipher in transmitter side. In receiver side, the same cipher is decoded with same key thereby obtaining of original plain text. The clefia block cipher is used different diffusion matrices and two different S-boxes for enhancing the speed of cipher by reducing number of rounds. The two S-boxes are implemented based on the various algebraic functions that are to increase the immunity. To increase the security of advanced clefia block cipher, the compact key scheduling design and double swap function are used. The key scheduling part is used a generalized feistel structure thereby sharing for data processing parts. The double swap function of clefia block cipher is efficiently implemented for key generation of encryption and decryption. Feistel cipher is a symmetric structure used in the construction of bock ciphers and it is advantage that the same key used for both encryption and decryption. The operation of encryption and decryption are same and also identical. As requiring reversal of key for identical operation of both encryption and decryption with rotation, the required circuitry is half than other conventional circuits for generating cipher. Fig.2 depicts an optimized asynchronous encryption padding (OAEP) which is used a simple feistel network to obtain randomize block cipher for asymmetric key algorithms. For instance, MISTY1 is a feistel block cipher which is three round feistel networks with rotation. From fig.2, it is understood that the generating of cipher by dividing plain text in to two parts that is left and right thereby adding key to the feistel network. The number of rounds of rotation is depended on the length of plain text.

(a) S-box

A substitution box(S-box) is typically is used for block ciphers to obtain synchronization between key and cipher text based on confusion law of Shannon's. S-box conventionally has 'm' number of inputs and 'n' number of outputs where 'm' is not equal to 'n'. For each size of $m \times n$ S-box is produced 2^m words where size of each word is equal to length of n. Table 1 presented the S-box size of 6×4 which is implemented with Shannon's confusion law. The 6-bit input is given as rotation based to S-box. The 4-bit output is generated by selecting a row of outer two bits that are first and last bits. For instance, an input of "011011" is outer bits are "01" and inner bits are "1101" hence the output is "1001". For any S-box, the output bits are selected with applying bent function for the inputs.

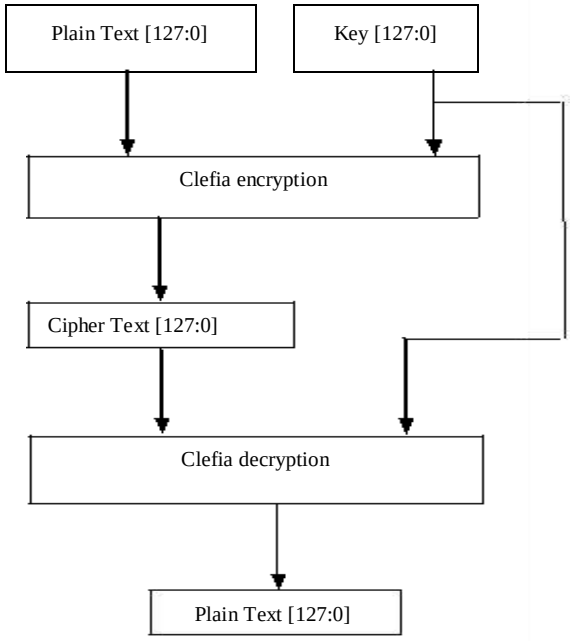

Fig.1 Block diagram of clefia block cipher

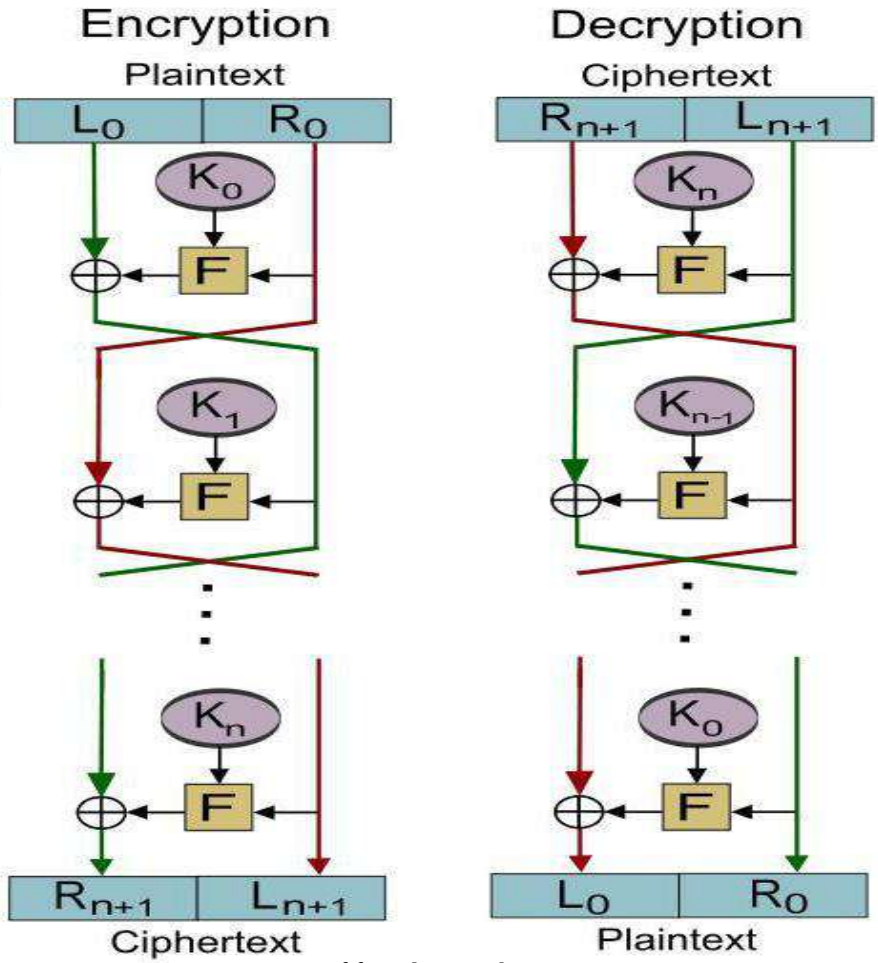

Fig.2 structure of feistel network

(b) Diffusion Switching Mechanism

One of the novel approaches for clefia block cipher is diffusion switching mechanism (DSM) by employing different diffusion matrices to achieve high immunity algorithm against differential and linear cryptanalysis. The S-box of clefia block cipher is employed two different algebraic structures thereby increasing the algebraic immunity. This structure is facilitated easy analysis, strong security against attacks. With DSM, the clefia block cipher is generated key by applying two matrices and also 4-branch network for generalized feistel.

Table 1 Implementation of 6×4 S-box

S_5		Middle 4 bits of input															
		0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
Outer bits	00	0010	1100	0100	0001	0111	1010	1011	0110	1000	0101	0011	1111	1101	0000	1110	1001
	01	1110	1011	0010	1100	0100	0111	1101	0001	0101	0000	1111	1010	0011	1001	1000	0110
	10	0100	0010	0001	1011	1010	1101	0111	1000	1111	1001	1100	0101	0110	0011	0000	1110
	11	1011	1000	1100	0111	0001	1110	0010	1101	0110	1111	0000	1001	1010	0100	0101	0011

(c) Key Management Interoperability Protocol

Key management is one of the major concerns for keys at the user level either between the users or the systems. In contrast, key scheduling is typically referred to the internal handling of keys within the operation of a cipher. A Key Management System (KMS) is also known as the Cryptographic Key Management System (CKMS), which is an integrated approach for generating and distributing and managing cryptographic keys for devices and applications. The KMS is included a backend functionality to generate the key, distribution, and replacement thereby functioning of the client in terms of injecting keys, storing and managing keys on devices. The Key Management Interoperability Protocol (KMIP) is allowed to create keys and also distribute among the various systems. It is provided full key life cycle for both cryptographic algorithms in terms of various formats and Meta data based keys.

IV. RESULTS AND DISCUSSION

The proposed design is implemented in Xilinx ISE 14.6 software and performance is analyzed in terms of synthesis results that are occupied area, latency and power consumption. The simulations of proposed design are conducted in Modelsim and synthesis results are obtained with implementation of Spartan 3E (3s50vq100-4) FPGA device.

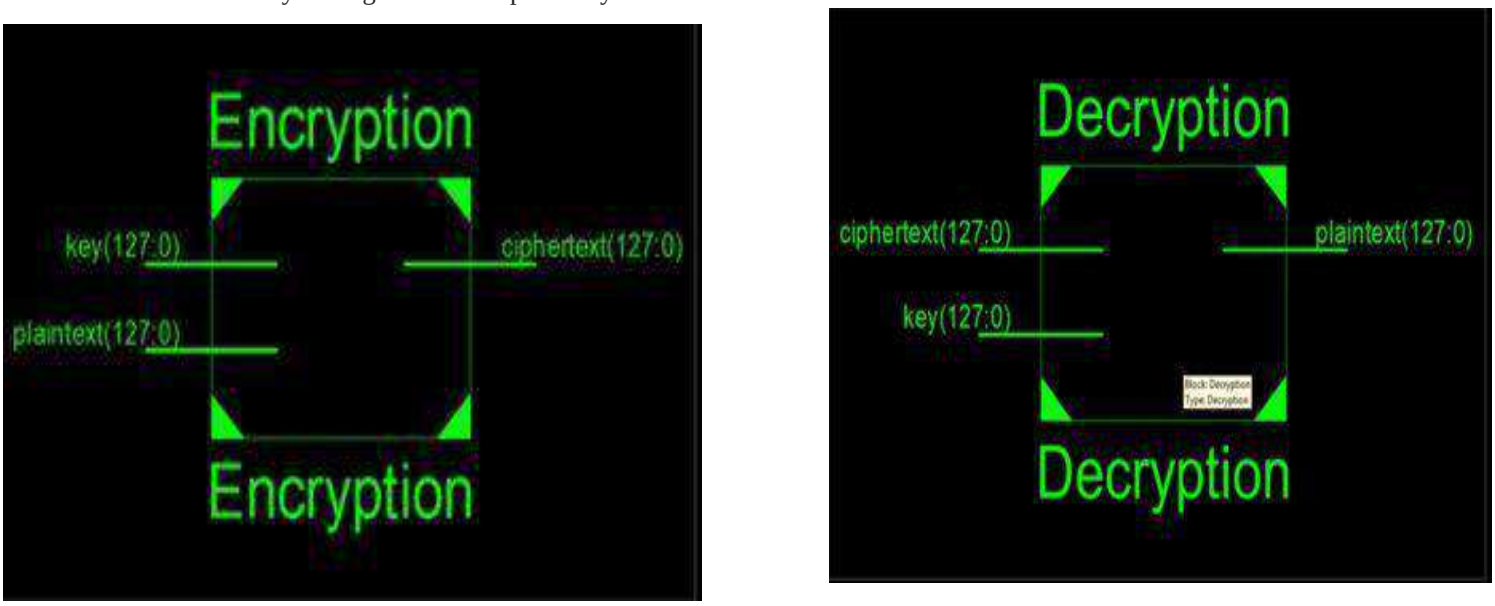

Fig. 3 RTL schematic of top module for encryption and decryption

The proposed block cipher of encryption and decryption is implemented separately thereby combining entire design as single module. The 128-bit clefia block this is encrypted and decrypted in feistel network. The top level RTL structure is shown in fig.3 which is represented encryption and decryption separately.

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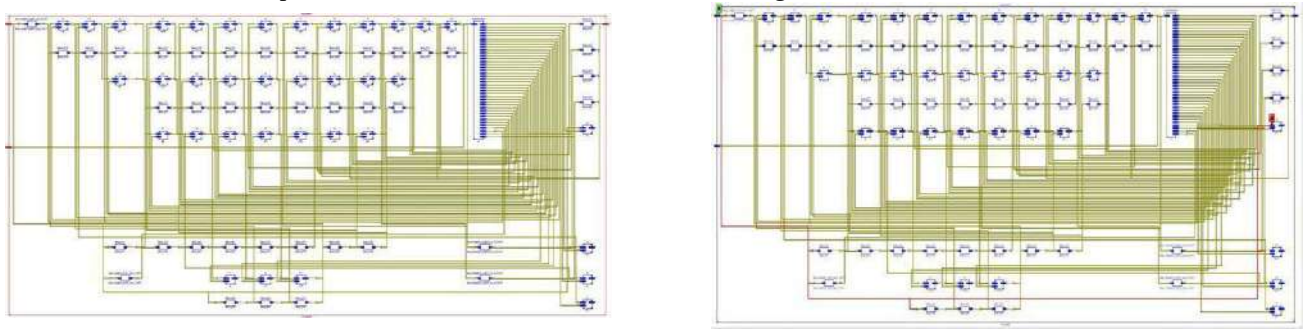
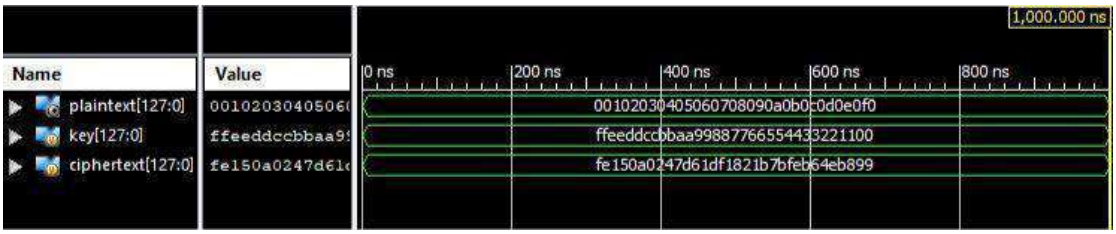


Fig.4 RTL internal schematic of encryption and decryption for block cipher

From fig.4, it is clear that the 128-bit block cipher is efficiently implemented in FPGA target device and also analyzes the performance of clefia block cipher in terms of resource utilization, delay and power consumption.The 128-bit simulation results are presented in fig.5 that is encryption and decryption processes are presented with cither text. From fig.5, it inferred that the advanced clefia block cipher for feistel network is worked accurately thereby proving of high security for personal data even when public channels are used.

(a)



(b)

Fig.5 128-bit clefia block code (a) encryption (b) decryption

The synthesis results for 128-bit clefia block cipher are presented in table.1 in terms of occupied slices, LUT-FF pairs and IOBs. From table.2, it is clears that the area utilization of 128-bit clefia block cipher in feistel network is less because of advanced method for implementing block cipher that is whitening of keys.

Table 2 Area utilization of 128-bit advanced clefia block cipher in feistel network

128-bit CLEFIA	Utilized	Available	Percentage of utilization
No. of Slices	19373	768	2524% (*)
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Table 3 is presented delay and power consumption of 128-bit clefia block cipher. From table.3, it is cleared that the speed of encryption and decryption techniques are high and power consumption is also less because of reduced number of rounds for generating key for cipher.

Table 3 Delay and power consumption results of 128-bit advanced clefia block cipher

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Delay (ns)	336.727
Power consumption (mW)	18.74

Clefia is achieved 1.60 Gbps with 6K gates in hardware using 0.09 µm CMOS ASIC library and also 13 cycles/byte, 1.48 Gbps on 2.4 GHz AMD Athlon 64 processor in software. Hence, Clefia is an efficient block cipher in security and also performance is more than advantageous among other block ciphers especially in terms of hardware.

V. CONCLUSION

A clefia is implemented with 4-branch generalized Feistel structure which is enabled F-functions for both in hardware and software. In this paper, the advanced CLEFIA block cipher is employed Diffusion Switching Mechanism that is ensured the immunity against major attacks. The advanced clefia is simulated and synthesized on Xilinx ISE 14.6 software. The 128-bit block cipher CLEFIA is improved the security of encryption with

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High Reliability and Low Latency for Network on Chip

High speed data transfer and efficient error control in on-chip interconnects

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Abstract—**Reliability and performance of Network on Chip (NoC) with two Processing Elements (PEs) is major issue when permanent faults are occurred in the communication links and associated routers. This paper presents an efficient method for detecting and diagnosis of permanent faults and two virtual channels are used for bypassing the faults there by attaining the high speed communication. A Built in Self Test (BIST) with comparing module is presented for detection of struck at faults and selecting virtual channel or physical channel of transmission. For evaluation, this work is simulated at various traffic patterns and results are shown 98% of fault coverage. The latency of this NoC switch is less when compared with E-rescuer, smart reliable router.**

Keywords— NoC; Permanent Faults; BIST; Virtual Channel; FPGA

I. Introduction

To concern user applications at real time, the more processors are required in System on Chip (SoC) and need of efficient intercommunication between these processors. The Chip Multi Processor (CMP) is the key solution to satisfy the embedded environment but communication medium is the major issue in multiprocessor system on chip (MPSoC) [1] [2]. Network on Chip (NoC) is the new paradigm which replacing bus based communication for proving efficient communication in CMP. NoC comprises with inter connecting routers and links with Processing Elements (PEs) or Intellectual properties (IPs). The PEs are composed of either Memory or I/O connected with router with Network Interface (NI). The architecture of router is directly affects the overall performance of NoC based system of SoC hence the design of router crucial with major parameters of Topology, routing algorithm and switching mechanism. The data transferring is routed from source to destination by routing algorithm through intermediate routers [3]. Therefore, the direction of data packet in the network is depends on routing algorithm (deterministic, adaptive). Fig.1 presents the architecture of 3 3 NoC switch with consumer- producer pair of PEs. The conventional NoC switch architecture composed of four ports for communicating neighbour routers and one port for PE but this paper gives extra PE for assisting of router for high speed communication. The PEs is working as a producer-consumer without involvement of the corresponding router [4].

Reliability is also one of the design concerns for the router in presence of the faults and it is achievable with fault tolerance algorithm [5]. The faults may be occurs anywhere of the NoC system (Links, Routers and Network Interface) including PEs. The faults called soft can be transient nature which is abstracted in bit-flip in memory or register and also considering effect of crosstalk and capacitive coupling on interconnection wires [6]. To preserve the data packets against these errors, Error Correction Codes (ECC) are implemented within the router of NoC. Grecu et al [7] have proposed different directions of ECC for enhancing the performance. Mainly, three types of solutions popular among various types. Namely end to end, switch to switch and code disjoint solutions are used ECC in routers in the network which increases the latency, area and power consumption. Another type of faults permanent in nature called as hard faults which is effect of shorting and manufacturing defect. The different types groups classified based fault occurrence location (faulty router, faulty link). A lot of research is conducting on fault tolerant NoC mechanism because of deadlock or packet loss in the faulty system. The testing approach of NoC is classified into two parts, one is test of cores and other one is communication architecture. Test access mechanism (TAM) is used to test overhead for testing of cores [8]. The test of communication architecture includes test of router and test of associated communication link [9] and huge research has been conducted for testing of the router along with communication channels. Built in Self Test (BIST) is commonly used technique utilizing for detection and

diagnosis of faulty parts in communication architecture [10]. It is popular because of its usage for getting fully fault coverage and high performance in offline or online based mechanisms.

The main aim of this work is to provide high performance for NoC system and avoiding deadlock when permanent fault occurs in communication infrastructure. This paper also using BIST based method to detect faults at router and communication link between pair of nodes. The struck faults detected in wires of interconnection links and diagnosis for bypassing data packets from faulty components. The two virtual channels are using for two PEs (producer-consumer) for high speed communication even when permanent fault occurred in the NoC. The selection of virtual channel is based on traffic of the direction and also depends on the number free slots of FIFO buffer in neighbour router there by NoC switch provides low latency and high reliability in the presence of permanent faults.

The major contribution of this paper is store and forward switching based NoC for high fault coverage.

1. Detect and diagnosis of permanent faults with low hardware of BIST mechanism with comparing module in Network Interface.
2. Identify the direction of virtual channel to bypassing data packet in presence of the hard fault with less power consumption.
3. Design and implementing of proposed work in 2 2 NoC switch with producer- consumer pair of PEs for low latency.

The remaining of paper is as follows. Section II presented some highlights of related work of fault tolerance method. Section III describes the modified switch architecture by baseline NoC switch. Section IV proposing a modified micro router for handling the permanent faults. Section V presented results and discussion of this work with existing work and finally, section VI concludes the paper.

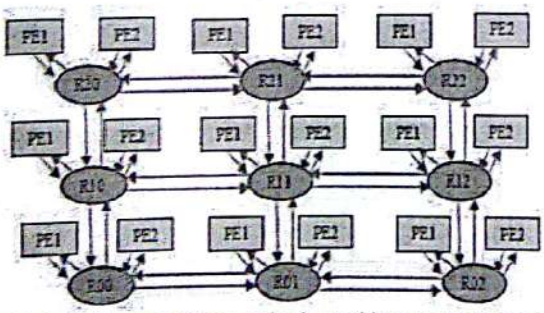


Fig.1 Bi-directional Communication architecture for NoC (3X3) switch with two PEs

II. Related work

The fault- tolerance algorithms are used to detect, diagnosis and correcting of a fault occurs in the various places of NoC architecture. The permanent faults are occurs majorly in either router component or communication links of data transmission and both. The goal of fault tolerance algorithm is preserving the NoC architecture integrity and avoiding the dead-lock when faults occur in the system. The aim of research of fault tolerance is maintaining the high performance of system even when fault introduced in elsewhere of system. Test access mechanism (TAM) is used to testing of NoC router with NI and during testing, these TAMs are working parallel there by reduces the test time but disadvantage is requiring extra wires to construct a TAM [11]. Immunet is an automatic response mechanism presented for NOC when link and node faults occur [12] and this technique is handles for different types of faults with any number of faults but it succeeds only when network is connected. To suitable any type of network topology, Gomez et al [13] proposed a fault routing algorithm for intermediate node by sending data packets from source after that transferring to the destination, this manner dividing the communication channel two sub channels. There is no degradation of performance when limited number of faults but increasing of virtual channel with increase of intermediate nodes. Emmert et al [14] proposed an online multilevel fault tolerance approach for FPGA logic blocks to tolerate hardware faults in the NoC system. The roving self – test areas (STARs) approach based on BIST used for diagnosis and repair faults without breaking normal function of system but more system degradation in the presence of new faults which occurs due to adjusting of programmable clock period. To test communication link with short faults, Cota et al [15] proposed a novel method and reviewed a cost effective test sequence for detecting short faults in data path and control path of Mesh based NoC. The scan-based test method presented in NI which consists of TDG and TRA for detection of short faults and cores are also tested by re-using NoC. For large number of faults, the system performance is degrades due to increasing undetectable faults in this strategy. Holst and wunderlich [16] proposed a new adaptive and statistical approach for pattern analysis with Automatic Test pattern Generation (ATPG) for struck at faults. These patterns achieves high diagnosis capability due to the knowledge of Device under Diagnosis (DUD) and turn guides but a fault in DUD is not active always because of known knowledge mechanism. Lehtonen et al [17] presented a novel approach for self detection and bypassing the permanent faults with a set of spare wires. A new technique in-line test (ILT) is used for detection of short faults at adjacent pair of wires in communication link. Syndrome Storage based

Detection (SSD) is assigns the spare wires even when transient fault is estimates wrongly as a permanent fault and there is no recovering spare wire hence a performance of NoC system degrades. To use the partially faulty links in link failures, Palesi et al [18] proposed a scheme and thereby improving yield performance. With additional logic in the router and appropriate selection policies, the partially faulty links enhance the performance of system but area, latency and power consumption also increases with extra needed circuit. To improve the processing at architecture level, Collet et al [19] present a Self Organized Fault Tolerant (SOFT) method from adding of self diagnosis, disconnection and discovery in the presence of permanent faults. Self test and mutual diagnosis in multi core arrays are provides advantage of isolating faulty nodes from healthy nodes but scarifies the efficient communication resources. A bidirectional communication channel NoC (BiNoC) [20] is presented to enhancing the performance and each channel self configured in its direction. The Channel Direction control (CDC) algorithm is used for controlling flow of each direction thereby avoiding deadlock and starvation but if data packet takes more latency to transmit at one direction, communication bottlenecks gives low bandwidth for the system. DeOrio et al [21] proposed a reliable routing architecture for dealing large number permanent faults in communication. Vicis, a two level approach used for attempting faults in router and communication links. It employs the port swapping technique with fully adaptive routing for avoiding congested traffic of faulty node. Vicis gives performance degradation when transistors are automatically failed. To detect faults on dynamic NoC, Killian et al [22] proposed online detection of data packets with adaptive routing errors in XY routing. A new communication switch is presented called a RKT NoC switch which is capable of handling soft errors and permanent errors. This method accurately identifies the source of error which disconnects the healthy parts of NoC router. Poluri and louri [23] proposed a reliable NoC router to tolerate of soft and hard faults called Shield mechanism. The 4-stage pipeline scheme presented for dealing hard faults with spatial redundancy method and selective hardening for soft faults thereby improvement shown in reliability but latency increases in case of faulty arbiter. To maintain function and performance of core even when router disabled, Wang et al [24] have been proposed an E-Rescuer technique by proceeding advantage of bypass channels between cores and router. This technique concentrated more on faults of control path because of deadlocks and it is not suitable for transient faults. E-Rescuer method gives limited flexibility for NoC due to it is using default path from input to output when router is disabled. Aghaei [25] has proposed a new fault coverage approach for short faults in links by adding BIST and Packet Comparing Module (PCM) in network adapter. This method is provided less test time because of parallel testing of communication channels but shown more hardware redundancy.

The proposed work is directed from Killian et al [22], Wang et al [24] and Aghaei [25] for improve flexibility of NoC switch and avoiding hardware redundancy of circuit when detection of permanent faults due to struck at fault in the communication channel. With continue of above mentioned techniques; enhance the fault coverage with BIST method and virtual channel allocation.

III. Reliable Router Architecture

The router architecture is modified for achieving the high performance of NoC and improved the faults mechanisms to get highly reliability in the presence of single or multiple permanent faults. The Network Interface is advanced with existing work where the research gap is found for detecting and diagnosis of permanent faults. The structure of NI with necessary components for handling faults and NoC switch (2 2) are described in the next section. This work initially implemented and tested for 2 2 NoC switch thereby used for implementing 4 4, 8 8 and 16 16. To demonstrate the behavior of entire NoC switch (16 16), Fig.2 shows how 2 2 NoC switch detects and diagnosis of BIST mechanism thereby improving reliability for the entire system. Each reconfigurable router is crucial for the network with faulty components. The input and output ports of router are consists of First in First out (FIFO) buffer to store the data packets and Finite State Machine (FSM) is controlling the buffer for data transfer between the buffer and NI. The dead-lock is avoided with use of store and forward switching technique along with buffer memory. The distributed round robin arbiter is providing permission to one of the input ports which is high priority to transfers the data packets and the crossbar switch sends towards the output port. To reduce the latency of crossbar switch, the multiplexer-demultiplexer (MUX-DEMUX) circuit is used and acknowledgment of selected input port is sent from the arbiter. The direction of data packet routing is given by the adapting routing algorithm and is bypassing if data traffic more in the path. To detect the permanent faults in routers and communication link, BIST based NI is used in reconfigurable NoC architecture. The comparing module decides the communication is requires virtual channel or not. The two PEs are assigned with two virtual channel, and

selection of PE is decided by the congestion that direction. The assigning of virtual channel for neighbour router is based on the free slots in the buffer of corresponding router.

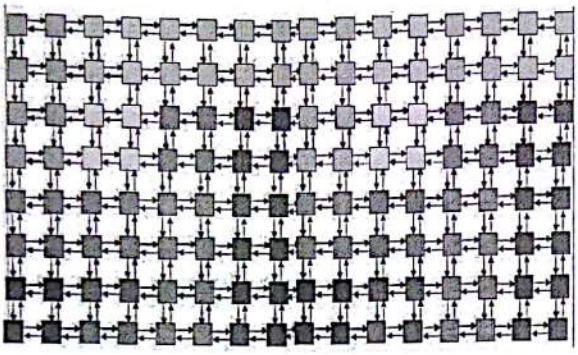


Fig.2 Architecture of 16 16 NoC using 2 2 modified NoC

IV. Proposed Approach

The finding of permanent error in the circuit is difficult in NoC switch and the channel corresponding error blocked permanently. The links between router, router and router, NI must check to before transferring the data. A lot of research methods have used for identifying the permanent error between the ports to ports. In this paper, Built in Self Test (BIST) with low power pattern generator is used for testing the router. Fig.3 described the possible location of errors in the links between router and router in 2 2 NoC. The fault may be occurred any one of link in total of 16 unidirectional links and 128 wires (16 links 8 bit data packet). The error may rise in anywhere of transferring data path from source router to destination router. If R0 is the source router and R3 is the destination router, the errors will occur in either link (L10) or link (L31). R1 is acts as the intermediate router and error may be in the router.

The probability of occurrence errors at any router depends on the number routing paths from its neighbour routers. If router R1 sending the data packets to the R0, the error will occur at links between these routers or NI, hence the probability of occurrence is . The finding of single error location is depending on probability of error occurrence location. The single error will detect and correct using with the test patterns in BIST efficiently but sometimes, error may occur more than once or same error repeats more than one location. The system gets more complex when number errors are more and detection of errors is gets critical. Hence, the proposed schemes should able to handle the more errors such that the system will not reduce performance. The proposed work uses combination of techniques for detection and correction of permanent error. For detection, the Built in Self Test (BIST) is used and for the correction, ECC codes are used. If the error is not corrected in the links, the new link will established between the nodes. The BIST module placed in Network Interface (NI) for detection of faults and even if BIST placed in routers, it does not detect faults in interconnects.

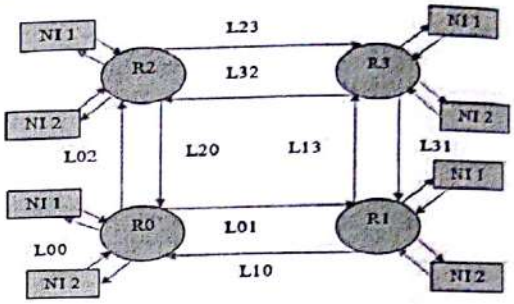


Fig.3 Possible occurrence of errors at the links either router and router or router and NI in 2 2 NoC

A. Pattern Generation:

The patterns generation is used for detecting the error in the links by assigning different inputs to the testing circuit. The circuit is which generates the pattern is important because depends on patterns, the power consumption of the circuit changes. Fig.4 describes the basic BIST operation. Linear Feedback Shift Register (LFSR) provides the patterns at conventional BIST circuits. The power consumption of pattern is more when the LFSR generates the sequence. In this proposed work, Low Power LFSR used for reducing the power consumption. The LP-LFSR generates the sequences such way that the transition activity is less. The transition activity is directly proportional to the dynamic power consumption. To get low transition sequence, the LP-LFSR is use the sequence such a manner like first part of the sequence is processing while second part is maintaining constant and also vice-versa. The generated sequence is sent for testing in the Circuit under Testing (CUT). The Response Analyzer (TRA) provides the output after comparing the outputs from Multi Input Signature Register (MISR) and expected data signal. The total operation controlled by BIST Controller Unit (BCU) and each module controlled and acknowledged to BCU.

B. Detecting faults:

The communication channel is monitored by the BIST module and when the channel is detected as faulty, the transmission of data packets stops. The faults in the channels are identified by the comparison module whose inputs are coming from BIST output and original input data signal from local port of the switch. During this process, the data packets are

blocked by the neighbour router and the current router detected as Router under Test (RUT).

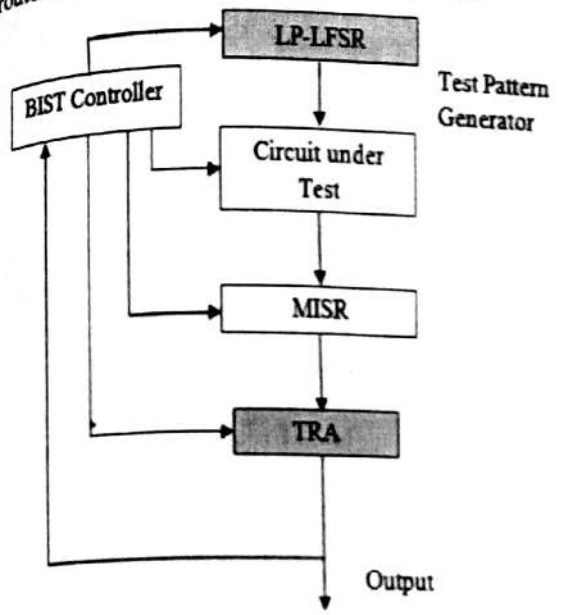


Fig.4 Block diagram of Built in Self Test with low power LFSR

After testing, the Comparing Module decides whether transmission is with virtual channel if fault indicator is positive or with physical channel if fault indicator is negative. This reconfigurable switch is not designed for the transient faults. The Error Correction Codes (ECC) is required for detection and correction of transition faults in the ports of NoC switch or re-transmission.

In this paper, the permanent faults are detected and diagnose within the communication channel. To identify the efficiency of proposed work, the struck-at-faults are introduced at links of communication between router to router or router to core.

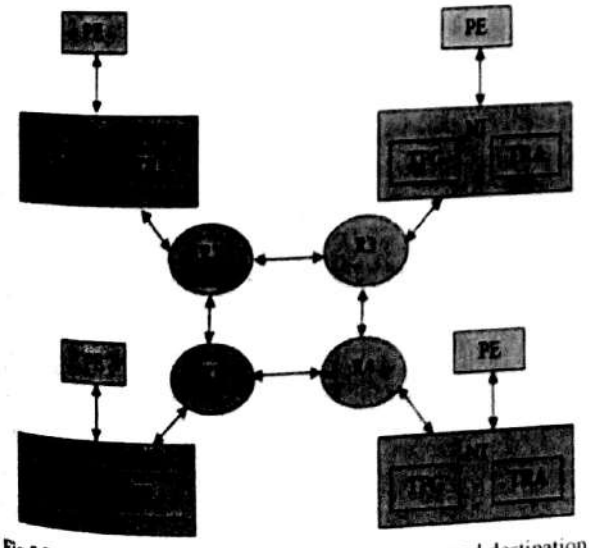


Fig.5 Process for detection of fault between source and destination switch per PE

Fig.5 presented flow of error detection from local port to destination port for single PE and same operation repeats for the double PE. The same structure designed for two PEs and selection is depends on the availability. Two types of struck faults are struck at zero (0) and struck at one (1) and these may be occurred in unidirectional or bi-directional links. The faults in bi-directional links grow exponentially with increasing of wires shorted and denoted in eq. (1)

Where is exponential growth of faults in the function of, and is the number of fault- free wires, is the number of faulty wires. The faults in wires are considered for 2X2 NoC switch in this paper and four directional links with X-Y routing are used for data transmission among the routers. The comparing module construct of Exclusive–Or (EX-OR) for both serial and parallel inputs. The output of comparison module is given to the router to use the virtual channel or physical channel. As comparing module is placed in NI, the testing of NI is not concentrated. If the fault is detected between local port and router, it is diagnosis in the same place but not propagated to remaining routing path.

Table 1 Faulty and faulty less channel for router in 2 2 NoC switch per PE

States			Router(R0)		Diagnosis Capacity
L20	L10	L00	Faulty	Fault Less	Status
0	0	0	Fault Free		-
0	0	1	NA0,R0	R1,R0 & R2,R0	-
0	1	0	R1,R0	R2,R0& NA0,R0	-
0	1	1	R1,R0 & NA0,R0	R2,R0	No Diagnosable
1	0	0	R2,R0	R1,R0 & NA0,R0	-
1	0	1	R2,R0 & NA0,R0	R1,R0	No Diagnosable
1	1	0	R1,R0 & R2,R0	NA0,R0	No Diagnosable
1	1	1	Permanent Failure		No Diagnosable

'0' indicates the fault-less and '1' indicates the faulty channel

The identification of faulty channel for any router is depending on interconnection channels between neighbour router and local port of corresponding router. Table 1 provides the information of channels is connected to router, R0. The Diagnosis capacity of R0 is 50% of total capacity because only half of the states are diagnosable among total communication channels. Table 2 Diagnosis Capacity is measured for various size of NoC Switch. For 128 wires in 2 2 NoC, 8,128 faults considered and two identical faults considered as single fault until the comparing module detects two different faults in links.

The network of NoC switch which is more than 2 2 is tested with help of 2 2 part of the switch thereby detection of faults is simple even when size of NoC is large (16 16). This work is implemented with 8 TPGs and TRAs as 2 2 NoC switch using 8 local ports for connecting PEs. Consider the same scan path for both TPG and TRA thereby the fault detection time given by 20 clock cycles since one clock cycle for start TPG, 8 clock cycles for generating 8 bit data packet to testing circuit, one clock cycle for transferring NI to router, one clock cycle for data transferring from router to neighbour router and one clock cycle for start TRA and eight clock cycles for detection of fault (1+8+1+1+1+8). Hence the total detection time for 2 2 NoC switch is given by 160 clock cycles (20 8).

Table 2 Diagnosis Capacity for various size of NoC

NoC	Status		Capacity (%)
	Total channels	Identified faulty channels	
2 2	24	15	62.5
3 3	60	43	71.4
4 4	112	85	75
8 8	480	384	80.1
16 16	1984	1626	82.3

The NoC switch is using the virtual channel for data transmission when the communication channel is permanently blocked. The creation virtual channel is given by the comparing module of switch when permanent fault identified in the physical channel between source and destination ports. The two virtual channels are using for the data transmission for two PEs and selection of direction for virtual channel is depended on memory available in FIFO buffer of neighbour router. Even though, the performance of switch is enhanced by the virtual channel but still some communication issues (power consumption, cost etc) are arises when physical channel divided into virtual channel. Fig.6 clearly explains the algorithm of virtual channel allocation in faulty communication links. The two virtual channels are utilized to avoid of faulty links as well as congestion in that direction. Ebrahimi et al [26] proposed a two virtual channel algorithm for efficient communication between nodes. This algorithm is modified and used in 2PE architecture of NoC switch thereby the high speed communication performed with the faulty links. The deadlock also avoided in this work as the NoC switch is using the store and Forward switching for data packet transmission [27].

```
Dx,Dy: X and Y co-ordinates  of the destination switch
Sx,Sy: X and Y co-ordinates  of the source node switch
Cx,Cy: X and Y co-ordinates  of the current switch
E: East; W: West; N: North; S: South; vc: Virtual Channel
Δ: Distance, DP: Destination Position
-------------------------------------------------------------------
DP <= E if Dx>Sx, Dy=Sy;      DP <= W if Dx<Sx, Dy=Sy
DP <= N if  Dx=Sx, Dy>Sy;     DP<= S if Dx=Sx, Dy<Sy
x_dir <= W when Dx<Cx otherwise E;  y_dir <= S when Dy<Cy otherwise N
VC <= vc1 if DP={N} else vc2 if DP={S}
Δ_x <= |Dx-Cx|
Δ_y <= |Dy-Cy|
-------------------------------------------------------------------
if DP={N or S}
 if (Δ _x=0)
   if neighbouring_router(y_dir)=faulty
     if congestion (east)= high
       select <=  W(vc)
     else
       select <=  E(vc)
   else
       select  <= y_dir
 else
     if neighbouring_router(x_dir)=destination
       select <= x_dir(vc)
     else
       select <= y_dir
else if DP={E or W}
    if (Δ _y=0)
      if neighbouring_node(x_dir)=faulty
        if Cy=0
          select <= south direction
        else
          select <= north direction
      else
        select <= x_dir(vc2)
    else
      if neighbouring_router(y_dir)=destination
        select <= y_dir
          else
            select <= x_dir(vc1)
```

Fig.6 Pseudo code for virtual channel allocation for faulty NoC

V. Results and Discussion

Normally, the external automatic test equipment (ATE) used for testing of FPGA but this proposed work switch is tested internally by generating test patterns of the BIST circuit. To evaluate the performance of proposed work, NoC switch (2 2) is simulated in Xilinx ISE 14.7 using Verilog HDL and synthesized in Vertex-6(V-6) FPGA device and for more accurate of results, this NoC switch is simulated in traffic patterns in Riviera Pro. First, the communication channel is tested by BIST module which is designed with TRA and TPG having Low- Power LFSR (LP-LFSR) circuit to generate less switching activity sequences. Then, stuck faults are introduced in the communication channels thereby the TPG and TRA modules are used in the NoC switch for pattern generator and fault detector addition with the comparator module. The synthesis results of proposed work which consists of BIST, comparing module, network interface, input and output ports and crossbar switch with data width of 8 bit are presented in table 3. The 12,192 shorts are injected from 192 data channels in 2 2 NoC switch and simulation of this took several minutes.

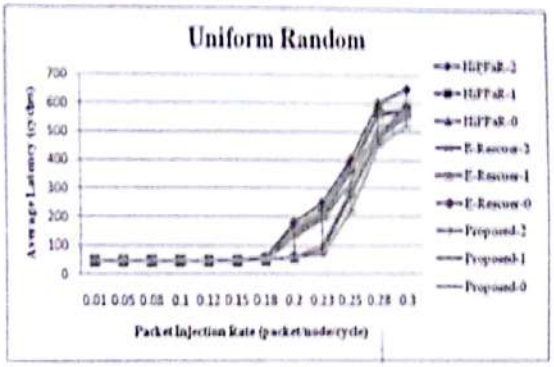
Table 3 Synthesis results of NoC switch components individually

NoC 8 bit without virtual channel	Occupied Slices	LUT-FF pairs	IOBs	Delay (ns)	Power Consumption (mW)
BIST	44	130	19	1.509	3.93
Comparison Module	3	4	17	0.91	0.76
Arbiter	3	3	14	0.74	2.91
Crossbar	53	160	109	0.74	3.95
Input Port	7	19	26	1.70	15.41
Output port	8	22	20	1.74	4.83
Total	584	1961	108	1.88	39.87
With virtual channel	165	444	120	1.80	405.94

NoC 16 bit without virtual channel	Occupied Slices	LUT-FF pairs	IOBs	Delay (ns)	Power Consumption (mW)
BIST	52	136	35	1.709	4.02
Comparison Module	7	8	33	1.91	1.76
Arbiter	3	3	14	0.74	2.91
Crossbar	98	298	205	1.42	8.06
Input Port	10	25	42	1.73	20.57
Output port	13	30	36	1.77	8.98
Total	633	2053	204	1.93	41.19
With virtual channel	237	660	232	2.10	808.15

NoC32 bit without virtual channel	Occupied Slices	LUT-FF pairs	IOBs	Delay (ns)	Power Consumption (mW)
BIST	87	213	67	1.96	7.35
Comparison Module	13	16	65	2.68	2.46
Arbiter	3	3	14	0.74	2.91
Crossbar	157	541	396	1.74	12.47
Input Port	14	29	74	1.85	30.97
Output port	16	34	68	1.92	22.05
Total	718	2320	396	2.13	42.79
With virtual channel	373	925	456	2.39	1661.88

The reliability of this switch is comparing with HiPFaR [26], E-Rescuer [24] in terms of delay and power consumption and for this, the NoC switch is simulated for 32 times at various traffic patterns such as Uniform Random and Transpose. The each simulation shows less delay and less power consumption even when number of identified faults is increasing. Fig.7 shows the average latency (number of cycles) under the uniform and transpose traffic patterns for 8 8 mesh based NoC switch with 0, 1 and 2 faulty routers in the system. The proposed work reduced the latency than HiPFaR [26], E-Rescuer [24] because of two virtual channels are used for bypassing the permanent faults and the allocation of virtual channel is based on congestion paths. E-Rescuer [24] is providing limited flexibility because the default paths are allocated when permanent faults are detected. This work also tested for fault coverage when number of faults is increasing. The data packet transmission is 100% successful if NoC is fault less and slight degradation in successful transmission when faults are detected. This work shown 98% and 96% of fault coverage of one fault and two faults are detected in the NoC switch.



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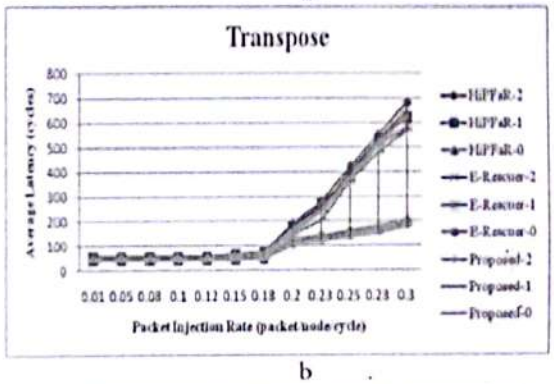

b

Fig.7 Simulation results for average latency (cycles) at different traffic patterns of 8 8 mesh based NoC switch with increasing of faulty routers

The hardware is analyzed in terms of total power consumption of circuit with virtual and without virtual channels shown in table 4. The Baseline router is using the dynamic XY routing algorithm and without bypass channels the data packets are transferring between nodes. It is using total of 8 ports (7 physical and 1 virtual) but HiPFaR [26] and the proposed work are using 6 6 input and output ports along with 2 virtual channels. The total power consumption (static and dynamic) of this paper is slightly more than HiPFaR [26] because of the states involved for allocation of virtual channels.

Table 4 Comparison of power consumption for HiPFaR [26], Baseline and proposed work

NoC	Total power consumption (W)	
	Without Virtual Channel	With Virtual channel
NoC 8-bit	1.33	4.87
NoC 16-bit	1.34	5.29
NoC 32-bit	1.42	6.19
HiPFaR[26]	-	2.39
Baseline	2.53	-

VI. Conclusion

The fault tolerance routing algorithms are aiming of high reliability and efficient communication between nodes with faulty component at NoC switch. This paper concentrates on detection and diagnosis permanent faults with BIST approach. The comparing module gives message of struck faults occurred in the communication links and two virtual channels are used for bypassing the permanent faults. Based on algorithm of virtual channel allocation, these virtual channels are selected and utilized efficiently. Initially, the NoC switch is designed and implemented of 2 2 and tested for fault coverage of this circuit thereby the 4 4, 8 8 and 16 16 mesh based NoC switch implemented and tested. The method provides 98% of fault coverage in NoC switch (16 16). In future, the reconfigurable router is design with transient and permanent faults in online and offline.

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Identity Mapping using Cluster-based Certificate technique for Vehicular Ad-Hoc Networks

Publisher: IEEE

M. Naresh ; K. Srinija ; N. Varsha ; M. Kalpana **All Authors**

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In this paper, we introduced a secure authentication technique for VANETs called Identity-Mapping using cluster-based revocation technique. In this technique, all the nodes are split into various clusters and Cluster Head is selected accordingly. The certificate authority is responsible for retracting and issuing certificates, upon the successful transmission of messages or identification of any harmful activities by any node, to the corresponding vehicles. From the simulations and comparative analysis provided in this paper, it is verified that the recommended method shows better performance when compared with the existing works.

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Identity Mapping using Cluster-based Certificate technique for Vehicular Ad-Hoc Networks

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Abstract— **In this paper, we introduced a secure authentication technique for VANETs called Identity-Mapping using cluster-based revocation technique. In this technique, all the nodes are split into various clusters and Cluster Head is selected accordingly. The certificate authority is responsible for retracting and issuing certificates, upon the successful transmission of messages or identification of any harmful activities by any node, to the corresponding vehicles. From the simulations and comparative analysis provided in this paper, it is verified that the recommended method shows better performance when compared with the existing works.**

Keywords—VANET, ID-MAP, Cluster-Based Revocation Technique

I. INTRODUCTION

Interconnection of elements is referred to as Network. In the network, all the elements may or may not interact. There are two types of networks namely, wired and wireless network. Wired network refers to the transmission of the data over a physical medium like cables, optical fibres etc. whereas wireless networks uses radio waves to transmit the data. Wireless networks encompass of wireless sensor networks, MANETs and VANETs.

In the past few years, VANETs have gained significance over the conventional modes of communication when travelling in vehicles. Vehicular ad-hoc networks, popularly known as VANETs, provide communication between vehicles and between vehicles and roadside units. Here, vehicles are treated as nodes and roadside units are treated as base stations. There are two types of communication in VANETs namely, vehicle to vehicle (V2V) and vehicle to infrastructure(V2I).

In VANETs, there must be a minimum movement of vehicles. Each vehicle communicates with each other and with the roadside unit using On-Board Unit, a wireless device loaded into the vehicles and Dedicated Short-Range communication (DSRC) protocol. Since the mode of communication is wireless, the communication links are sensitive to manipulations like changing, deleting and replaying messages. These manipulations may lead to confusion or accident while driving in traffic. To avoid these threats, the communication link must be made resistant by improving the security of message and privacy of the vehicle's identity.

The most commonly used communication protocols are UDP (User Datagram Protocol) and TCP (Transmission Control Protocol). TCP is preferred to UDP as TCP allows acknowledgments of the data being sent and received with checksum whereas UDP may take different paths and some information may be lost or sent out of order. We are using MAC (Medium Access Layer) IEEE 802.11p which regulates the data flow. Additionally, it is in charge of compensating the channel capacity in case of congestion and collisions by initializing retransmission if a jam signal is detected. CBR (Constant Bit Rate) and FTP (File Transfer Protocol) are traffic generators. FTP uses TCP for transferring packet and CBR uses UDP for transferring packet. In this paper, we are using TCP-FTP combination as communication protocols.

There are various routing protocols like reactive, proactive, geo-cast etc. In this paper we are using AODV protocol. The reactive on demand routing protocols establish the route to a particular destination only if it is needed. It minimizes the number of packets involved in route discovery by establishing routes on-demand. AODV is a reactive enhancement of the DSDV protocol.

A. Our Contribution

Contributions of the paper is given below.

a. To overcome the problems of PBAS technique proposed by Dr. Liu, a new Identity mapping authentication technique is introduced.
b. To enhance the vehicle's security and privacy, as an extension to the Identity mapping authentication technique, a new Cluster-based Revocation Authentication Technique has been proposed.

B. Organization of the Paper

Section I- Introduction to field of Wireless networks and existing problem.
Section II- provides literature survey i.e. existing methods and their drawbacks.
Section III- explains our proposed system in detail.
Section IV-provides the results and comparison between proposed and existing methods.
Section V-Conclusion

II. LITERATURE SURVEY

In 2006, Raya along with his team presented an IEEE paper on secure vehicular communication [5] in which they described about a security architecture which could prevent the security and privacy threats of VANETs but they need large storage space for the same to save the bilinear pairings. The drawback of storage space has also affected another authentication technique which was proposed by Zhang [1] and his team. Furthermore, in 2008, Zhang [8] took advantage of the identity-based cryptography to design the authentication techniques to overcome the problems faced before [4],[5]. They recommended identity-based signature technique so that the computational overhead of the RSUs can be reduced to some extent and it reassures the conditional privacy but not completely.

In 2011, Chim [12] proved that the technique presented by Zhang in 2008 is not resistant against some kinds of threats like privacy violating attacks or manipulation in messages by hackers etc. and introduced a new authentication technique based on Identity which similar to the previous ones with 2 shared keys but with a bloom filter and binary search techniques. This reduced the communication overhead by approximately 45% when compared with the Zhang's method. Lai and Lee [6] in 2013 additionally proved that the technique recommended by Zhang and his team is sensitive to repetitive or delayed messages by the attackers in the network and improved this technique further by keeping its efficiency. Horng along with his team in 2013 showed that the technique recommended by Chim and his team is not impervious to attackers resembling another vehicle's identity and they changed the phase of signing of the message in their technique so that it can satisfy the privacy and security constraints. In 2015, Shim together with his team [13] mates introduced an ID-based authentication technique which includes batch verification as a new addition. Liu accompanied by his team in 2014 proved that Shim's technique has certain drawbacks concerning the security constraints i.e. accepting an invalid batch signature. In addition to this, they also proved that shim's technique is sensitive to the modification of messages by the attackers and recommended some changes for that. In 2014, Zhang [14] along with team made some modifications in the signing algorithm of Liu's technique as it is not resistant against impersonation attack. But in 2015, Liu accompanied by his team [7], introduced a new proxy-based authentication technique to decrease the number of computations performed at the RSUs and this technique proved to be a better technique compared to all the other techniques proposed previously. It is seen that this technique can be of great advantage when larger area is taken into account. But it does not provide any resistance to attacks like impersonation, modifying, deleting or replaying the messages etc.

III. PROPOSED SYSTEM

ID-MAP technique

In this section, ID-MAP technique is specified followed by its analysis.

A. System model

Identity mapping technique comprises of 3 major active members that are as follows:

1. Trusted Authority: It is a 3rd party that produces the parameters like private key, public key and pseudo identity i.e. false identity for the vehicles and loads them into the On-Board Units which are fixed into the vehicles. In case of any malicious activity, it can find the vehicles using their false identities.
2. RSUs: They are used as an interface between the third party and the vehicles. They communicate with vehicles (mostly proxy vehicles) and checks the accuracy of the messages sent by the proxy vehicles and also by the vehicles. This information is then transmitted to the traffic control centre. Additionally, the RSUs send the data regarding the history and false identities of the vehicles including the proxy vehicles to the Trusted authority in case of any malicious activity by any of the vehicles.
3. Vehicles: The vehicles that come under certain range of the RSU are considered as proxy vehicles. Each vehicle contains an on-board unit for the purpose of transmission. The transmission takes place using the Dedicated Short-Range Communication protocol and the data transfer between the road side unit and the trusted third party takes place using the SSL (secure socket layer).

B. Security model

Identity Mapping technique has to fulfil both the security and privacy constraints [4], [8], [11], [12]:

1. Proxy vehicles and RSUs should be able to check authenticity, reliability and accuracy of the messages received.
2. Vehicles and RSUs must not be capable to extract hidden identity of a vehicle or a proxy vehicle from its messages whereas the TA can note the hidden identity of a vehicle from its message in case of any malicious activity.
3. Vehicles and RSUs must not be capable to find the interconnection between two messages sent by the same vehicle.
4. Common attacks in VANETs are forging the identity, modifying, replaying and deleting the messages by the attackers and also attacks done by damaged proxy vehicles. The identity mapping technique used must be resistant to all these attacks.

C. Details of ID-MAP

In this section, details of ID-MAP technique are described as shown in figure 1. There are five stages in this technique which are defined as follows.

Setup: In this stage, the trusted authority produces the required private and public keys and incorporates them into the on-board unit of the vehicles.

False identity generation: In this stage, each vehicle withholds its hidden identity by using the false identity and then produces its respective private key.

Message generation: In this stage, each vehicle chooses a message, sends the computed message to the proxy vehicle using timestamp.

Validation of messages by proxy vehicles: In this stage, a proxy vehicle authenticates the reliability and senders' identities from the messages received.

Validation of proxy vehicle's output by RSUs: In this stage, an RSU validates the outcome sent by proxy vehicle to notice false outcomes and retract damaged proxy vehicles.

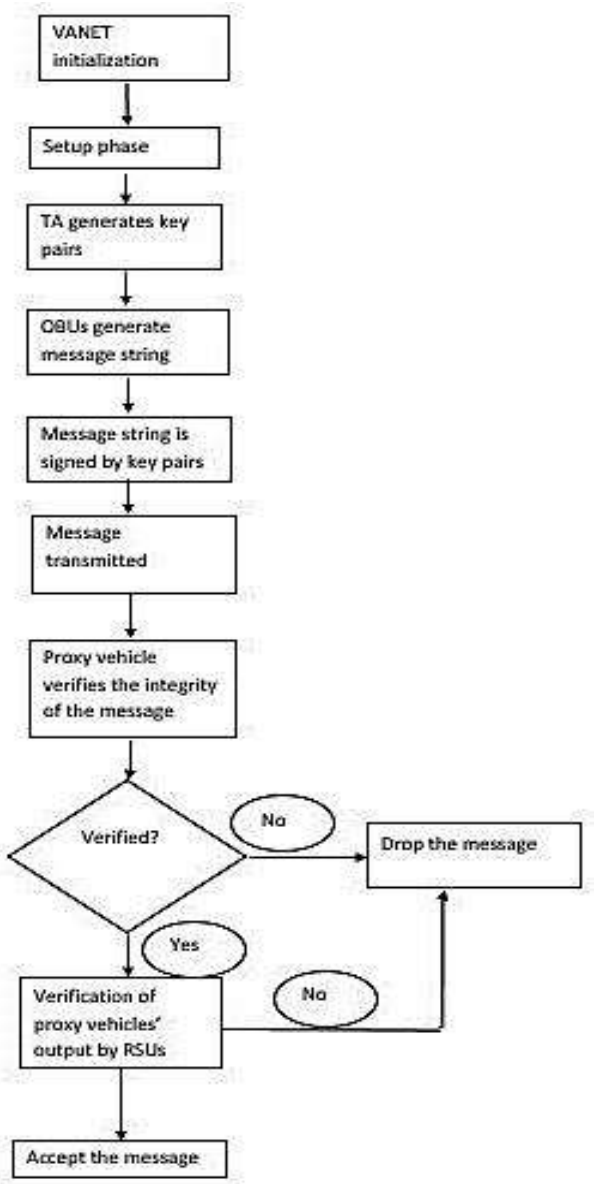

Figure 1: flowchart of ID-MAP D. Cluster based certificate technique

ID-MAP provides the security required for the vehicle's messages. To improve the vehicles identity furthermore, a cluster- based certificate technique which includes ID-MAP technique is introduced to detect the damaging nodes and completely stop their activities. It also produces effective certificates for the successful transmission of messages. In this section, the cluster-based certificate technique is introduced for VANET. The certificate authority produces the certificates of the vehicles and retracts the damaged nodes. The members in the cluster can appeal the head concerning the information about the certificates. The retracted nodes certificates are sent to the respective nodes through the RSUs and head of the cluster. Additionally, the information of the damaged and harmful node like private key and retracted certificate are stored in the certificate revocation list.

a. CH selection

Clustering is a method for segregating the entire network into several groups and then each cluster is given a head through which the interface between the members of clusters and proxy vehicles takes place. It means that the node which is at minimum distance from the other nodes in the same cluster will be designated as head.

b. Issuing certificates by CA

The basic constituents behind this function are as follows:

1. Certification authorities
2. Vehicles
3. Road-side units
4. Certificate revocation list

IV. PERFORMANCE METRICS

Performance Metrics

We have simulated the results using NS-2.35 and made a comparative analysis discussed below. Also, the simulation parameters are mentioned in the form of table refer to table 1.

Table 1 – Simulation parameters

Simulation parameters	Value
Application layer protocol	CBR
Radio range	1500 * 1500 m^2
Transmission rate	1000 bytes/0.1ms
No. of nodes	24
Routing protocol	AODV
Simulation time	9000ms
MAC protocol	IEEE 802-11 EXT
Interface queue	Queue/ DSRC
Packet size	1000 bytes
Channel data rate	20Mbps
Maximum speed	30m/s
No. of Malicious nodes	1
Data communication protocols	TCP, SINK

The merit of a routing protocol is qualitatively and quantitatively judged by the performance metrics. The following performance metrics are considered:

A. Throughput

The throughput is the maximum rate at which data can be transmitted successfully from sender to receiver. Its units are bits/sec

$$\text{Throughput} = \sum \text{received packet size/time taken}$$

Where Time taken = start time - stop time

It depends on accessible data transmission, signal-to-noise ratio and equipment constraints. The aggregate throughput is measured as the sum of the data rates which are delivered to all the terminals in a network. The comparison of Throughput for the Existing, Proposed and Extension is given in Figure 2. Here, compared to the previous techniques used, Identity mapping using cluster-based certificate technique has improved the throughput by approximately 60% with respect to Proxy based scheme and by 25% with respect to ID-MAP scheme

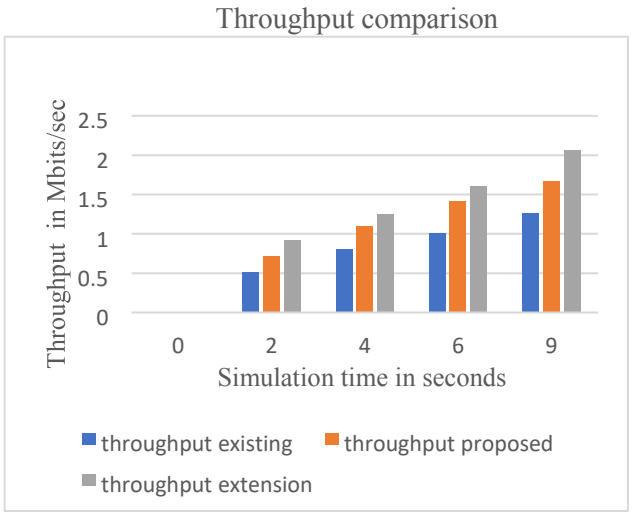

Figure 2: Comparison of throughput of existing, proposed and extension methods

B. Residual Energy

A node loses a specific measure of initial energy for each bundle transmitted and each parcel got. The initial energy utilization level of a node can be dictated by finding the distinction between the present initial energy esteem and beginning Energy_ esteem. The residual energy of a system can be dictated by summing the whole hub's residual energy in the system.

The comparison of residual energy for the Existing, Proposed and Extension is given in Figure 3. Here, compared to the previous techniques used, Identity mapping using cluster-based certificate technique has improved the residual energy by approximately 60% with respect to Proxy based scheme and by 25% with respect to ID-MAP scheme. This implies that the identity mapping using cluster-based certificate scheme is utilising less energy and reducing the computational overhead of the proxy vehicles and the RSUs.

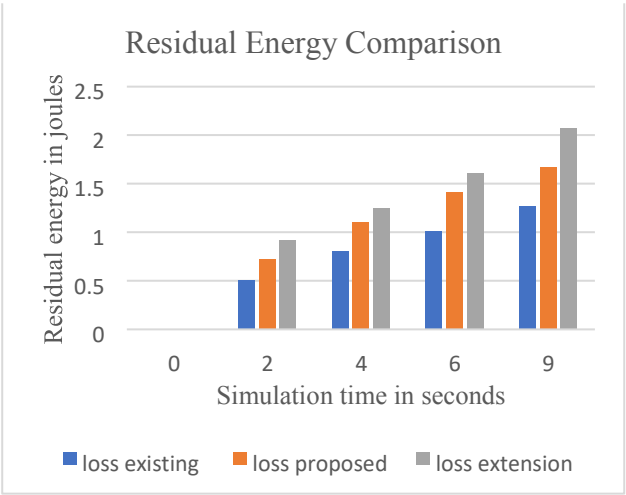

Figure 3: Comparison of energy loss of existing, proposed and extension methods

C. End-to-End Delay

Delay is computed utilizing awk content. This metric value determines the packets from point to point. The difference between the time at which a node sends out a packet and the time at which a node receives the packet is Delay. It takes into account the packet size and the time taken to send one packet.

$$\text{Delay} = (t_{received} - t_{sent})$$

Where, $t_{received}$= packet received time, t_{sent}= packet sent time.

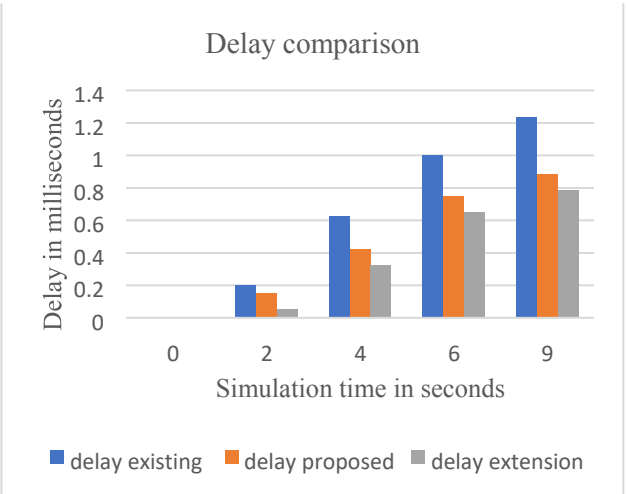

Figure 4: Comparison of delay of existing, proposed and extension methods

The comparison of residual energy for the Existing, Proposed and Extension is given in Figure 4. Here, compared to the previous techniques used, Identity mapping using cluster-based certificate technique has reduced the delay by approximately 37.5% with respect to Proxy based scheme and by 16% with respect to ID-MAP scheme.

V. CONCLUSION

To overcome the drawbacks posed by the proxy-based authentication method for VANETs, we introduced the Identity mapping for vehicular networks. This paper proves that

identity mapping is efficient when compared with proxy-based authentication method in real time scenarios. Thus, the usage of Identity mapping authentication method must be increased when number of vehicles considered are more in the coverage area of RSU. Additionally, to increase the efficiency of the identity mapping method we have introduced the cluster-based revocation method that includes the ID-MAP technique. This method is supported by the respective analysis of parameters like throughput, delay and energy loss for PBAS, ID-MAP and cluster-based revocation method.

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Link Prediction Algorithm for Efficient Routing in VANETs

Publisher: IEEE

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Abstract: Extraordinary attributes of Vehicular Ad Hoc Networks (VANETs) for instance large network sizes and quick topology changes make it hard to keep up communication links res... **View more**

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Extraordinary attributes of Vehicular Ad Hoc Networks (VANETs) for instance large network sizes and quick topology changes make it hard to keep up communication links resulting in frequent link disconnections. Since VANETs are a critical element of Intelligent Transport Systems (ITS), routing should be given in a way that fulfills any Quality of Service (QoS) limitations. In this paper, we propose a link prediction based approach to predict the duration of availability of the present path. This methodology expects to anticipate a connection breakdown before its incidence and directing the data packets through a substitute route. In order to evaluate the accessibility of an active link to the neighboring modules, we intend to make use of Newton's divided difference interpolation. In view of the data given, a substitute route will be developed even before the connection breaks when the connection is likely to collapse. Results of simulation approve the adequacy of the algorithm for the planned link prediction.

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Contents

VANETs i.e. Vehicular Ad Hoc Networks are a key part of Intelligent Transport Systems (ITS) and smart cities. They have been attracting attention from both the communities of research and industry. Each vehicle (module) in VANETs acts as a device (router) for communicating with each other without any other infrastructure support. Despite recent developments in VANETs, there are many design and implementation challenges for instance routing, privacy, security, scalability and quality of service.

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Link Prediction Algorithm for Efficient Routing in VANETs

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Keywords—VANETs, Routing, QoS, Link, Interpolation

I. INTRODUCTION

VANETs i.e. Vehicular Ad Hoc Networks are a key part of Intelligent Transport Systems (ITS) and smart cities. They have been attracting attention from both the communities of research and industry. Each vehicle (module) in VANETs acts as a device (router) for communicating with each other without any other infrastructure support. Despite recent developments in VANETs, there are many design and implementation challenges for instance routing, privacy, security, scalability and quality of service.

Position based routing protocols [3] are more suitable and stable for extensively dynamic VANET surroundings. They use the geographical positions of portable hubs and their neighboring modules to pass on data packets. However, protocols like VADD [4], GpsrJ+ and A-STAR [5] find routes using QoS past and statistical route that may not be accurate in a dynamic VANET environment.

Intersection based routing protocols, such as GyTAR [6] and TADS make use of local traffic parameters such as vehicular traffic and distribution in selecting the succeeding intersection. Yet, these parameters do not show the QoS of routing paths effectively. However, GyTAR and TADS do not take into account parallel global routing QoS which leads to a consequence i.e., in successive route selection processes, data packets may go through severe traffic circumstances.

CAR [7], a source-driven routing protocol surveys whole source-to-destination routing paths using blind flooding scheme is ineffective and usually results in huge network overhead.

AQRV, an Ant Colony Optimization (ACO) based algorithm treats the route selection problem as a controlled optimization problem with three QoS constraints namely connectivity probability, packet delivery ratio and delay. However, it neglects the lifetime of a link which may result in frequent link disconnections.

Thus, the main challenge we face is that route exploration algorithms do not take into account the lifetime of a communication link along with other QoS parameters. A link-based methodology was proposed in this paper to calculate the total time available for this route. This methodology seeks to enhance service quality (QoS) by predicting a link break before it occurs and then routing data packets through a different path. The accessibility of routes is identified by the links available between all route modules. It is therefore essential to predict the availability of links in order to calculate approximately the future availability of the route.

We intend to use Newton divided difference interpolation to calculate the available time of an active link to nearby modules approximately. Based on this data, even before the link breaks, when a link failure between two modules is likely, another path is built up. This results in reduced drops in the data packet and therefore the recovery time.

The main contribution of this paper is the development of an algorithm for predicting the total available time of a route based on QoS constraints and building an alternate path for data packets before the disconnection of the link. The main QoS parameters considered in this paper are throughput, delay and energy consumption.

The paper is structured as follows:

Literature Survey is described in Section II and proposed link prediction algorithm is elaborated in Section III. Section IV contains performance metrics, analyses and simulation results. The paper concludes with Section V.

II. Literature Survey

There are many protocols for routing that have been anticipated to resolve the issues correlated to VANETs and to sustain a variety of its applications.

A. Link Prediction Routing Algorithm

In conventional portable network and also wired-network routing algorithms, a modification in path occurs only when there is a link failure along the path or any other shortest path is found. In LPRA [1], every module saves the received signal strength and the received time of the route link request in its local memory and the predicted lifetime is updated during every period. It is updated again in the route response packet when it is returned to the destination module. Nevertheless, QoS of route does get affected with the routing protocols following this given model though it has a high number of path disconnections occurring.

B. Intersection-based routing protocols

In urban VANET situations, intersection-based routing protocols [6] are more stable. CAR uses city digital maps to find short routing paths and is not adaptable to changes in routing as it maintains complete end-to-end routes. SADV uses stationary modules to transfer data packets at road intersections so that the packets can be buffered in the stationary modules for a while until an appropriate automobile is accessible down the finest path of delivery. It is important to note that these stationary modules are not connected through a wired system, and periodic messages update the existing delay between two neighbouring intersections, which may result in congestion of the network. IEGRP [7], [8] is a hybrid vehicle routing protocol that enables uni-cast V2V or V2I communication through interactively modifying intersection routing decisions.

C. ACO-based routing protocols

Ant Colony Optimization (ACO) is based on real ants' food search behaviour [9] and can be used to resolve multi-objective issues [10]. For the following reasons, it can be used to solve VANET routing problems [11], [12] 1.) scalability: depending on network sizes, the percentage of ants in ACO might differ; 2.) adaptation: based on network changes, ants can change, die or reproduce themselves; 3.) parallelism: ant activities are naturally parallel, and this strategy enables to accelerate the convergence processes; 4.) fault tolerance: the loss of a small number of modules or connections would not lead in disastrous missteps, as ACO shows decentralized method of control. Based on the above statements, ACO meets the requirements for solving dynamic routing optimization issues in terms of exceptional adaptation, robustness and decentralized nature.

III. Link Prediction Algorithm

Here, we put forward the link prediction algorithm in detail. A path change occurs in conventional portable and wired-network routing algorithms only when there is a link failure along the path or when there is any other shortest path. A link failure is expensive as a number of broadcasting interruptions are needed to spot the breakdown and following that a fresh path has to be established, which will lead to delay in re-establishment process. Given that paths fail so rarely in wired networks, it is not a significant problem. In any case, QoS of route does get affected with the routing protocols following this given model though it has a high number of path disconnections occurring.

The algorithm of link prediction predicts the time after which an active link will break. This is done by calculating the approximate time at which data packets received signal strength falls below the specified cutoff power. The power level received below the cutoff implies that the two modules move away from one another's transmission range. The prediction of link break alerts the source sooner than the path breaks, and with the help of AQRV routing protocol, the source can find again a new path before hand, helping to optimize route setting while fulfilling QoS parameters.

A. Assumptions

For link prediction algorithm to work effectively, we presume that every automobile is provided with a Global Positioning System (GPS) feature, navigational system and digital map that provide automobiles information including speed of the automobile, direction of vehicles' movement, geographical positions of the vehicles, the intersection positions and the road segment length. Moreover, we presume that geographic locations of the particular destinations can be obtained by the source vehicles by means of location services, and different communication pairs have the same QoS requirements. AQRV aims to find the route that is optimal with the finest QoS in urban environments in terms of packet delivery ratio, delay and link lifetime.

B. Optimal Route Selection

AQRV uses two terminal modules called Terminal Intersection Source (TIS) and Terminal Intersection Destination (TID) to route data packets from source to destination. Two factors determine terminal intersections – direction of movement and its separation from neighbouring intersections. Depending on the score, whichever candidate has highest score is chosen as TIS and using the same process TID is selected. After the selection of TIS, it sends a route request in order to find an optimal route in the forms ants. These ants travelling from TIS to TID are known as forward ants. If the time taken by the forward ants to travel is greater than that of the particular module's cutoff delay, then the route request data is dropped immediately. If the time taken by the forward ant to reach the module is less than that of the cutoff delay, that forward ant is turned back and is selected to go back to TIS with the optimal route request information. These ants later are termed as backward ants. These backward ants while travelling back carry a list of intersections which are chosen depending upon the most satisfying QoS constraints. This process is repeated at each module thus creating multiple ants and the

process continues as described above. These selected backward ants get back to the TIS by travelling along the same route as travelled from TIS to TID. Finally, the optimal route among many routes is selected on the basis of scores given to each route. These scores are allotted on the basis of Quality of Service. The route satisfying QoS constraints is given highest score and is finally termed as optimal route. The flowchart for the process is shown below.

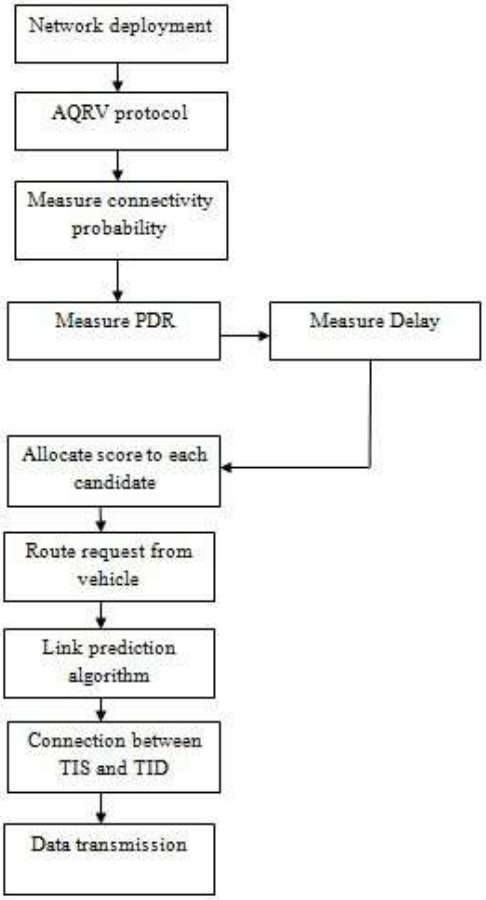

Fig1: Process of optimal route establishment

C. Link prediction

Link disconnection can be predicted by calculating the time at which power received by a module falls below a cutoff value. Since modules in VANETs are moving continuously, the power received by the receiver module decreases as modules move away and out of each other's radio ranges. In this methodology, three signal strength measurements of packets received from the previous module are taken back to back and are used to predict the failure of the link. This link failure can be calculated by means of Newton divided difference interpolation method.

Protocol requires certain duration of time to develop a new route known as critical time t. This time is sufficient to send an error to the next module and for the source to find a fresh path. 't' is a little less than 't1' which is the time taken by the link to break. The module enters a critical state after time t and must therefore find a fresh path. The upstream module tries to find a route to the destination when a connection is likely to be disconnected. If no such route is found within a given period of time known as discovery period, a link failure alert will be sent to the sources using this link. Source modules can call alternative paths to the route discovery method. At time t, the power received is enough to send an alert to the upstream module and find an alternative path either by repairing the local route around the link that will break or by building substitute paths from sources. Links broken due to decrease in received power are repaired locally in the given number of hops (j). The value of j can be taken as two, i.e. it is possible to rebuild broken links in two hops. This method of repairing the local route tries to rebuild the broken route locally, with minimal overhead control for quicker recovery. The receiving module checks the link with algorithm 1 whenever a data packet is received.

IV. Performance Metrics

The merit of a routing protocol is qualitatively and quantitatively judged by the performance metrics. We have used the following performance metrics:

A. Simulation Parameters

We use Network Simulator Version 2.35 to simulate the network in our simulation experiments,. The area of simulation is taken as 800 meters (m) x 800m which consists of 30 vehicles which move at an utmost speed of 50 meters/second (m/s). We bring into play Constant Bit Rate (CBR) to generate traffic mobility. The communication range of each module is 250 meters and the simulation runs for 10 seconds. AODV protocol is used for routing data from the source and destination module selected. Remaining simulation parameters are enlisted in Table 1.

B. Throughput

The aggregate throughput is measured as the sum of the data rates which are delivered to all the terminals in a network.

$$Throughput = \frac{\Sigma PR}{\Sigma t_{st} - \Sigma t_{sp}}$$

Where, PR = Received Packet Size, t_{st} = Start Time, t_{sp} = Stop Time. Unit – bits per second (bps)

Figure 1 shows an increase in throughput of the transmission when link prediction is used.

C. Packet Delivery Ratio

Packet delivery ratio defines the ratio of packets delivered to a destination successfully compared to the number of packets sent by the sender. The calculation of Packet Delivery Ratio (PDR) is based on the received and generated packets as recorded in the trace file. Packet Delivery Ratio is calculated using awk script that processes NS 2.35 generated trace file and produces the result as shown in figure 4.

$$PDR = \frac{Number\ of\ packets\ successfully\ received}{Total\ number\ of\ packets\ sent}$$

D. Energy Consumption

The modules involved in the network and their work are based on individual levels of energy. Here we can calculate energy levels of modules and maintain the routing. The bytes of data collected and depend on energy consumption. The network process working on lifelong must know energy consumption. The vitality display speaks to the vitality level of modules in the system. The vitality display characterized in a module has an underlying quality that is the level of vitality the module has toward the start of the reenactment. This vitality is named as initial energy. In reproduction, the variable "vitality" speaks to the vitality level in a module at any predefined time. The estimation of initial energy is passed as an information contention. A module looses a specific measure of vitality for each bundle transmitted and each parcel got. Subsequently, the estimation of introductory Energy in a module gets diminished. The vitality utilization level of a module whenever of the recreation can be dictated by finding the distinction between the present vitality esteem and beginning energy esteem. On the off chance of a module's level of vitality reaching zero, it can no longer get or transmit bundles. The measurement of the use of vitality in a hub can be imprinted in the document below. A system's vitality level cab be dictated by summing up the vitality level of the entire hub in the system. Figure 2 shows the effectiveness of link prediction algorithm in terms of energy consumption. It can be seen that the total energy consumed by link prediction algorithm is less than AQRV.

E. Delay

Delay is the distinction between the time at which the sender generates the packet and the time at which the receiver receives the packet. Delay is computed utilizing awk content which forms the follow document and delivers the outcome.

This metric value determines the packets from point to point.

$$Delay = \Sigma t_{PR} - \Sigma t_{PS}$$

Where, t_{PR} = Packet Receive Time, t_{PS} = Packet Sent Time.

$d_{end\text{-}end} = N[\ d_{trans}+d_{prop}+d_{proc}+d_{queue}]$

$d_{end\text{-}end}$ = end-to-end delay

d_{trans} = transmission delay

d_{prop} = propagation delay

d_{proc} = processing delay

d_{queue}= Queuing delay

N= number of links (Number of routers - 1)

Each router will have its own d_{trans}, d_{prop}, d_{proc} hence this formula gives a rough estimate.

Figure 3 shows the decrease in delay in AQRV and Link prediction algorithms.

Algorithm1 *Link prediction*

1: For each and every neighbor,
2: Upon reception of a packet,
3: Upgrade time, receiving power for the preceding three packets,
4: **If** ((P1>P2) as well as (P2>P3)) in that case prediction();
5: prediction()
6: {
7: Approximate and upgrade t1 and upgrade t, whenever module enters critical state, before link detachment
8: }
9: **If** (present time >= t)
10: {
11: Send alert to succeeding module,
12: Sleep for set time
13: }
14: Upon reception of rebuild message,
15: Set the route and link status as defenseless,
16: Local_route_rebuild ()
17: Local_route_rebuild ()
18:{
19: Find path to subsequent module i;
20: **If** (find path in j hops within time)
21: Use this path for rerouting
22: **Else**
23: Find path to destination D;
24: **If** (path found) {
25: Route packet through new path,
26: Send new path discovery requests to sources
27: }
28: }
29: At source:
30: {
31: Discover new path upon reception of new path discovery request
32: Redirect traffic through new path
33: }

TABLE 1: SIMULATION PARAMETERS

Parameter	Value
MAC Protocol	IEEE 802.11p
Traffic Protocol	Constant Bit Rate
Communication range R	250 m
Transmission Rate	1024 B/0.1ms
Data Packet Size	1024 Bytes
Number of Modules	30
Simulation Time	10s
Routing Protocol	AODV
Routing Method	AQRV
Channel Data Rate	10Mbps
Maximum Speed	50 m/s
Area	800m x 800m

TABLE 2: ENERGY MODEL ATTRIBUTES

Attribute	Meaning	Value	Default value
Energy model	Type of energy model	Energy model	None
rxPower	Power for receiving one packet	Power in watts (i.e.0.4)	281.8mw
txPower	Power for transmitting one packet	Power in watts (i.e. 1.0)	281.8mW
Initial energy	Energy of module in the Beginning	Energy in joules	0
Sleep power	Power consumed during sleep state	Power in watts	-
Transition power	Power consumed during state transition from sleep to idle	Power in watts	-
Transition time	Time in seconds taken during transition	Seconds	-

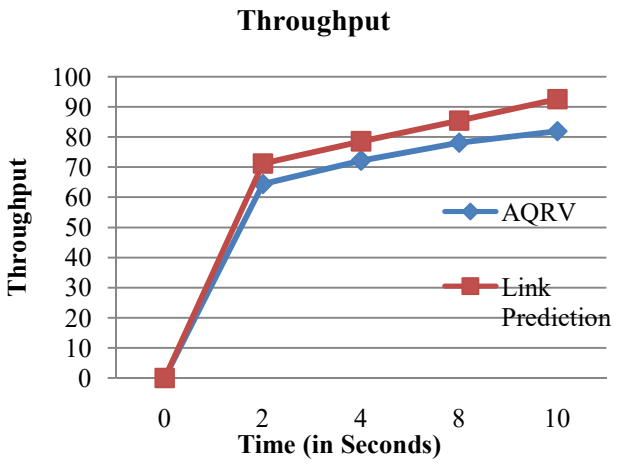

Figure 1: Comparison of Throughput of AQRV and Link prediction algorithm

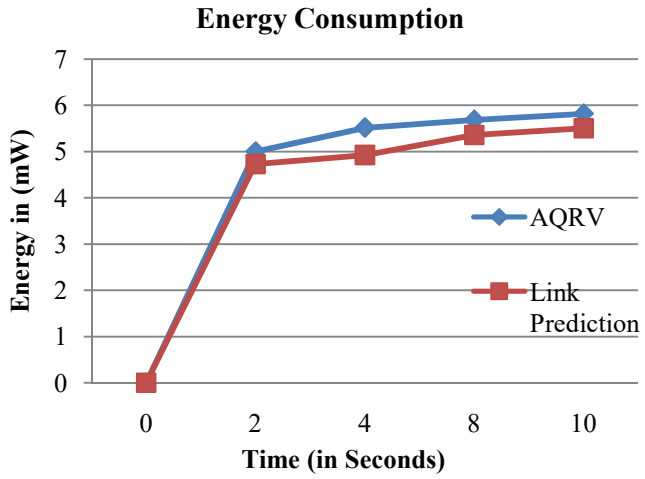

Figure 2: Comparison of energy consumed by the network using AQRV and Link prediction algorithms

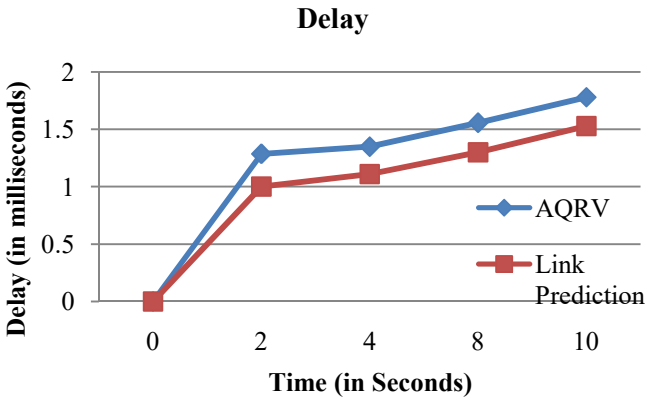

Figure 3: Comparison of end-to-end delay in AQRV and Link prediction routing

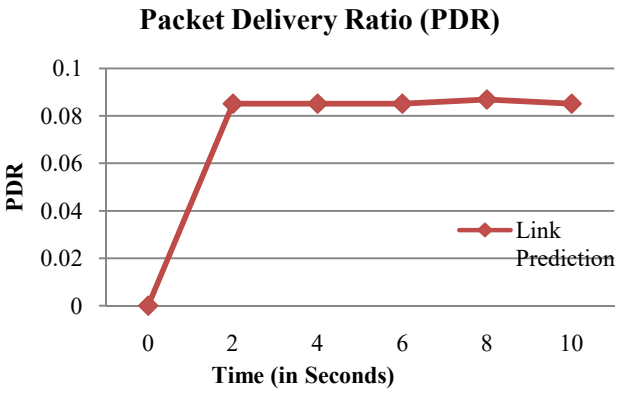

Figure 4: Packet delivery ratio using Link prediction algorithm

V. CONCLUSION

In this paper, we proposed a link prediction algorithm as an addition to the AQRV protocol that selects the best routing path in urban vehicle environmets while fulfilling certain quality-of-service requirements. Since the topology of VANETs is changing constantly, it is difficult to keep up a link between source and destination for the transfer of data. We have therefore proposed a link-based approach to predict the duration of the current route's availability . This methodology intends to improve QoS by predicting a failure in link before it occurs and routing the data packets through an alternate path. We begin the process by estimating the lifetime of link by measuring the decrease in received signal strength. Secondly,to estimate the lifetime of an active link to ts neighboring modules,we use Newton Divided Difference Interpolation method. Based on this information, when a link is about to fail, an alternate path is built up by AQRV which reduces the drops of data packets and recovery time. Finally, have validated our link prediction model through simulations and demonstrated that AQRV with link prediction performs better. This can be seen in the increase in throughput and the decrease in delay and energy consumption.

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Visiting Center Based Portable Emissary Approach for Data Gathering in Wireless Sensor Networks

Publisher: IEEE

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Abstract: Wireless sensor networks (WSNs) have been lately recognized as a trust-worthy innovation for many applications, for example, defence, ambient and physiology-monitoring. A... **View more**

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Contents

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Visiting Center Based Portable Emissary Approach for Data Gathering in Wireless Sensor Networks

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Abstract: **Wireless sensor networks (WSNs) have been lately recognized as a trust-worthy innovation for many applications, for example, defence, ambient and physiology-monitoring. A WSN includes stationing of hundreds or thousands of minor sensor hubs that communicate remotely with each other to detect explicit activities in a field of intrigue. The way towards gathering tactile information from sensor hubs and returning back to the handling unit (e.g., sink hub) is called data gathering. In network-oriented gathering, single-hop strategy involves the information being transmitted specifically from the source hub to the sink; which includes high power utilization and transmission from source hub to sink through multi-hops with other system hub as the intermediate hub or nodes. This procedure prompts data congestion, increased dormancy and high energy utilization, especially for hubs situated close to the sink, because of the gigantic measure of information stream. To mitigate these issues, a portable emissary (PE) was proposed in order to give an alternative approach for customary information gathering procedures in WSNs. Furthermore, visiting center based approach (VCBPE) is proposed with the goal that versatile hubs need not venture out to each hub for information gathering.**

KEYWORDS: Portable emissary, Hubs, Data gathering, Multi hop.

1. INTRODUCTION

Portable emissary (PE) is a software segment that moves from sink to the various hubs that need to transmit information and gathers all the information and returns to the sink. The main aim is to make this round trip productive. The fundamental hurdle with portable emissary is the high dormancy when a portable emissary needs to congregate information from a substantial system with number of hubs in thousands or beyond. So, to manage this, there are two itinerary planning approaches: single-path methodology (SPM) and multi-path methodology (MPM). SPM deals with sending just a single PE for the data gathering whereas in MPM more than one PE, depending on the number of hubs are sent. SPM has numerous impediments; high dormancy, increment in parcel estimate because of data aggregation and high packet loss as a result of migration to various hubs.

Despite the fact that MPM surmounts these impediments, it is proficient only when the path pursued by them is nearly ideal. To upgrade the itinerary there are a few proposed hypotheses. A few parameters, for example, hub energies, distance and so on are considered and the best way is then given. These path optimizations occur in two different ways, they are static optimization and dynamic optimization. In static itinerary the sink gets the information about the source nodes and consequently processes the visiting order. This order is then stacked in to the PE and the PE pursues this itinerary. Sometimes, there is an possibility of hub failure and accordingly it isn't for all intents and purposes fitting to visit that categorical hub which transpires to be an eminent disadvantage to static itinerary. In dynamic itinerary optimization, calculations to optate the following hub to visit are done at every hub once information has been fetched.

In dynamic planning, computations to choose the following hub to visit are done at every hub once information has been brought. This is valuable for applications which don't include gathering information from pre-decided source hubs. Tracking happens to be one such application. The data gathering ought to be done progressively dependent on the trace of object that we are tracking which isn't known initially.

The parameter considered to decide an optimized itinerary in the greater part of the works is constrained just to the separation between the hubs. This will negatively affect the achievement of PE's round trip. To overcome this FUMAM approach was proposed. Moreover, the investigations show even with the best ideal way the latency isn't diminished to the degree we would wish to accomplish. So, in this

paper ,we propose a visiting Centre methodology where we would exploit the merits of both multi-hop gathering and portable emissary gathering and thereby achieve a rise in the network lifetime.

Contributions of this paper as follows

1) To propose an algorithm to give an optimal itinerary to the portable emissary using a fuzzy based logic and AODV routing protocol.

2) To propose a Visiting Centre based approach to further deal with the problem of increasing dormancy when portable emissaries are used in very large networks.

The paper is organized as follows. Section 2 explains literature survey. Section-III presents the proposed VCBPE approach. Section-IV describes the performance metric evaluation and experimental results. Section-V provides the conclusion and suggests the further research direction.

II. LITERATURE SURVEY

MPM entails many SPM's working simultaneously to a group of source hubs in the assigned sequence. This visiting order has a significant impact on overall network parameters. This division discusses several algorithms given for finding the appropriate path for PE in WSN's. In [2] the authors proposed two static itinerary migration approaches namely, local nearest first (LNF) and global nearest first (GNF). In LNF, the minimum distance from the present location of PE is considered to take the next hop while in GNF shortest distance from the sink is considered. Later in [3], PE-based targeted diffusion was proposed as other alternative. It is similar to LNF but involves selection of a node that is farthest to the sink. In [5], a near-optimal itinerary design (NOID) algorithm was introduced to estimate the number of PE's and their itineraries. The distance (calculated using the MST based NOID algorithm) between the source hubs acts as the parameter for estimation of cost measure. The NOID algorithm employs a mechanism such that a source node with less energy will be visited first by the PE. In [6], the author proposed an algorithm called BSTMIP. This method allows us to have flexible authority over the trade-off between energy cost and task duration. A genetic algorithm (GA)-based MPM was proposed in [4] to compute the itineraries and the count of required PE's in MPM using a two-level coding generic based method. The code has two sub-divisions: source ordering code (sequence array), to select the visiting order in each group and a source grouping code (group array), to allocate the source hubs in the form of a group. Genetic-MPM exhibits better rendition characteristics in terms of dormancy and vitality usage.

In a large portion of the previously mentioned methodologies, the main parameters utilized to decide PE schedule are the separation among hubs and the connection cost between each pair of hubs. Different parameters, for example, the hub's outstanding vitality and the number of neighbors of the following jump hopeful, are dismissed.

Portable emissary movement will be antagonistically influenced if just the parameters of separation and vitality cost are considered. This situation will result in an profitless PE round-trip given that the intermediate hub may have lacking vitality to exchange an PE to the following hop. What's more, uneven vitality dispersal can diminish network lifetime on the grounds that a specific hub can be chosen more than once amid information gathering rounds because of its closest separation. To alleviate these issues, a fuzzy-based MA migration approach (FuMAM) is proposed in this exploration [6]. The FuMAM approach decides a proper agenda for an PE by taking in account three parameters: dormancy, remaining vitality, and the number of neighbors for every hopeful hub by utilizing a fuzzy rationale framework (FRF). The goal FuMAM approach is to expand the rate of successful PE round-trip.

Due to the high-energy efficiency and scalability, the clustering routing algorithm has been extensively used in WSNs. In order to amass information more efficiently, each sensor node transmits data to its Cluster Head (CH)(which is selected by a fuzzy logic) to which it belongs, by multi-hop communication [7]. In [8], a fuzzy logic controller that accepts the input descriptors energy, time and velocity to determine each node's role for the next duration and the next hop relay node for authentic-time packets was proposed. In [9], a genetic algorithm to predict the efficient itinerary was proposed. In [10], a proposal to increase the network lifetime by multi-hop clustering algorithm (MCH) was made . MCH selects cluster head using 2 parameters i.e. the remaining energy and node degree. In [11], a mobile agent is used to perform both data aggregation and data filtration. This approach advocates the sharing of resources and reducing the energy consumption level of sensor nodes. In [12], an algorithm of multi-agent itinerary planning to find the optimal number of distributed mobile agents, source nodes grouping, and optimal itinerary of each mobile agent for simultaneous data gathering are proposed.

In FuMAM approach, FRF is utilized to figure the PE's hop successions between every two source hubs (middle of the hubs) by figuring the likelihood of each hopeful node dependent on their info parameters. Before the sink sends PEs to the system for information gathering, it must keep up the global

data of the considerable number of hubs to segment the system and decide the meeting request of every PE for both source and intermediate hubs. The meeting request of source hubs is calculated by utilizing the LNF though the meeting request of intermediate hubs is determined by utilizing FRF.

The three parameters utilized in this examination are Remaining Energy, the distance between each candidate node and the next source node and the number of node's neighbors.

III. PROPOSED SYSTEM

The proposed framework here considers the three parameters as the contributions to decide the agenda as in FuMAM however rather than programming the PE to go to every hub in the system we allocate a couple of visiting centers furthermore, the portable emissary needs to simply go to these hubs and gather the information. The information is transmitted to these meeting centers by multi-hop transmission. The meeting centers are so picked with the end goal that they are at an ideal separate from every one of the hubs in guaranteed segment. This significantly diminishes the generally speaking vitality utilization in the system. Moreover, the inertness diminishes as the PE never again goes to every single hub (for the most part simultaneous errands happen). In this manner the network lifetime increases and the success of PE's round trip is significantly increased.

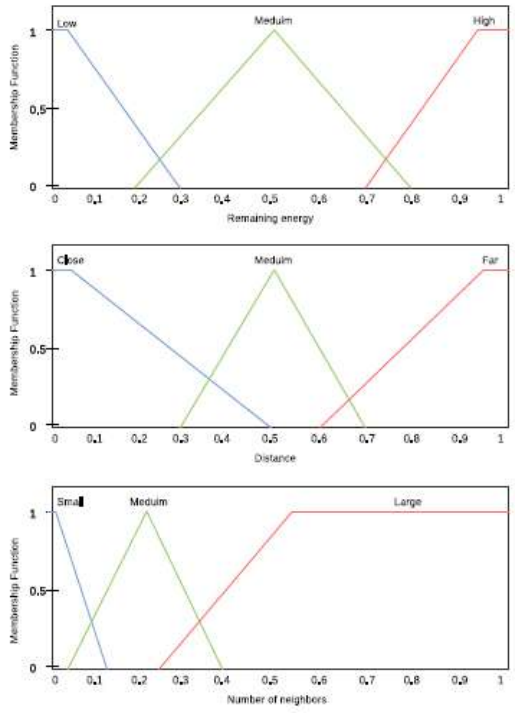

Fig 1 Input parameters

This section emphasizes the proposed VCBPE approach. The block diagram corresponding to the proposed system is shown in figure 2. Visiting center (VC) is also a node which acts as a data collecting center (it receives data from the nearby hubs). In the very first phase of this, proper network deployment is done. Network deployment includes notifying the sink about the locations of all the hubs in the network under consideration, assigning each node with a specific energy level. In the following stage, we separate the conveyed hubs into a few sub-parts and role out a meeting focus to every hub. Elements that are to be considered in this stage are

1. The meeting hubs are chosen to the point that they are at an ideal separation from all the hubs in the segment.
2. The quantity of visiting centers must be least, else the system inertness increments Count of the meeting request: The three info parameters parameters to the rationale framework that we are emphasizing about here are

1) Number of neighbors
2) Distance between the hubs
3) Energy levels at every hub

Figure1 shows the input parameters under consideration.

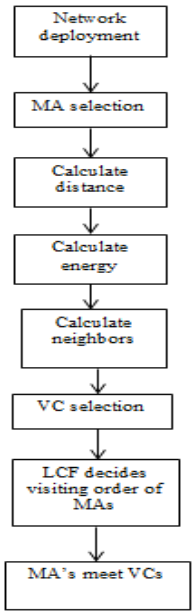

Fig 2: The Block Diagram of VCBPE approach

1) Number of neighbors:

This parameter indicates the following number of visiting centers which lie in a predefined sweep inside the area of PE. For PE's fruitful round excursion, it is critical to take into thought, every one of the parameters (remaining vitality, remove) for the neighboring hubs to choose to which VC it ought to

go straightaway. For example, there are three closest neighbors with various vitality levels. It is important that the PE should go to the VC with least vitality level first. This choice can be made just when we

2. Distance between the hubs :

Distance happens to be one of the major parameters which was considered in almost all the previous researches. It is advisable to choose the visiting center closer to the PE's current position rather than the one which is far away. The later one can induce some unnecessary delays as the portable emissary spends most of the time migrating to different VC's. Also, there is a possibility of the path being traced multiple times.

$$D=\sqrt{(Ax-Bx)+(Ay-By)}$$

Where D is the separation between sending node and candidate node, (A_x and A_y) are position of next source node and (B_x and B_y) are position of each candidate node .

3. Energy levels at each node:

Initial energy provided to each node in a WSN is the same. Whenever the node performs various sensing, data transmission operations etc. they tend to lose a part of the initially provided energy. This remaining energy at the node should be taken into consideration while deciding the visiting order. As the node with less remaining energy has a high probability of becoming inactive we need to address it first.

Energy Remaining = Initial energy - Energy consumed by all hubs

All these parameters form the input to the fuzzy logic which is written as a part of AODV protocol. AODV is a protocol which sets up a route between the center points on need premise in uncommonly selected frameworks. it is set up to perform single and multi- broadcast also known as unicast and multicast routing. The course disclosure is begun in AODV [7] by sending a course request for RREQ in the wake of checking the controlling table whether a course exists. when satisfied of the course being existent the correspondence starts. For the most part a RREQ bundle is conveyed inside the framework. exactly when the interest accomplishes the objective RREP is sent back to the source center point and centers set up forward pointers to the objective. the correspondence starts when the source center finds the solution group. the bundles are passed on irregularly from source to objective using the dynamic course. at whatever point any center stops sending packs to the objective by then course mistake RRER will be sent by the centers that see the errors. Ensuing to getting the RRER all of the center points will invigorate the information in their coordinating tables. If the source center point still needs the course it will restart the course disclosure process.

For communication, the node at source initiates the action by specifying the destination node, and checks the existing routing table for a suitable path to the destination node. In the absence of a route a Route Request is sent as a RREQ packet which is broadcasted. Nodes , having received the RREQ update the routing tables and set up forward pointers , and in case the destination is within reach , will reply with a RREP after setting the forward pointers. Otherwise broadcast the RREQ.

IV. PERFORMANCE EVALUATION

The performance evaluation is done for the three systems under consideration: traditional multi-hop system, FuMAM approach and the proposed system.

TABLE: Simulation parameters

Parameter	Value
Application traffic	CBR
Transmission rate	2048 bytes per sec
Radio Transmission range	250 meters
Packet size	1024 bytes
Maximum speed	20 m/sec
Simulation time	10 sec
Number of Source Hubs	40
Area	1000*500 m^2
Initial energy at each node	100 Joules
MAC protocol	802_11,TDMA
Routing methods	FuMAM, VCBPE
Routing protocol	AODV

The size of the network we took for simulation is 100x500sq.mts. The simulation time is 10 seconds. It seems to be very simple but as the time scale is in nano-seconds even 10 seconds simulation time can give results required. Number source hubs are taken to is sent back to the source center point and centers be 40. This number can go as high as 10000 or even more. The tool used for this simulation is Network Simulator version 2. The node deployment is random i.e; it the distance between the hubs is not uniform throughout. The sink is placed at one extreme end

and the portable emissary starts from the sink with a migration speed of about 20m/sec.

All these approaches use three performance metrics: total energy consumption, delay and throughput. We are plotting an cumulative mean of 50 simulation runs for each point represented in the plots.

Now, let us consider the trade-off between the energy dissipation and network lifetime. In a real-time scenario, each network node is given with fixed energy and once this energy is lost the hubs become inactive. Majority of the energy is consumed during data transfer operations. The main aim of our proposed system is to reduce such vitality usage and thereby improve the system lifetime.

Though the energy consumption and data congestion are reduced in FuMAM approach compared to all the other data gathering techniques, the overall delay is greatly increased when a portable emissary has to visit a large number of hubs. The overall delay is the sum of delays at individual hubs and the total time taken to move to different network hubs. To overcome this problem we are going to visiting center approach. The experimental results happen to support the above theory which is shown in figure 3

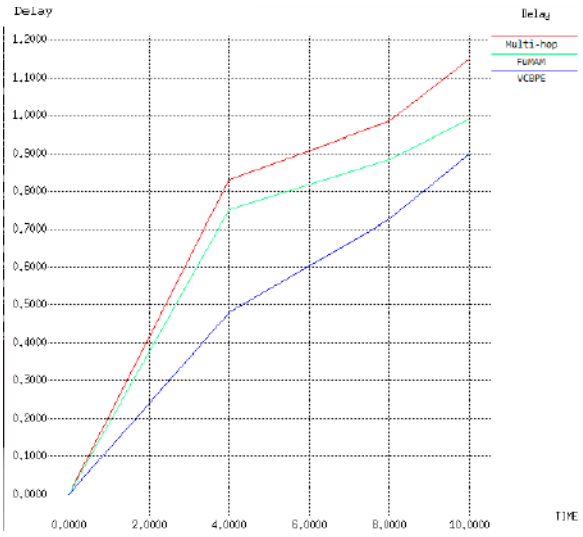

Fig 3 :Comparison of overall delay between multi-hop, FuMAM and VCBPE

End to End Delay= ∑tPR-∑tPS Where, tPR – Packet Receive Time, tPS – Packet Sent Time.

Dend-end= N[dtrans + dprop + dproc + dqueue]

The graph in figure 4 shows the energy consumption with time. It can be clearly observed from the graph that existing multi-hop technique has got a relatively greater energy consumption because of the transmission of data from a far-off point to sink through intermediate hubs also consumes a lot of energy. Coming to FuMAM approach the characteristic shows an improvement. The proposed method happens to show the best result in comparison.

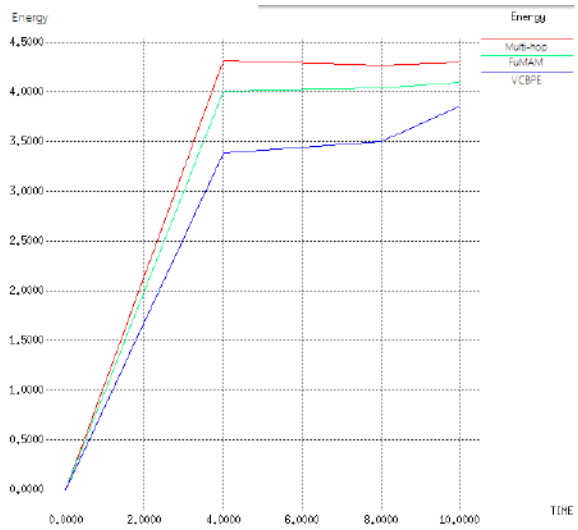

Fig 4: Comparison of Energy Consumption between multi-hop, FuMAM and VCBPE

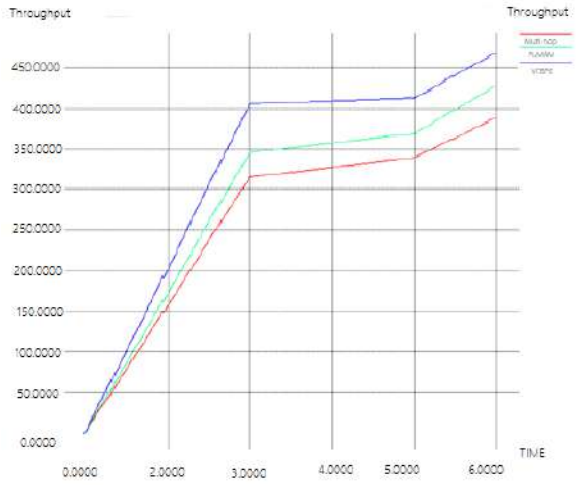

Fig 5 :Comparison of Throughput between multi-hop, FuMAM and VCBPE

The throughput of the framework is high in VCBPE approach contrasting and FUMAM and multi hop approach on the grounds that at the point when multi hop is brought through extensive number of hubs because of blockage the proficiency of information is decreased thus throughput is less while in FUMAM the PE ought to go to each hub to gain admittance to the information by that interim PE may lose its vitality or there might be bundle drops which prompts information misfortune consequently

throughput is similarly high in VCBPE approach. This is shown in Fig 5.

Throughput = ΣPR/Σ(tst)- Σ(tsp) Where, PR – Received Packet Size, unit-bps

V.CONCLUSION

The current data gathering systems have three issues in particular, data aggregation, high energy utilization and increased dormancy. To mitigate these issues, numerous PE based algorithms were put-forth. These calculations took just the separation between the hubs as a parameter for giving the ideal itinerary to the portable emissary(s). This lead to certain entanglements in the event of node failures. FuMAM approach was as of late proposed to mitigate these issues. It considered three parameters in particular, number of neighbors, remaining energy and separation between hubs. This helped us to achieve optimize itinerary. However, the principle issue with this framework is that even with the most optimized path the PE visiting every single node in a huge system can offer ascent to tremendous delay values. To avoid this, the proposed visiting center based methodology is compelling. The PE instead of migrating to every single hub it goes to the VC and assembles the data that originate from the nearby hubs. Extensive simulation results further second the above claim. As all the above issues with the current frameworks have been addressed, the network life time is enormously increased.

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Implementation of the Standard Floating Point DWT Using IEEE 754 Floating Point MAC

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Abstract

This work concentrates mainly for the implementation of Standard DWT using IEEE 754 floating point format. Currently, in the signal processing, for audio purpose the fixed point DWT is used as audio CODEC [1]. The main bottleneck of the fixed point DWT or the traditional DWT is the speed because at the input of the fixed point DWT the over-sampled ADC which is the Sigma-Delta ADC is used. The Sigma-Delta ADC can't give the speed more than 1 MHz because as the sampling rate increases, the step size decreases so that it takes more time to follow the analog signal which causes the limitation of the speed. Due to the speed limitation of ADC, the whole audio CODEC system which was designed by the fixed point DWT becomes slow even it has the capability to operate with a better speed. Hence, to optimize the system the FIR filters which are used to constitute the standard floating point DWT have been implemented in VLSI.

Keywords

DWT IEEE 754 floating point Audio CODEC Sigma-Delta ADC

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Personalised recommendations

Implementation of the Standard Floating Point DWT Using IEEE 754 Floating Point MAC

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Abstract. This work concentrates mainly for the implementation of Standard DWT using IEEE 754 floating point format. Currently, in the signal processing, for audio purpose the fixed point DWT is used as audio CODEC [1]. The main bottleneck of the fixed point DWT or the traditional DWT is the speed because at the input of the fixed point DWT the over-sampled ADC which is the Sigma-Delta ADC is used. The Sigma-Delta ADC can't give the speed more than 1 MHz because as the sampling rate increases, the step size decreases so that it takes more time to follow the analog signal which causes the limitation of the speed. Due to the speed limitation of ADC, the whole audio CODEC system which was designed by the fixed point DWT becomes slow even it has the capability to operate with a better speed. Hence, to optimize the system the FIR filters which are used to constitute the standard floating point DWT have been implemented in VLSI.

Keywords: DWT · IEEE 754 floating point · Audio CODEC · Sigma-Delta ADC

1 Introduction

To overcome the limitation of the speed of Sigma-Delta ADC, it has to be replaced by the logical connection instead of the physically connected Sigma-Delta ADC between the audio source and the fixed point DWT. The logical connection is provided through the development of user defined float point package using IEEE 754 standard and compile with IEEE standard library of digitally define tool. DWT designed in this manner is called Standard floating point DWT. To such floating point DWT, the audio source which is in the form of analog is converted into IEEE 754 standard and applied at the input using a test-bench. This floating point DWT be designed with floating point FIR filters. The floating point FIR filters are designed by floating point MAC [1]. Such MAC is designed by the floating point adder and floating point multiplier along with shifter. These floating point arithmetic operators are designed by the user defined

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floating point library package [2]. With all such topics, this chapter explains the complete implementation issues of the Standard floating point DWT using IEEE 754 format. At the end of the work, various results of the standard floating point DWT are also illustrated.

2 Traditional 3-Stage DWT and Its Limitations

Traditional fixed point DWT functions with fixed-point MAC and its MAC has been designed through fixed point adder and multiplier along with a shifter. Because, it operates along with the sigma-delta analog to digital converter and digital to analog converter at the input side and output side of the fixed point DWT correspondingly, the first drawback of the traditional DWT is speed [3]. The sigma-delta analog to digital converter is used to alter the analog signal to the digital signal. Sigma-delta operates with oversampling rate which means that the sampling rate is more than twice to that of the maximum frequency component of the signal. When it is oversampled, the number of step sizes are more which will take more time to follow the analog signal. Likewise the speed will be less [4].

The second bottleneck of the traditional DWT is, db4 co-efficients are actually in floating point hence these should be transformed into the fixed point using various scale parameters before and after the computation. At the end the results are scaled down by the same parameter [5], due to which the system may obey the non-linear property and hence there may be a chance to decrease the system stability.

3 Realization of Standard Floating Point DWT for 3 Stage Using Filter Bank Approach

The primary objective of this research is to design the 3-stage floating point audio CODEC using floating point DWT. As the floating point DWT is constituted by the filter bank and it has been implemented by the sub-band coding advance as given in the following sections [6].

3.1 Sub-Band Coding

Sub-band coding can be explained with the successive decomposition of input signal through filter bank. The discrete wavelet transform crumbles a signal to a set of dissimilar resolution sub-signals correspond to the different frequency bands. It results in a multi-resolution representation of signals with localization in both the spatial and frequency domains [7]. It is attractive in the case of signal compression, but it is not possible in the case of Fourier Transform which gives good localization in one domain at the expense of other. Sub-band coding is a process in which the input signal is divided into various frequency bands. The filter bank is a compilation of filters which are having a similar node either at output or input. If filters have a common node (N) at the output, they form the synthesis bank and when they share a common node (N) at the input, they form the analysis bank which is shown in Fig. 1. The fundamental concept of filter bank is divide a signal equally at the frequency domain [8, 9].

3.2 Perfect Reconstruction Filters

The above Fig. 1 shows the two-band analysis cum synthesis filter bank system. In the analysis bank $H_0(z)$ and $H_1(z)$ are the low pass and high pass FIR filters respectively. Similarly, in the synthesis filter bank $F_0(z)$ and $F_1(z)$ are the low pass and high pass FIR filters respectively. From the above Fig. 1 the final output X(Z) is given by

$$\begin{aligned} X(Z) &= 1/2[H_0(Z)F_0(Z) + H_1(Z)F_1(Z)]X(Z) \\ &\quad + 1/2[H_0(-Z)F_0(Z) + H_1(Z)F_1(Z)]X(-Z) \end{aligned} \tag{1}$$

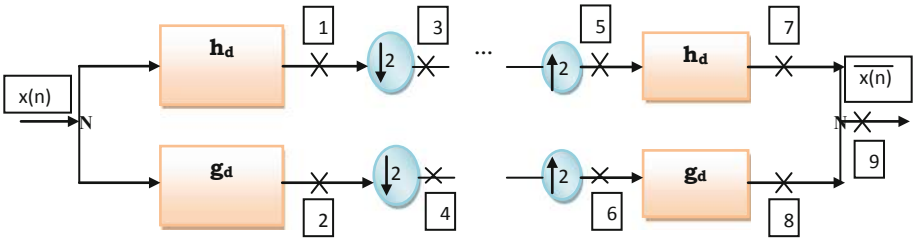

Fig. 1. A two band analysis cum synthesis filter bank system

Alias can be cancelled by choosing the filters such that the quantity in Eq. 6.9, $H_0(-Z)\ F_0(Z) + H_1(-Z)\ F_1(Z)$ is zero [9].

Thus the following choice cancels aliasing.

$$\begin{aligned} F_0(Z) &= H_1(-Z) \\ F_1(Z) &= -H_1(-Z) \end{aligned} \tag{2}$$

For the $H_0\widehat{(z)}$ and $H_1(z)$ it is possible to completely cancel the aliasing by the choice of synthesis filters [10].

In the matrix form expression1 can be written as –

$$z.\ \widehat{x(z)} = [x(z)\ .\ x(-z)\ ] \begin{bmatrix} H0(Z) & H1(Z) \\ H0(-Z) & H1(-Z) \end{bmatrix} \begin{bmatrix} F0(Z) \\ F1(Z) \end{bmatrix}$$

$$H(z) = \text{Alias component matrix}$$

The matrix H(Z) is called the aliasing component (A.C) matrix. The term which contains X(−Z) originates because of the decimation. On top of the unit circle, $X(-z) = X\left(e^{j(w-n\square)}\right)$ which is a right shifted version of $X(e^{jw})$ by an amount of $\prod$. This term takes into account aliasing due to the decimators and imaging due to the expanders [11]. It could be referred this just as the alias term or alias component.

3.3 Elimination of Aliasing Effect

When the input signal to the decimator is not band-limited, then the spectrum of decimated signal has aliasing. Hence, the input signal should be band-limited to π/D, where D is the decimator.

3.4 FIR Filters

For the multi-rate signal processing, FIR filters are chosen than IIR filters because

(1) FIR filters are stable
(2) FIR filters can be designed with exactly linear phase
(3) Limit cycles are not produced in the FIR filters since these filters are not having feedback [12].

FIR filters can be designed using three techniques i.e.,

(1) Fourier series technique
(2) Frequency sampling technique
(3) Window technique

Because, in this research Daubechies-4 window which is suitable for audio applications is used, the design of FIR filter using window technique is illustrated here.

3.4.1 FIR Filter Using Window Technique

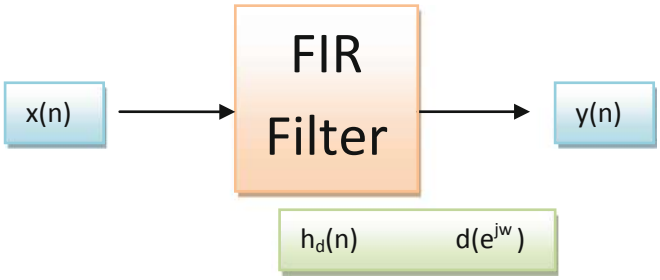

Fig. 2. FIR filter

The above Fig. 2 shows the FIR filter. In Fig. 2

$$\begin{aligned} h_d(n) &= \text{Fourier coefficients having infinite length} \\ &= 1/2\pi \int_{-\pi}^{\pi} H\left(e^{jw}\right) \cdot e^{jwn} dw \end{aligned} \tag{3}$$

$$\begin{aligned} H_d(n) &= \text{Fourier series representation of } h_d(n) \\ &= \sum_{n=-\infty}^{\infty} hd(n) \cdot e^{jw} \end{aligned} \tag{4}$$

3.4.2 Daubechies Wavelet Co-efficients

Because of the 3-stage Standard floating point audio CODEC is to be implemented by DWT using multi-rate analysis, the window size is not fixed which means that analysis is to be done for different frequency bands by the high pass and low pass filters with the different resolutions by the decimators. As the specifications are changed window to window, a superior exercise is required to find the resultant filter co-efficients. After a lot of exercise, Prof. Ingrid Daubechies, had invented the low pass and high pass filter co-efficients for various applications and released for the public domain. It is important to note that the objective of this research is not to introduce the wavelet concepts starting from the scratch, but to present the application of wavelet in the field of signal compression such as in audio applications. But, in general to find the order of the filter (N); the transition frequency (Δf), sampling rate (fs), pass band attenuation ($\square_p$), stop band attenuation ($\square_s$) are required. If the response of the low pass filter is considered with various specifications as given below,

f_s = sampling rate
Δf = transition frequency
$\square_p$ = pass band attenuation
$\square_s$ = stop band attenuation

The order of the filter (N) could be found with the empirical relation as given below:

$$\begin{aligned} &\Delta f_{min} = f_s/N \text{ or} \\ &\Delta f \approx f_s/N * [\text{Atten(db)} - 8]/14 \text{ or} \\ &N = f_s/\Delta f * [\text{Atten(db)} - 8]/14 \end{aligned} \tag{5}$$

There are different mother wavelets like db2, db4 and db6 etc., which are invented by Prof. Ingrid Daubechies and for each one, there is a specific application. Some of the basic wavelets are explained as given below.

db2 Wavelet

db2 wavelet is also called Haar wavelet. It has 2 vanishing movements.

db4 Wavelet

As the name itself, db4 is having the four vanishing movements. It is specified for the audio applications. The filter co-efficients are extracted from the Matlab command as given below:

?[L.H] = orthfilt(dbwavf('db4'))

$$L = -0.1294 \quad 0.2241 \quad 0.8365 \quad 0.4830$$
$$H = -0.4830 \quad 0.8365 \quad -0.2241 \quad -0.1294$$

db6 Wavelet

It has 6 vanishing movements. It is used for C.T scan to identify the tumors by EEG and ECG.

3.4.3 Stage Standard Floating Point DWT Implementation

This section illustrates the implementation of the Standard floating point DWT decomposer and the DWT re-constructor.

Standard DWT Decomposer and Re-constructor

Figures 3 and 4 show the 16 bit floating point Standard DWT decomposer and re-constructor respectively. Its operation is explained in the below sub-sections.

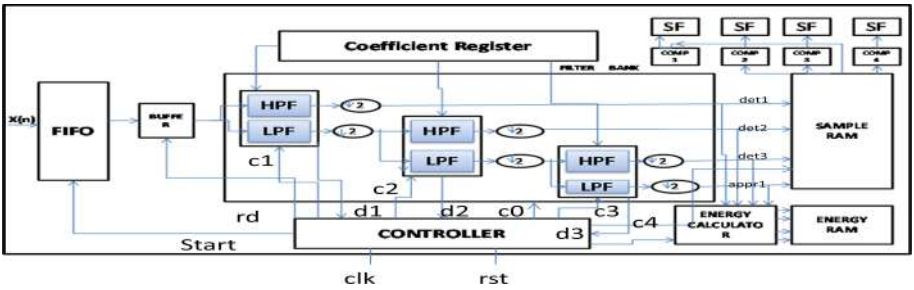

Fig. 3. 16-bit floating-point decomposer

The proposed 16-bit Standard floating-point DWT consists of various modules [5]. Each module can be explained in the below sub-sections.

FIFO

This module takes the signal sample and stores in the memory location. Once the FIFO module gets filled up the stored data is approved to the input buffer module. The FIFO module accepts the data when start signal goes high and passes data out to the input buffer module under read signal going high. The FIFO consists of 16 locations and passes out parallelly 16 samples of data at a time to the buffer module.

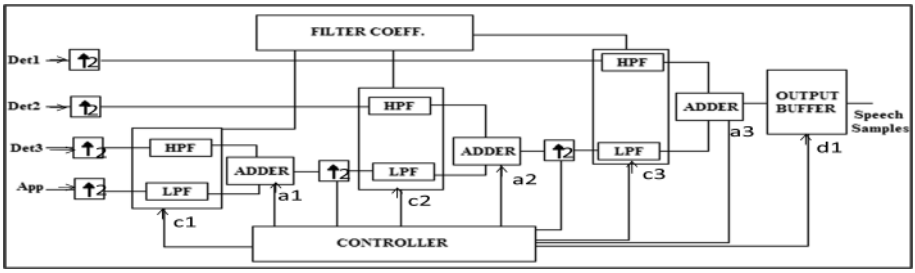

Fig. 4. 16 bit floating point re-constructor

Input Buffer

The module takes the data from the FIFO unit and packetizes the data and passes to the filter bank module. On every system clock the module passes out four samples each to the data transfer to attain synchronization between the data received and the filter bank operation.

Filter Bank

The Standard floating point DWT design consists of the core unit as the filter bank, which contains three banks of high-pass and low-pass filters. The filters decompose the input-signal samples into various sub bands depend upon the filter co-efficients sent to it.

Filter Stack

The filter stacks are the sub-modules of the filter bank where a pair of high-pass and low-pass filters are embedded into it. The high pass filter performs convolution operation between the input signal and the filter co-efficient passed from the co-efficient register. The convolution operation is carried out by the implementation of a floating point multiplier and a floating point adder module followed by shifting operation.

The high pass filter extracts the upper frequency components from the signal that get decimated by 2. The obtained samples are then passed down to SRAM unit where the samples get stored into the memory unit. The high pass unit gives the detail co-efficients and the low pass filter gives the approximate co-efficients which get further decomposed into its individual components. The low pass filter carries out the operation similar to high pass filter.

Controller

The controller is the control unit of the standard DWT design. It generates the control signals to different modules for its proper functionality. The controller reads the status of the filter stack as d1, d2 and d3 signal and generates appropriate control signals to the filter stack for its proper functioning. The controller gives the start signal to the FIFO unit when the system is reset and on the completion of FIFO filling generates a control signal to energy RAM and sample RAM to store the obtained samples and their energy.

Co-efficient Register
This unit holds the filter co-efficients for the filter unit and passes the co efficients to the filter bank for its operation.

Sample RAM
The detail and approximate co-efficients obtained from the filter bank are stored into the sample RAM unit. Sample RAM unit consists of 9 × 4 memory location to store the sub band samples. Each band is stored separately in sequence in the memory location.

Energy RAM
This module calculates the energy of each sample unit. The energy of a sample is calculated as square of the magnitude sample.

Comparator
The comparator module compares the obtained detail co-efficients and approximate co efficient elements in each sub band and finds the highest value in every sub band. The obtained value is the scale-factor for that sub band stored as Sfac1, Sfac2, Sfac3 and Sfac4.

Operation
The samples of the speech or audio whichever is to be processed that should be applied at the input of the FIFO of Fig. 3. As soon as controller sends the start signal to FIFO, it commences to accept the samples from the input. Because, FIFO length is 16 × 16, it stores the maximum of sixteen samples with the 16-bit length of each. Whenever FIFO is filled by the 16 samples it sends the first 4 samples to the buffer. From the buffer, the four samples are applied to the first section of the high pass filter and low pass filter of the filter bank. The low-pass and high-pass filters perform convolution operation between the input samples which come from the buffer and the high pass filter co-efficients from the co-efficient register. After convolution, HPF sends its output to the decimator. The decimator reduces the number of samples by 2 and then sends its output to the sample RAM. The components stored in this manner in sample RAM through the first section of the HPF are called detail1 components or det1. In the similar way, the convolution operation is carried out by the first section of the LPF between the samples come from the buffer and the low pass co-efficients from the co-efficients register. The output of the LPF is sent to the decimator for the decimation process. It reduces the number of samples to the half and sends its output to both HPF and LPF of the second section. After convolution, the outputs of the HPF which are called detail2 (det2) components, stored in the sample RAM and the outputs of the LPF are applied to the decimator. After decimation process, these will be applied to the third section of the HPF and LPF. The HPF performs the convolution operation and sends the detail3 (det3) components to sample RAM and the output of the LPF which are approximate components (appr1) are also sent to store in sample RAM at the end.

The comparator (comp) compares the respective detail and approximate components and sends the maximum component to the scale factor (SF) section. The reconstructor reads the detail components and approximate component from the scale factor section of the 16-bit floating point decomposer of Fig. 4. In the reconstructor side interpolators are used to obtain the samples which were dropped by the decimator during transmission. In the same way, adders are used to reconstruct the high pass and low pass filters' output. The reconstructor operation is exactly vice-versa to the decimator operation. At the output of reconstructor, the same signal of x(n) which was applied near the input of decomposer could be observed.

4 Results

This part presents the simulation and synthesis outcome of Standard floating point DWT.

Standard Floating-Point DWT

The simulation for the Standard-floating point DWT design is carried-out by the Modelsim 10.3cl. Since, the Modelsim has not the floating point packages, the customer defined floating point library packages are implemented and added with the standard library of the Modelsim tool. Now by porting the 16-bit floating point values using the testbench, the output would be obtained as shown in Fig. 5.

Simulation Results

Table 1 shows the simulation results of the Fig. 5 at particular instant of time t1 in binary. For easy understanding the same Table 1 was shown in Table 2 in decimal which states that the error is zero between the transmitted (input) and the received (output) values.

Table 1. Using floating-point binary values

Figure	At time	Input value (Binary)	Output value (Binary)	Error
5	t1	1000010000110110	1000010010110110	Zero

Table 2. Using floating point decimal values

Figure	At Time	Input value (Decimal)	Output value (Decimal)	Error
5	t1	$-7.6444 * 10^{-06}$	$-7.6444 * 10^{-06}$	Zero

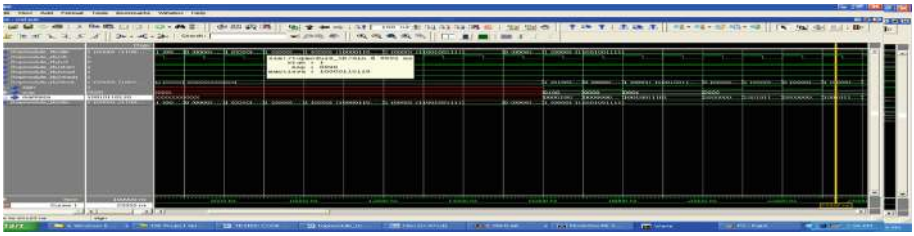

Fig. 5. The input and output values of the standard floating point DWT at particular instant of time say t1

Synthesis Results

The synthesis is developed by Xilinx Synthesis Technology (XST) tool. The chosen hardware device is Xc2s50e-ft256-6. The speed rating is −6. In this machine, the maximum number of IOs are 182 and the maximum number of BELs are 1728.

Figure 6a shows the top module of the Standard floating point DWT with pins from 0 to 15 among which 0 to 10 range is for the mantissa, 0 to 3 range is for exponent and 1-bit for sign. Figure 6b shows that internal RTL structure between FIFO and buffer. Figure 6c–d show the overall RTL diagrams of the Standard floating point DWT.

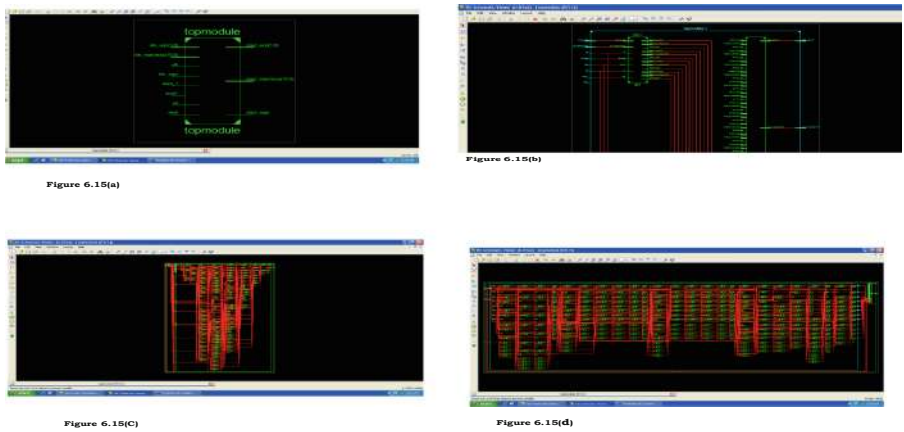

Fig. 6. RTL diagrams of standard-floating-point DWT

Synthesis Details

By the Table 3, it is known that the attained speed of the Standard floating-point DWT is 377.501 MHz through the power utilization and delay of 38.64 mw plus 2.649 ns respectively. The hardware resources that were taken by the Standard floating point DWT be 57% of IOs and 11.8% of BELs.

Table 3. Synthesis results for Standard floating-point DWT

Hardware parameters	Standard DWT
No. of IOs	105 out of 182 (57%)
No. of BELs	205 out of 1728 (11.8%)
Min. period	2.649 ns
Maximum speed	377.501 MHz
Power utilization	38.46 mW

5 Conclusion

The Standard floating-point DWT had been realized here is by the consumer defined floating-point – library-package with IEEE 754 standard. In the fixed-point DWT, the ADC and DAC need to be used physically but by develop the user defined floating-point package, a logical link had been given between source and DWT instead of physically connected data converters. To the Standard floating point DWT half precision is used; in which 1 bit is used for sign, 4-bits are used for the exponential and 11 bits are allotted for the mantissa.

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Implementation of the Standard Floating Point DWT Using IEEE 754 Floating Point MAC

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Abstract

This work concentrates mainly for the implementation of Standard DWT using IEEE 754 floating point format. Currently, in the signal processing, for audio purpose the fixed point DWT is used as audio CODEC [1]. The main bottleneck of the fixed point DWT or the traditional DWT is the speed because at the input of the fixed point DWT the over-sampled ADC which is the Sigma-Delta ADC is used. The Sigma-Delta ADC can't give the speed more than 1 MHz because as the sampling rate increases, the step size decreases so that it takes more time to follow the analog signal which causes the limitation of the speed. Due to the speed limitation of ADC, the whole audio CODEC system which was designed by the fixed point DWT becomes slow even it has the capability to operate with a better speed. Hence, to optimize the system the FIR filters which are used to constitute the standard floating point DWT have been implemented in VLSI.

Keywords

DWT IEEE 754 floating point Audio CODEC Sigma-Delta ADC

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Implementation of the Standard Floating Point DWT Using IEEE 754 Floating Point MAC

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Abstract. This work concentrates mainly for the implementation of Standard DWT using IEEE 754 floating point format. Currently, in the signal processing, for audio purpose the fixed point DWT is used as audio CODEC [1]. The main bottleneck of the fixed point DWT or the traditional DWT is the speed because at the input of the fixed point DWT the over-sampled ADC which is the Sigma-Delta ADC is used. The Sigma-Delta ADC can't give the speed more than 1 MHz because as the sampling rate increases, the step size decreases so that it takes more time to follow the analog signal which causes the limitation of the speed. Due to the speed limitation of ADC, the whole audio CODEC system which was designed by the fixed point DWT becomes slow even it has the capability to operate with a better speed. Hence, to optimize the system the FIR filters which are used to constitute the standard floating point DWT have been implemented in VLSI.

Keywords: DWT · IEEE 754 floating point · Audio CODEC · Sigma-Delta ADC

1 Introduction

To overcome the limitation of the speed of Sigma-Delta ADC, it has to be replaced by the logical connection instead of the physically connected Sigma-Delta ADC between the audio source and the fixed point DWT. The logical connection is provided through the development of user defined float point package using IEEE 754 standard and compile with IEEE standard library of digitally define tool. DWT designed in this manner is called Standard floating point DWT. To such floating point DWT, the audio source which is in the form of analog is converted into IEEE 754 standard and applied at the input using a test-bench. This floating point DWT be designed with floating point FIR filters. The floating point FIR filters are designed by floating point MAC [1]. Such MAC is designed by the floating point adder and floating point multiplier along with shifter. These floating point arithmetic operators are designed by the user defined

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floating point library package [2]. With all such topics, this chapter explains the complete implementation issues of the Standard floating point DWT using IEEE 754 format. At the end of the work, various results of the standard floating point DWT are also illustrated.

2 Traditional 3-Stage DWT and Its Limitations

Traditional fixed point DWT functions with fixed-point MAC and its MAC has been designed through fixed point adder and multiplier along with a shifter. Because, it operates along with the sigma-delta analog to digital converter and digital to analog converter at the input side and output side of the fixed point DWT correspondingly, the first drawback of the traditional DWT is speed [3]. The sigma-delta analog to digital converter is used to alter the analog signal to the digital signal. Sigma-delta operates with oversampling rate which means that the sampling rate is more than twice to that of the maximum frequency component of the signal. When it is oversampled, the number of step sizes are more which will take more time to follow the analog signal. Likewise the speed will be less [4].

The second bottleneck of the traditional DWT is, db4 co-efficients are actually in floating point hence these should be transformed into the fixed point using various scale parameters before and after the computation. At the end the results are scaled down by the same parameter [5], due to which the system may obey the non-linear property and hence there may be a chance to decrease the system stability.

3 Realization of Standard Floating Point DWT for 3 Stage Using Filter Bank Approach

The primary objective of this research is to design the 3-stage floating point audio CODEC using floating point DWT. As the floating point DWT is constituted by the filter bank and it has been implemented by the sub-band coding advance as given in the following sections [6].

3.1 Sub-Band Coding

Sub-band coding can be explained with the successive decomposition of input signal through filter bank. The discrete wavelet transform crumbles a signal to a set of dissimilar resolution sub-signals correspond to the different frequency bands. It results in a multi-resolution representation of signals with localization in both the spatial and frequency domains [7]. It is attractive in the case of signal compression, but it is not possible in the case of Fourier Transform which gives good localization in one domain at the expense of other. Sub-band coding is a process in which the input signal is divided into various frequency bands. The filter bank is a compilation of filters which are having a similar node either at output or input. If filters have a common node (N) at the output, they form the synthesis bank and when they share a common node (N) at the input, they form the analysis bank which is shown in Fig. 1. The fundamental concept of filter bank is divide a signal equally at the frequency domain [8, 9].

3.2 Perfect Reconstruction Filters

The above Fig. 1 shows the two-band analysis cum synthesis filter bank system. In the analysis bank $H_0(z)$ and $H_1(z)$ are the low pass and high pass FIR filters respectively. Similarly, in the synthesis filter bank $F_0(z)$ and $F_1(z)$ are the low pass and high pass FIR filters respectively. From the above Fig. 1 the final output X(Z) is given by

$$\begin{aligned} X(Z) &= 1/2[H_0(Z)F_0(Z) + H_1(Z)F_1(Z)]X(Z) \\ &\quad + 1/2[H_0(-Z)F_0(Z) + H_1(Z)F_1(Z)]X(-Z) \end{aligned} \tag{1}$$

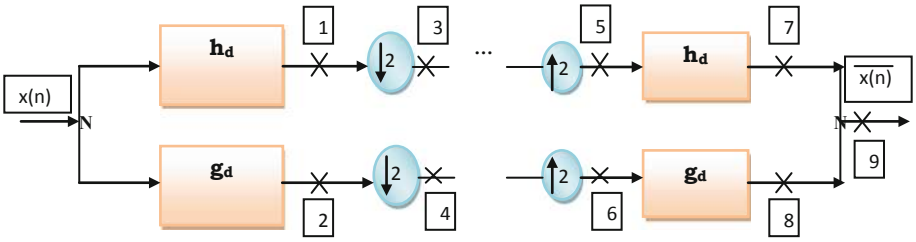

Fig. 1. A two band analysis cum synthesis filter bank system

Alias can be cancelled by choosing the filters such that the quantity in Eq. 6.9, $H_0(-Z)\ F_0(Z) + H_1(-Z)\ F_1(Z)$ is zero [9].

Thus the following choice cancels aliasing.

$$\begin{aligned} F_0(Z) &= H_1(-Z) \\ F_1(Z) &= -H_1(-Z) \end{aligned} \tag{2}$$

For the $H_0\widehat{(z)}$ and $H_1(z)$ it is possible to completely cancel the aliasing by the choice of synthesis filters [10].

In the matrix form expression1 can be written as –

$$z.\ \widehat{x(z)} = [x(z)\ .\ x(-z)\ ] \begin{bmatrix} H0(Z) & H1(Z) \\ H0(-Z) & H1(-Z) \end{bmatrix} \begin{bmatrix} F0(Z) \\ F1(Z) \end{bmatrix}$$

$$H(z) = \text{Alias component matrix}$$

The matrix H(Z) is called the aliasing component (A.C) matrix. The term which contains X(−Z) originates because of the decimation. On top of the unit circle, $X(-z) = X\left(e^{j(w-n\square)}\right)$ which is a right shifted version of $X(e^{jw})$ by an amount of $\prod$. This term takes into account aliasing due to the decimators and imaging due to the expanders [11]. It could be referred this just as the alias term or alias component.

3.3 Elimination of Aliasing Effect

When the input signal to the decimator is not band-limited, then the spectrum of decimated signal has aliasing. Hence, the input signal should be band-limited to π/D, where D is the decimator.

3.4 FIR Filters

For the multi-rate signal processing, FIR filters are chosen than IIR filters because

(1) FIR filters are stable
(2) FIR filters can be designed with exactly linear phase
(3) Limit cycles are not produced in the FIR filters since these filters are not having feedback [12].

FIR filters can be designed using three techniques i.e.,

(1) Fourier series technique
(2) Frequency sampling technique
(3) Window technique

Because, in this research Daubechies-4 window which is suitable for audio applications is used, the design of FIR filter using window technique is illustrated here.

3.4.1 FIR Filter Using Window Technique

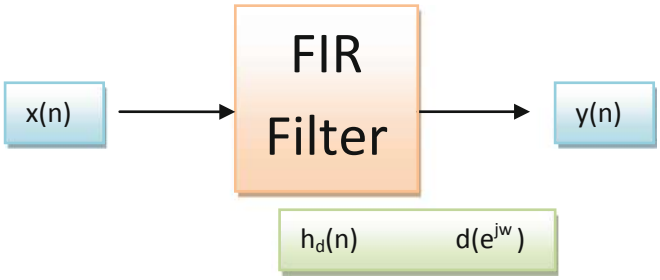

Fig. 2. FIR filter

The above Fig. 2 shows the FIR filter. In Fig. 2

$$\begin{aligned} h_d(n) &= \text{Fourier coefficients having infinite length} \\ &= 1/2\pi \int_{-\pi}^{\pi} H\left(e^{jw}\right) \cdot e^{jwn} dw \end{aligned} \tag{3}$$

$$\begin{aligned} H_d(n) &= \text{Fourier series representation of } h_d(n) \\ &= \sum_{n=-\infty}^{\infty} hd(n) \cdot e^{jw} \end{aligned} \tag{4}$$

3.4.2 Daubechies Wavelet Co-efficients

Because of the 3-stage Standard floating point audio CODEC is to be implemented by DWT using multi-rate analysis, the window size is not fixed which means that analysis is to be done for different frequency bands by the high pass and low pass filters with the different resolutions by the decimators. As the specifications are changed window to window, a superior exercise is required to find the resultant filter co-efficients. After a lot of exercise, Prof. Ingrid Daubechies, had invented the low pass and high pass filter co-efficients for various applications and released for the public domain. It is important to note that the objective of this research is not to introduce the wavelet concepts starting from the scratch, but to present the application of wavelet in the field of signal compression such as in audio applications. But, in general to find the order of the filter (N); the transition frequency (Δf), sampling rate (fs), pass band attenuation ($\square_p$), stop band attenuation ($\square_s$) are required. If the response of the low pass filter is considered with various specifications as given below,

f_s = sampling rate
Δf = transition frequency
$\square_p$ = pass band attenuation
$\square_s$ = stop band attenuation

The order of the filter (N) could be found with the empirical relation as given below:

$$\begin{aligned} &\Delta f_{min} = f_s/N \text{ or} \\ &\Delta f \approx f_s/N * [\text{Atten(db)} - 8]/14 \text{ or} \\ &N = f_s/\Delta f * [\text{Atten(db)} - 8]/14 \end{aligned} \tag{5}$$

There are different mother wavelets like db2, db4 and db6 etc., which are invented by Prof. Ingrid Daubechies and for each one, there is a specific application. Some of the basic wavelets are explained as given below.

db2 Wavelet

db2 wavelet is also called Haar wavelet. It has 2 vanishing movements.

db4 Wavelet

As the name itself, db4 is having the four vanishing movements. It is specified for the audio applications. The filter co-efficients are extracted from the Matlab command as given below:

?[L.H] = orthfilt(dbwavf('db4'))

$$L = -0.1294 \quad 0.2241 \quad 0.8365 \quad 0.4830$$
$$H = -0.4830 \quad 0.8365 \quad -0.2241 \quad -0.1294$$

db6 Wavelet

It has 6 vanishing movements. It is used for C.T scan to identify the tumors by EEG and ECG.

3.4.3 Stage Standard Floating Point DWT Implementation

This section illustrates the implementation of the Standard floating point DWT decomposer and the DWT re-constructor.

Standard DWT Decomposer and Re-constructor

Figures 3 and 4 show the 16 bit floating point Standard DWT decomposer and re-constructor respectively. Its operation is explained in the below sub-sections.

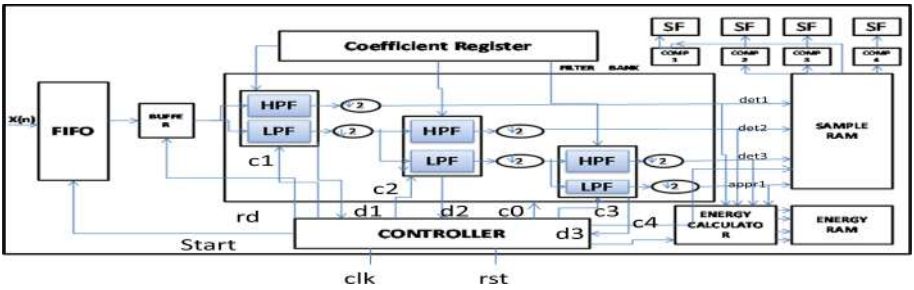

Fig. 3. 16-bit floating-point decomposer

The proposed 16-bit Standard floating-point DWT consists of various modules [5]. Each module can be explained in the below sub-sections.

FIFO

This module takes the signal sample and stores in the memory location. Once the FIFO module gets filled up the stored data is approved to the input buffer module. The FIFO module accepts the data when start signal goes high and passes data out to the input buffer module under read signal going high. The FIFO consists of 16 locations and passes out parallelly 16 samples of data at a time to the buffer module.

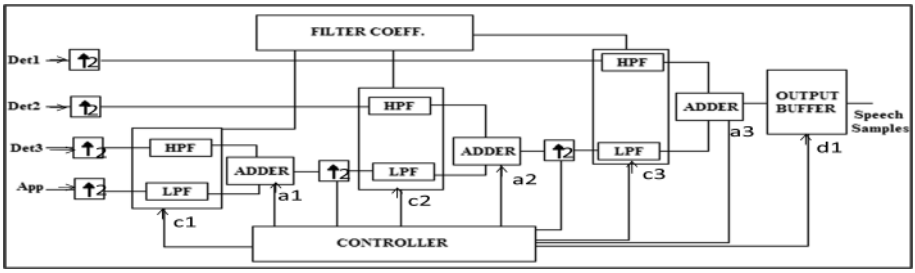

Fig. 4. 16 bit floating point re-constructor

Input Buffer

The module takes the data from the FIFO unit and packetizes the data and passes to the filter bank module. On every system clock the module passes out four samples each to the data transfer to attain synchronization between the data received and the filter bank operation.

Filter Bank

The Standard floating point DWT design consists of the core unit as the filter bank, which contains three banks of high-pass and low-pass filters. The filters decompose the input-signal samples into various sub bands depend upon the filter co-efficients sent to it.

Filter Stack

The filter stacks are the sub-modules of the filter bank where a pair of high-pass and low-pass filters are embedded into it. The high pass filter performs convolution operation between the input signal and the filter co-efficient passed from the co-efficient register. The convolution operation is carried out by the implementation of a floating point multiplier and a floating point adder module followed by shifting operation.

The high pass filter extracts the upper frequency components from the signal that get decimated by 2. The obtained samples are then passed down to SRAM unit where the samples get stored into the memory unit. The high pass unit gives the detail co-efficients and the low pass filter gives the approximate co-efficients which get further decomposed into its individual components. The low pass filter carries out the operation similar to high pass filter.

Controller

The controller is the control unit of the standard DWT design. It generates the control signals to different modules for its proper functionality. The controller reads the status of the filter stack as d1, d2 and d3 signal and generates appropriate control signals to the filter stack for its proper functioning. The controller gives the start signal to the FIFO unit when the system is reset and on the completion of FIFO filling generates a control signal to energy RAM and sample RAM to store the obtained samples and their energy.

Co-efficient Register
This unit holds the filter co-efficients for the filter unit and passes the co efficients to the filter bank for its operation.

Sample RAM
The detail and approximate co-efficients obtained from the filter bank are stored into the sample RAM unit. Sample RAM unit consists of 9 × 4 memory location to store the sub band samples. Each band is stored separately in sequence in the memory location.

Energy RAM
This module calculates the energy of each sample unit. The energy of a sample is calculated as square of the magnitude sample.

Comparator
The comparator module compares the obtained detail co-efficients and approximate co efficient elements in each sub band and finds the highest value in every sub band. The obtained value is the scale-factor for that sub band stored as Sfac1, Sfac2, Sfac3 and Sfac4.

Operation
The samples of the speech or audio whichever is to be processed that should be applied at the input of the FIFO of Fig. 3. As soon as controller sends the start signal to FIFO, it commences to accept the samples from the input. Because, FIFO length is 16 × 16, it stores the maximum of sixteen samples with the 16-bit length of each. Whenever FIFO is filled by the 16 samples it sends the first 4 samples to the buffer. From the buffer, the four samples are applied to the first section of the high pass filter and low pass filter of the filter bank. The low-pass and high-pass filters perform convolution operation between the input samples which come from the buffer and the high pass filter co-efficients from the co-efficient register. After convolution, HPF sends its output to the decimator. The decimator reduces the number of samples by 2 and then sends its output to the sample RAM. The components stored in this manner in sample RAM through the first section of the HPF are called detail1 components or det1. In the similar way, the convolution operation is carried out by the first section of the LPF between the samples come from the buffer and the low pass co-efficients from the co-efficients register. The output of the LPF is sent to the decimator for the decimation process. It reduces the number of samples to the half and sends its output to both HPF and LPF of the second section. After convolution, the outputs of the HPF which are called detail2 (det2) components, stored in the sample RAM and the outputs of the LPF are applied to the decimator. After decimation process, these will be applied to the third section of the HPF and LPF. The HPF performs the convolution operation and sends the detail3 (det3) components to sample RAM and the output of the LPF which are approximate components (appr1) are also sent to store in sample RAM at the end.

The comparator (comp) compares the respective detail and approximate components and sends the maximum component to the scale factor (SF) section. The reconstructor reads the detail components and approximate component from the scale factor section of the 16-bit floating point decomposer of Fig. 4. In the reconstructor side interpolators are used to obtain the samples which were dropped by the decimator during transmission. In the same way, adders are used to reconstruct the high pass and low pass filters' output. The reconstructor operation is exactly vice-versa to the decimator operation. At the output of reconstructor, the same signal of x(n) which was applied near the input of decomposer could be observed.

4 Results

This part presents the simulation and synthesis outcome of Standard floating point DWT.

Standard Floating-Point DWT

The simulation for the Standard-floating point DWT design is carried-out by the Modelsim 10.3cl. Since, the Modelsim has not the floating point packages, the customer defined floating point library packages are implemented and added with the standard library of the Modelsim tool. Now by porting the 16-bit floating point values using the testbench, the output would be obtained as shown in Fig. 5.

Simulation Results

Table 1 shows the simulation results of the Fig. 5 at particular instant of time t1 in binary. For easy understanding the same Table 1 was shown in Table 2 in decimal which states that the error is zero between the transmitted (input) and the received (output) values.

Table 1. Using floating-point binary values

Figure	At time	Input value (Binary)	Output value (Binary)	Error
5	t1	1000010000110110	1000010010110110	Zero

Table 2. Using floating point decimal values

Figure	At Time	Input value (Decimal)	Output value (Decimal)	Error
5	t1	$-7.6444 * 10^{-06}$	$-7.6444 * 10^{-06}$	Zero

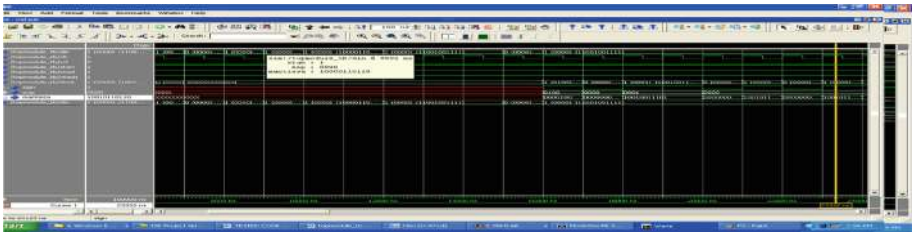

Fig. 5. The input and output values of the standard floating point DWT at particular instant of time say t1

Synthesis Results

The synthesis is developed by Xilinx Synthesis Technology (XST) tool. The chosen hardware device is Xc2s50e-ft256-6. The speed rating is −6. In this machine, the maximum number of IOs are 182 and the maximum number of BELs are 1728.

Figure 6a shows the top module of the Standard floating point DWT with pins from 0 to 15 among which 0 to 10 range is for the mantissa, 0 to 3 range is for exponent and 1-bit for sign. Figure 6b shows that internal RTL structure between FIFO and buffer. Figure 6c–d show the overall RTL diagrams of the Standard floating point DWT.

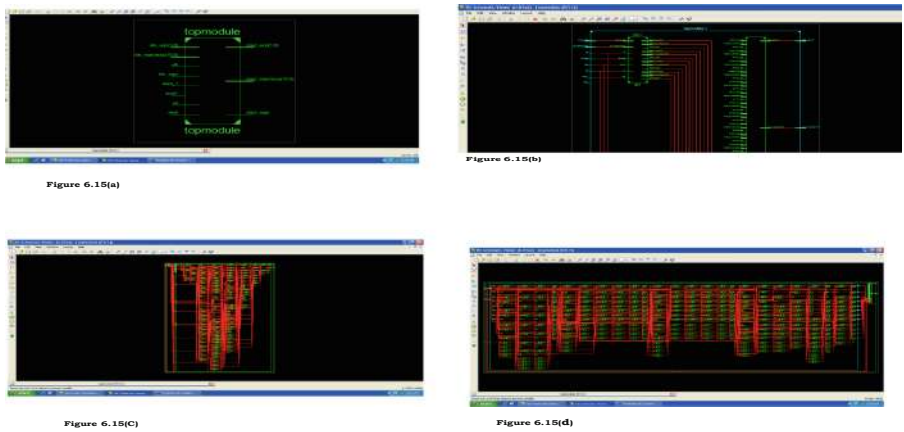

Fig. 6. RTL diagrams of standard-floating-point DWT

Synthesis Details

By the Table 3, it is known that the attained speed of the Standard floating-point DWT is 377.501 MHz through the power utilization and delay of 38.64 mw plus 2.649 ns respectively. The hardware resources that were taken by the Standard floating point DWT be 57% of IOs and 11.8% of BELs.

Table 3. Synthesis results for Standard floating-point DWT

Hardware parameters	Standard DWT
No. of IOs	105 out of 182 (57%)
No. of BELs	205 out of 1728 (11.8%)
Min. period	2.649 ns
Maximum speed	377.501 MHz
Power utilization	38.46 mW

5 Conclusion

The Standard floating-point DWT had been realized here is by the consumer defined floating-point – library-package with IEEE 754 standard. In the fixed-point DWT, the ADC and DAC need to be used physically but by develop the user defined floating-point package, a logical link had been given between source and DWT instead of physically connected data converters. To the Standard floating point DWT half precision is used; in which 1 bit is used for sign, 4-bits are used for the exponential and 11 bits are allotted for the mantissa.

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Abstract

In this paper, we present the design and simulation of co-axial fed microstrip antenna for C-Band (4–8 GHz) application with capacitive coupling technique. The antenna is designed from antenna theory (hand calculation) for centre frequency 5.6 GHz and later optimized for broadband using HFSS software. Dielectric substrate FR-4 proxy having dielectric constant 4.4 is used. The proposed antenna exhibits a much higher impedance bandwidth 53% (S11 < −10 dB).

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Energy-Efficient Waste Management System Using Internet of Things

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Abstract

Nowadays, waste management is a huge problem in the world. The key issue involved in waste management is waste collection within time, without overflowing the dustbins in public places. This paper presents an energy-efficient waste management system using IoT. This system measures the level of dustbin for every 30 min and sends the level to the cloud or database. Whenever the dustbin is full, it will send the location (longitude and latitude values) of dustbin to nearest garbage truck driver's application. An application is developed for showing dustbin level and to track the location of the dustbin for truck drivers. This system will operate for every 30 min to increase the battery life and remaining time system will be in sleep mode. Wi-Fi technology is used for sending the dustbin level to database.

Keywords

IoT Waste management Wi-Fi Location Database

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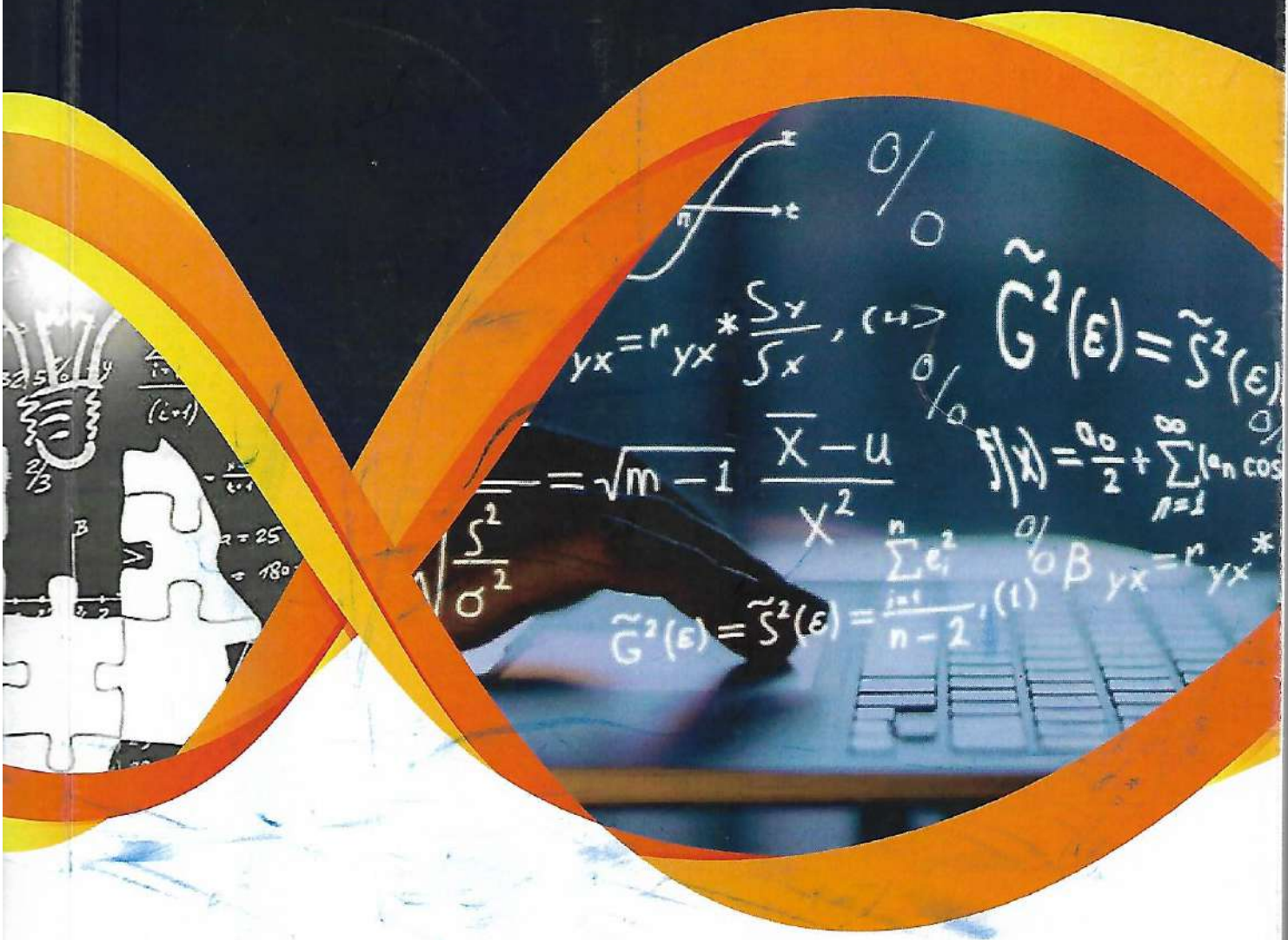

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PREFACE

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Dr. RAMESH MANNURU possesses the degrees of MSc (Maths), MSc (Statistics) from Osmania Science College, Hyderabad, TSSET and PhD in Mathematics (Operations Research). Passionate about teaching, he has an experience of 20 years in the field, teaching postgraduate and undergraduate level engineering students. He is an invitee to deliver GATE mathematics Lectures on specialized topics in premier institutions of India. He has been working as an Assistant Professor of Mathematics in Matrusri Engineering College, Saidabad, Hyderabad since 2011 and has published 6 research papers in reputed international journals. He has participated in more than 20 workshops, FDPs and presented papers in many national and international conferences and has been invited as a resource person in various engineering colleges.

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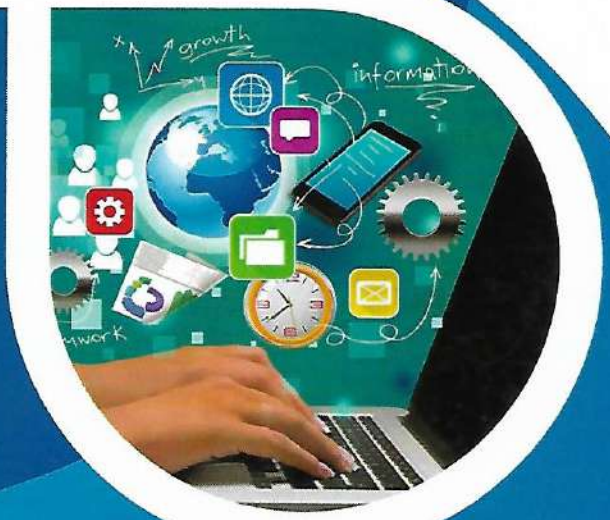

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In recent years, operations research (OR) is being used widely for decision making in management. As with most tools, however, OR is useless unless the user understands its application and purpose. The user has to ensure that the mathematical input accurately reflects the real-life problems to be solved and that the numerical results are correctly applied to solve them. With this in mind, this text emphasizes model-formulations, model-building skills and manual solution methods.

This book is intended for the use of beginners as well as advanced learners, as a text in operations research, management science, or mathematical programming.

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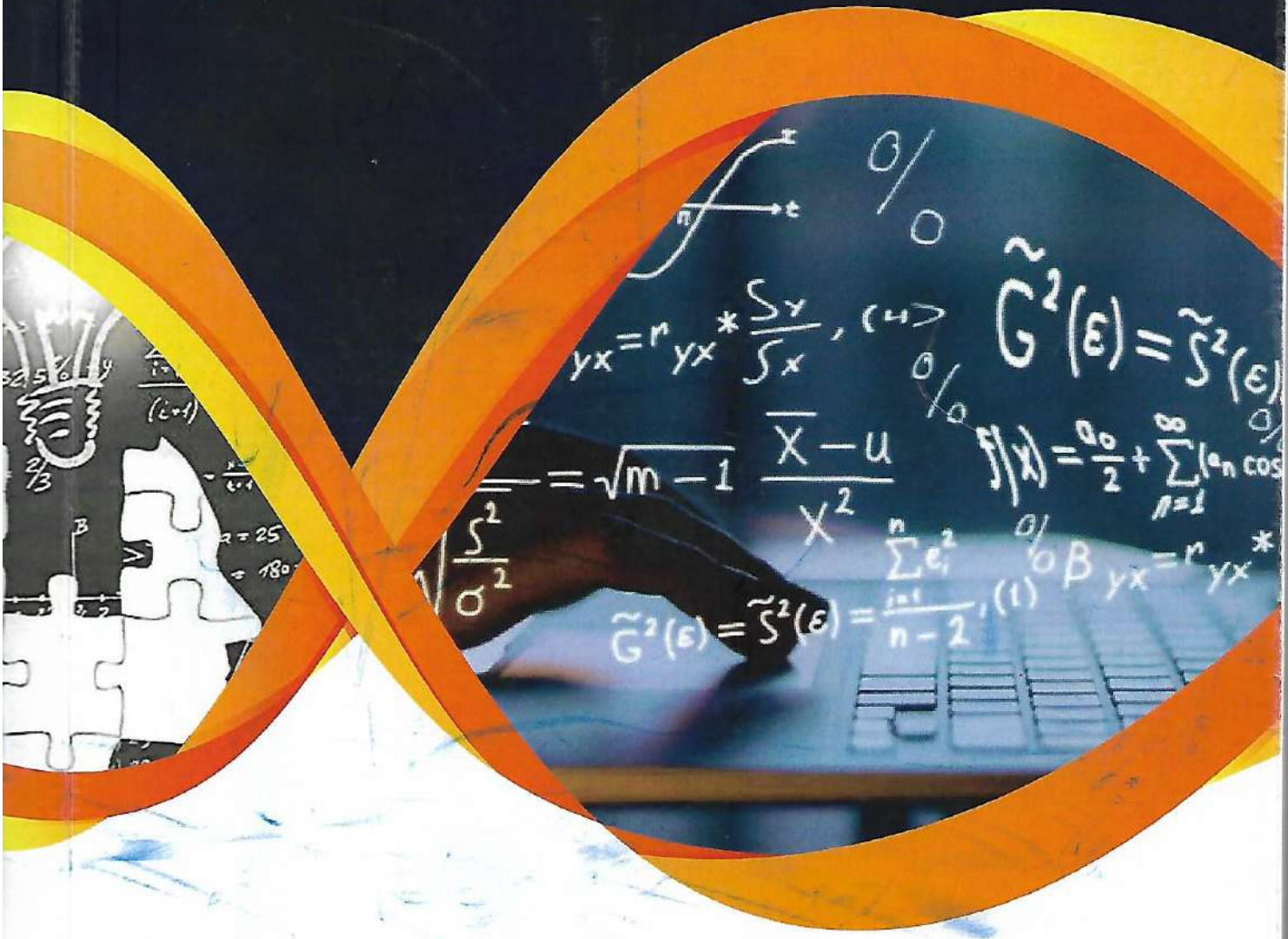

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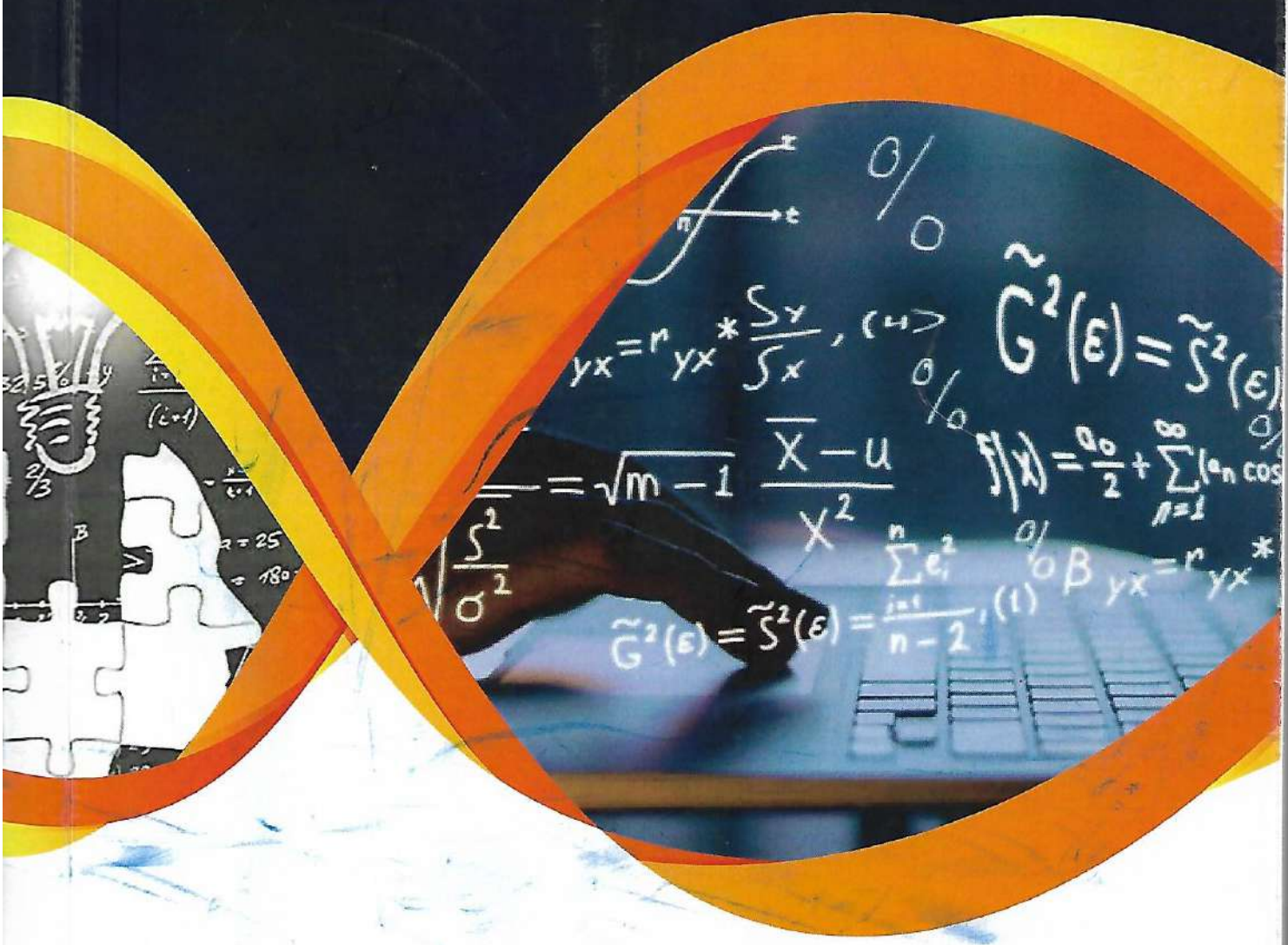

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PREFACE

We feel happy and honoured while presenting this book "ENGINEERING MATHEMATICS-III" for engineering students studying in B.Tech., III semester (CS and IT branch) of JNTU Hyderabad and all Indian Universities. In this book we have presented the subject matter in very simple and precise manner. The treatment of the subject is systematic and the exposition easily understandable. All the standard examples have been included and their model solutions have also been given.

Engineering Mathematics - III deals with the applications of applied Mathematics in the field of Engineering. This subject is generally taught in the III and IV semester of engineering. The basics of engineering mathematics as a branch of applied mathematics concerning mathematical models that are typically used in industry. This book on semesters III and IV will prepare students for their domain specific study and applications in their respective branches.

DR.RAMESH MANNURU
DR.YUVARAJU MACHA
MR.D.PURNA CHANDAR RAO

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* * * * *

Engineering Mathematics-III

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Dr. RAMESH MANNURU possesses the degrees of MSc (Maths), MSc (Statistics) from Osmania Science College, Hyderabad, TSSET and PhD in Mathematics (Operations Research). Passionate about teaching, he has an experience of 20 years in the field, teaching postgraduate and undergraduate level engineering students. He is an invitee to deliver GATE mathematics Lectures on specialized topics in premier institutions of India. He has been working as an Assistant Professor of Mathematics in Matrusri Engineering College, Saidabad, Hyderabad since 2011 and has published 6 research papers in reputed international journals. He has participated in more than 20 workshops, FDPs and presented papers in many national and international conferences and has been invited as a resource person in various engineering colleges.

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Dr. YUVARAJU MACHA has an M.Sc in Applied Mathematics, M.Tech in Computer Science and Engineering and a Ph.D in Mathematics (Operations Research). He was awarded by "Govern's Award - National award for Excellence in Teaching" in 2018 by GRA. Passionate about teaching, he has an experience of 14 years in the field, teaching postgraduate and undergraduate level engineering students and also has a year of real time experience in DRDL. He has been working as an Assistant Professor of Mathematics in Matrusri Engineering College, Saidabad, Hyderabad since 2012 and has published 10 research papers in reputed international journals. He has participated in more than 30 workshops, FDPs and presented papers in many national and international conferences and has been invited as a resource person in various engineering colleges. He has also been working as an Associate I/C of the Academic Branch of the college for the past 6 years. With a zeal to motivate and encourage the budding engineers, he is the NSS Program Officer of Matrusri Engineering College.

Mr. D.PURNA CHANDAR Rao is an Assistant Professor in the Department of Mathematics, Matrusri Engineering College, Saidabad, Hyderabad. He has an experience of 19 in teaching. His area of interest is Fluid Dynamics. He has a few publications to his credit in standard journals.

FUNDAMENTALS OF PROBABILITY AND STATISTICS FOR ENGINEERS

Dr. T. Yugandhar
Dr. Md. Shakeel
Dr. Yuvaraju Macha

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PREFACE

We feel great pleasure in bringing out the present book "FUNDAMENTALS OF PROBABILITY AND STATISTICS FOR ENGINEERS", which meets the requirements of the students. Probability has applications in every engineering as well as other disciplines. This book is designed, for graduate, post graduate, M.C.A. & Engineering courses of various Indian Universities. The matter presented in it is easy to understand. Each chapter begins with clear statements of definitions, principles and theorems with proofs and other descriptive and objective material .Each chapter contains large number of solved examples, hence it can easily be used for self study. Model questions from past university examinations have been included in examples.

We wish to thank BH International Publications, for their keen interest and Co-operation in bringing out this book.

We shall be grateful for any suggestions for improvement of the book.

DR.T.YUGANDHAR
DR.MD.SHAKEEL
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* * * * *

Fundamentals Of Probability And Statistics For Engineers

DR.T.YUGANDHAR
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DR. T. YUGANDHAR has to his credentials a dual masters degree in Statistics & Mathematics coupled with Ph.D in Mathematics (Operations Research). He has to credit an impeccable experience of 23 years in the teaching - learning process, teaching post graduate and undergraduate level students earmarking his passion for aforesaid. He has been working as an Associate Professor of Mathematics in Gurunanak Institutions Technical Campus, Ibrahimpatnam, R.R.Dist., since 2014. He is research savvy, an embodiment of his multifaceted repertoire in the realms of afore mentioned discourse with 11 research papers in reputed national & international journals. He has participated in more than 20 workshops, FDPs and presented papers in many national and international conferences. He played a pivotal role as a subject expert in P&S, Engg.Mathematics & O.R.

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DR. MD. SHAKEEL obtained Ph.D. degree in Mathematics from JNTUH, Kukatpally,Hyderabad. He did his M.Sc., B.Ed. from Osmania University and M.Phil. from MKU.He has more than 17 years of teaching experience (this includes 14 years teaching experience in Engineering discipline).Heis presently serving as an Associate Professor and the Head of Department of Mathematics in Sri Chaitanya Degree & PG College, MahabubnagarDist., Telangana. He is a visionary leader who enjoys creating a learning environment which motivates and inspires all the aspiring students to excel.As a committed teacher, he has a passion for teaching and a flair for writing.He has authored 7 research papers in various reputed International journals. He presented 5 research papers in International conferences. He participated in several national and international seminars and workshops.He also severed as the HOD of H&BS, NSS Programme officer, academic committee member, apart from primary duties.

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PREFACE

This "MATHEMATICAL FOUNDATIONS OF COMPUTER SCIENCE" text book explains how to use mathematical models and methods to analyze problems that arise in computer science. Proofs play a central role in this work because the authors share a belief with most mathematicians that proofs are essential for genuine understanding. Proofs also play a growing role in computer science; they are used to certify that software and hardware will always behave correctly, something that no amount of testing can do.

This Text Book is designed to meet the requirements of the under graduate students of B.Sc (Computer Science), B.C.A., B.Sc (CT) and post graduate students of M.C.A., M.Sc (Computer Science) and Computer Technologies. This text is for beginners as well as experts who wish to learn this subject. The language adopted is simple and the subject-matter self explanatory in nature. A variety of problems has been included in each chapter to enable the reader to gain further insight and clarity of the application of the techniques. It includes numerous examples that illustrate the basic concept and the exercises, to enhance the value of the book. Key Features This Text Book covers Matrices, Set Theory, Boolean Algebra, Mathematical Logic, Graph Theory, Grammars And Languages. Numerous illustrative problems are provided to help the reader understand the subject. To suit the needs of the B.C.A., M.C.A. and M.Sc curriculum of various universities. All major steps in the problems are presented in a step-by-step format.

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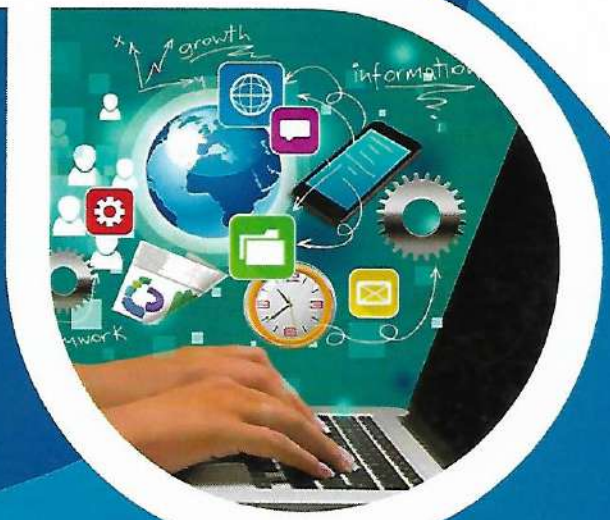

Operations Research

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PREFACE

In recent years, operations research (OR) is being used widely for decision making in management. As with most tools, however, OR is useless unless the user understands its application and purpose. The user has to ensure that the mathematical input accurately reflects the real-life problems to be solved and that the numerical results are correctly applied to solve them. With this in mind, this text emphasizes model-formulations, model-building skills and manual solution methods.

This book is intended for the use of beginners as well as advanced learners, as a text in operations research, management science, or mathematical programming.

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Conference paper
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Part of the Lecture Notes in Electrical Engineering book series (LNEE, volume 642)

Abstract

In this paper, we present the design and simulation of co-axial fed microstrip antenna for C-Band (4–8 GHz) application with capacitive coupling technique. The antenna is designed from antenna theory (hand calculation) for centre frequency 5.6 GHz and later optimized for broadband using HFSS software. Dielectric substrate FR-4 proxy having dielectric constant 4.4 is used. The proposed antenna exhibits a much higher impedance bandwidth 53% (S11 < −10 dB).

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Part of the Lecture Notes in Electrical Engineering book series (LNEE, volume 642)

Abstract

Nowadays, waste management is a huge problem in the world. The key issue involved in waste management is waste collection within time, without overflowing the dustbins in public places. This paper presents an energy-efficient waste management system using IoT. This system measures the level of dustbin for every 30 min and sends the level to the cloud or database. Whenever the dustbin is full, it will send the location (longitude and latitude values) of dustbin to nearest garbage truck driver's application. An application is developed for showing dustbin level and to track the location of the dustbin for truck drivers. This system will operate for every 30 min to increase the battery life and remaining time system will be in sleep mode. Wi-Fi technology is used for sending the dustbin level to database.

Keywords

IoT Waste management Wi-Fi Location Database

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12

Cloud Computing For IOT

Dr. Ashok Kumar K, Mr. V. Karunakar Reddy

Abstract

Internet of Things (IoT) is one of fastest technologies in the internet revolution. The IoT technology allows millions of devices integrated and also communicates among them for sharing the data. A fundamental problem of organization is storing of data therefore it is bounded within the walls of data centers. It is not suitable who are working from home with their own laptops and desktops and also not possible to establish data centers for remote access. Hence, cloud computing is solution for mentioned problems and also it provides the same performance like data centers. The IoT and cloud computing are two different technologies and the combination of these technologies are building robust solutions for IoT on cloud platform. This chapter is highlighted mainly overview of IoT, challenges and benefits of IoT with cloud computing. This chapter also discusses the architecture and implementing issues of cloud based IoT therefore directing new ways of research on IoT.

Keywords: *Internet of Things, Cloud Computing, Cloud IoT, Fog Computing, Integration.*

Introduction

Internet of Things (IoT) is defined as integrated of things or devices in a network which is embedded various sensors, actuators, software

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and network connectivity to exchange and share the data among them. The things which are sensors and actuators communicate each other to obtain a common goal. The motivation behind IoT is to get knowledge, measure and modify the environmental conditions around people. This plays a major role in the future to obtain the remarkable achievements like e-health, smart agriculture and industry automation etc. IoT provides huge information like Big data which has three characteristics that are volume (data size), velocity (data frequency) and variety (data type). The things in IoT have small storage capability and also computing capacity therefore raising issues in terms of performance, reliability and privacy. Scalability is also one of major drawbacks for IoT because of improper infrastructure [1]. Cloud computing is the technology that provides unlimited capabilities in terms of storage and computing virtually. This is providing services in terms of resource sharing for computing over Internet. The origin of cloud computing was started from the cluster computing and then moved to grid computing there after utility computing. The cloud computing has mainly five characteristics that are Metered service, on-demand self service, broad network access, rapid elasticity and resource pooling. The cloud computing has three main service models that are software-as-a-Service (SaaS), Platform-as-a-Service (PaaS) and Infrastructure-as-a-service (IaaS). Cloud computing has several models of providing services that are private cloud, public cloud, community cloud, hybrid cloud. It also has several issues when connecting to internet thereby requiring an efficient technology to obtain high performance in terms of storage and speed of sharing the data [2]. The characteristics of IoT and Cloud computing is presented in Table.1. A Cloud-IoT is the integrated technology to prevent issues of both IoT and Cloud. Cloud computing extends the real time performance of IoT into distributed and dynamic manner. It enables that the things of IoT are connecting to the cloud and also other devices to share the data securely. Google cloud platform, IoT based Amazon web services, IoT based Microsoft azure and IoT based IBM Watson are leading products in the market with technique Cloud-IoT. Most of the previous works are concentrated on IoT and Cloud computing separately. Recently, a lot of papers are proposing different techniques on cloud-IoT method.

Table 1: Characteristic of IoT and Cloud

IoT	Cloud Computing
It has real time things	It has virtual resources
It has limited storage and computational capabilities	It has virtually unlimited storage and computational capabilities
It has pervasive manner	It has ubiquitous manner
It uses big data source	It has used to manage big data
It uses internet as a point of convergence	It uses internet as service of delivery

The remaining of this chapter as follows: section-2 describes the background work of IoT and cloud computing. Section-3 presents advanced architecture of cloud-IoT and the section-4 propounds applications of integrated architecture. Finally, section-5 concludes the chapter.

Basic Concepts & Background

Internet of Things, the term is first coined by Kevin Ashton with knowledge of "Embedded internet" and "Pervasive computing" in 1999. Thereafter, International Telecommunication Union (ITU) presented formally in 2005. IoT refers that the devices are interconnected in a world-wide network with a unique address and a standard protocol [3]. The advancement of IoT is depended on recent advancements of devices and communicated technologies. The things of IoT not only complex like cellular mobile but also comprise daily life like clothes, food, furniture and so on. By considering many parameters, US National Intelligence Council reported in 2008 that one of the six technologies interests potentially impact on US by 2025 and it is also expected that IoT will cross 24 millions of interconnected devices by 2020 [4]. By observing that the IoT is one of main sources for Big data. Fig.1 presents IoT and its associated technologies. IoT is mainly linked technologies like Big data, Cloud to achieve sophisticated applications virtual to real. Because of integrated network, each component is necessary to the interaction and communication with other IoT [5].

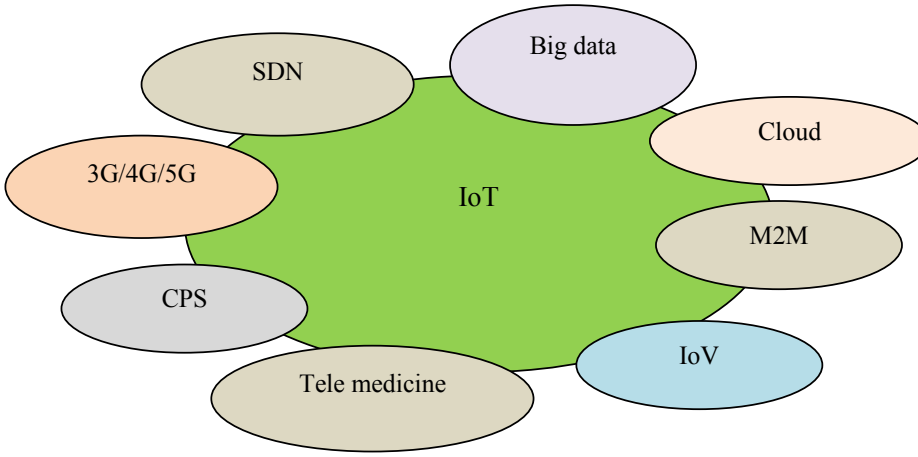

Fig. 1: IoT and its associated technologies

Challenges of IoT

The several challenges rise in IoT when handling high data and sharing huge number of devices [6]. The major issues of IoT are like security, privacy, scalability, interfacing, bandwidth management, energy management, data storage and so on.

1. **Security:** As huge number of devices are interconnected and always must be online to share the information among them. Both the device and its communication media must be secure otherwise entire devices in system are at risk. Smart health system is one of the examples that the IoT need to be secure otherwise patient is in risk.
2. **Privacy:** IoT is the bank of information whose access it immediately. Smart phone is one of the examples of required privacy. Things that are called Smart devices are need to privacy because of sharing information to entire devices in system.
3. **Scalability:** The scaling of things in IoT is another important challenge that affects the performance of the system. The scalability is inversely proposing the performance of IoT that the performance is slows down when number of devices are increases.

4. **Data storage:** The storing of information in IoT is increasing the requirement of energy demands. The major company like Google is using a myriad server farm which occupies large area such as thousands of square feet. This is crucial overhead for data storage of smart devices. The requirement of data storage is proportional to the applications of IoT. To prevent this overhead, the policies must be generated for data which is to be stored and which device can access it and also mention how long it is stored.
5. **Energy Management:** The energy dissipation is increasing with increase in things of IoT. According to estimations in the year of 2012, the data centers need to be required 30 billions of Watts in a year. This is increasing by number of applications in IoT. Though, solar and wind renewable sources are used, it is difficult to reduce energy demands. Hence, energy management of IoT is important research domain in future.
6. **Interfacing:** The interfacing media of IoT is also one of the important parameters that affect the performance of system. Bluetooth, 6LowPAN and Wi-Fi are the example of interfacing media of IoT. The interfacing is complex when number of things is present in the system.

Architecture of IoT

The basic architecture of IoT is shown in fig.2 which consists of four layer structure and it's interconnected each other. The architecture of IoT is mainly constructed with different architecture styles, smart objects, communication and networking, services, applications, cooperative data processing, business models, security and so on [7]. Based perspective of technology, IoT architecture needs to be considered main characteristics among heterogeneous devices such as scalability, extensibility, interoperability, modularity. According environment of things, the architecture needs to interact devices dynamically. Hence, IoT is providing the capability of event-driven efficiently because of heterogeneous and decentralized nature. The importance of each layer in four layered architecture is given table. 2.

Table 2: Importance of each layer

Sensing Layer	The layer is combined with existed real-time hardware (Sensors, RFID) to sense/control real-time world for acquiring information
Networking Layer	This layer supports the basic networking and data sharing devices wired/wirelessly
Service Layer	This layer owns and manages services satisfactorily
Interface Layer	This layer interacts with information to users and other applications

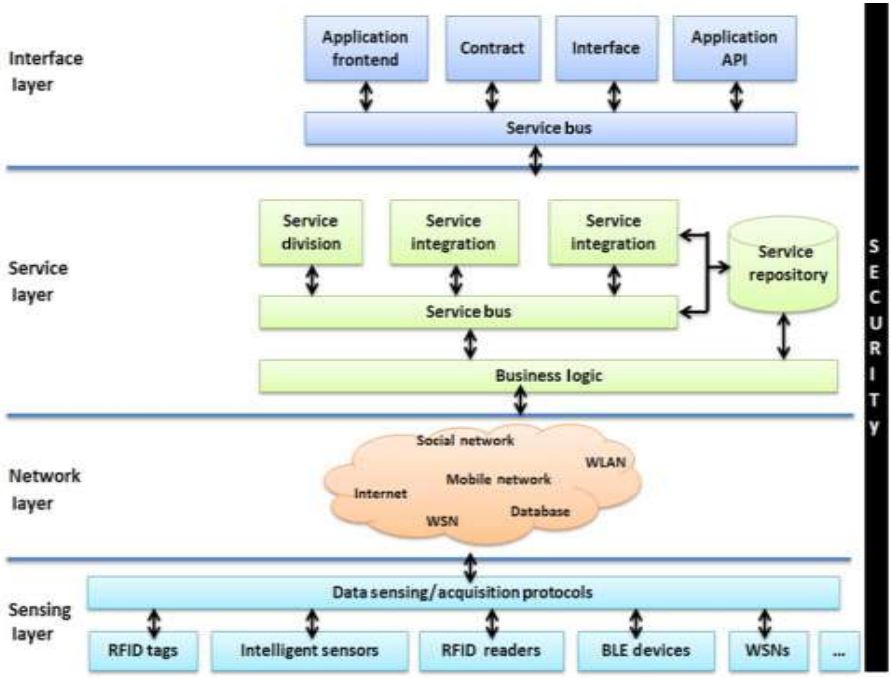

Fig. 2: Structure of IoT

Cloud Computing

There are several definitions are proposed for cloud computing which are accepted by the National Institute of Standard and Technology (NIST). The cloud computing has four different types of models, five basic characteristics and three types services. The deployment models of

cloud computing are classified as public, private, hybrid and community cloud which depends on how the resources are available to consumers through Internet. The public cloud is typically owned by the profitable organization such as Amazon web service where as private cloud is allocated to the single company to give services of particular sector of consumers (Microsoft private cloud). The private cloud provides information higher security and higher level of control. A hybrid cloud is the mixture of both public and private clouds that integrates the required characteristics of both clouds.

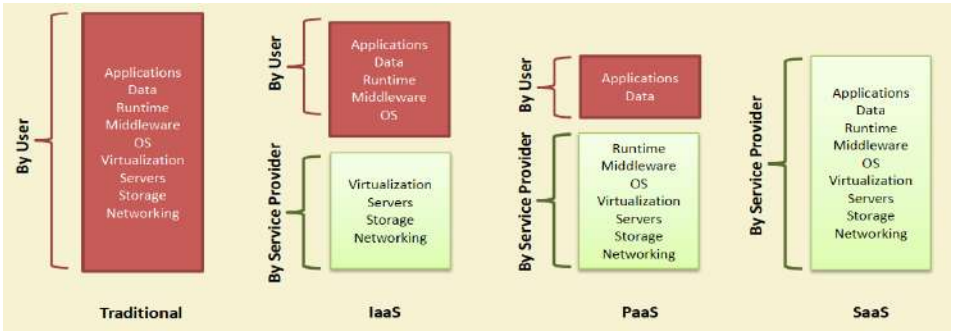

Fig. 3: Comparison of different cloud service models

A community cloud is the cloud which sends same information to group of consumers and also number of companies. Distributed cloud is the cloud which shares the information for collection of scattered set of computing devices in various locations. Public resource computing and volunteer cloud are the two types of distributed cloud. To increase flexibility and fault-tolerance, a multi-cloud which is multiple computing services are presented through single heterogeneous structure. To support interoperability, a inter cloud indicates that clouds of cloud through Internet globally. To enhance the flexibility of consumer, the cloud computing provides three different levels of services namely, SaaS, PaaS and IaaS. Fig. 3 depicts the comparison of services of traditional and cloud models. The SaaS is the service that the software is transferred over internet, example is Google apps. The PaaS provides higher level of service that offers integrated environment to build and test of certain software, example is Microsoft Azure. The IaaS is offering service in terms of infrastructure that is hardware, storage and servers, example is Amazon web services.

Need of Cloud Computing in IoT

Both cloud computing and IoT are developing rapidly with their unique characteristics and services to consumers. The IoT is characterized of large distributed things with low storage and processing capabilities. The things raise the issues in terms of performance in terms of reliability, scalability, security and privacy. The cloud computing featured more devices of a network with unlimited storage. It offers robust and flexible environment that integrates dynamic information from different information sources in the same network. With integration of cloud to IoT, the performance issues of both cloud and IoT are solved partially. Once cloud is integrated to IoT, information is sharing in uniform manner with a standard communication API thereby providing security, accessing information directly from anywhere. Another advent of this integration is IoT resources are deal with unprecedented infrastructure because cloud allows infinite storage with appropriate content. Prediction and data-driven decision making algorithms are presented with low cost, increased revenues and also reduced high risks. An essential requirement of IoT is to provide unique IP access for devices to share information over the dedicated hardware and also the communication among the devices is expensive. The cloud computing presents an affordable and effective solution like processing and tracking any device from anywhere to utilize the customized applications. Hence, the combined cloud-IoT technology solves complex problems thereby providing additional benefits such as ease of use, ease of access. Hence, it is indeed to the next generation in internetworking environment [8].

Challenges of Integrated Design

Though the combined cloud-IoT architecture solves complex problems, it also exhibits huge number of problems. Each application of integrated is showing different challenge thereby huge attention of research community. This integration imposes various challenges in the performance such as heterogeneity, scalability, reliability and big data.

1. **Heterogeneity:** One of the major challenges of integrated design is wide range of heterogeneous system such as devices, platforms, operating system and services used in different

advanced applications. The services of cloud computing are existed with proper interface, customized according to dedicated provider and causing resource integration. The heterogeneity of cloud computing is also non-negligible thereby exacerbating the issues when multi-cloud is utilized. These issues are solved partially with cloud breaking by third parties or cloud providers. If the services are depend on multiple providers, the performance and resilience of application are improved. Because things of IoT are tightly coupled with dedicated application, the service providers are required to conduct survey on the specified hardware and software, computing infrastructure and integrating heterogeneous system.

2. **Scalability:** The combined cloud-IoT design aims to develop massive system with large applications thereby requiring real-time devices to analyze the information. The large scale of devices results number of challenges to become system complex. With number of devices in the system, the scalability critical problem at each level including data sharing, data processing and service of networking. In addition to this, the distribution property of IoT creates tasks hard because the issues of connectivity and latency.
3. **Reliability:** Reliability is one of the major concerns for combined cloud-IoT design because of smart applications. There is a huge scope of occurring errors in integrated design such as intermittent to make the system unreliable. Applications like smart mobility, vehicular ad-hoc network becomes often unreliable because of its mobility in the cluster. In such applications, the resources are deployed in the constrained environment thereby occurring number of challenges such as device failure or device unreachable. The integrated system also exhibits uncertainties related to the resource exhaustion and data center visualization.
4. **Big data:** IoT is one of major sources of big data whereas cloud enables storing it for longer periods and process. Handling of this huge data is complex challenge since the performance of integrated design depends on the data management. On other hand, there is no perfect algorithm for the cloud to the data management. In addition to this, data integrity is one of main concerns because it affects the security and quality of service.

Security and Privacy

The combined cloud-IoT design allows transfer of data from cloud to real-world. The appropriate authorization rules are needed to be framed to access the information from the cloud. This is essential when privacy of users is major concern and also particularly data integrity is needed to be guaranteed. Several issues are arise when complex applications are merged with cloud because lack of information of service provider [9]. The public key of cryptography is not allocated entire layers since constraints of power deployed by IoT. New challenges can able to occur because of vulnerabilities such as hijacking.

Integrated Cloud-IoT Architecture

Based on literature, the IoT architecture consists of three layers that are network, perception and application layer. Fig.4 depicts the structure of integrated design. The sensing layer is used to sense data which is received from near things or surrounding environment [10]. A variety of sensor devices are used to acquire information from different sources such as RFID tags, cameras. A network layer transfers the data from the cloud or internet. Different number of protocols is existed in network layer to transfer data from perception layer to application layer. The primary service of application layer is interfacing of end-user.

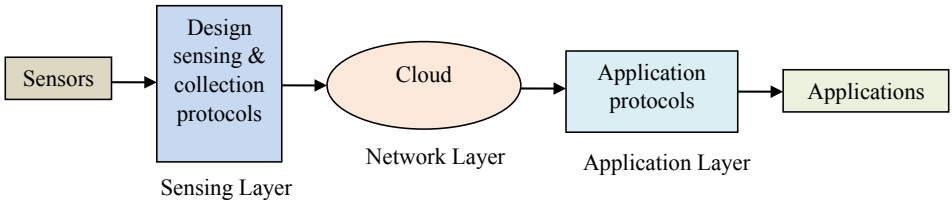

Fig. 4: Structure of integrated cloud-IoT

Applications of Integrated Design

The approach of cloud based IoT introduces large number of applications in terms of services of end-user. The integration of two different technologies shows variety of characteristics to obtain wide set of applications. Fig.5 shows some of major applications which builds on the integrated design.

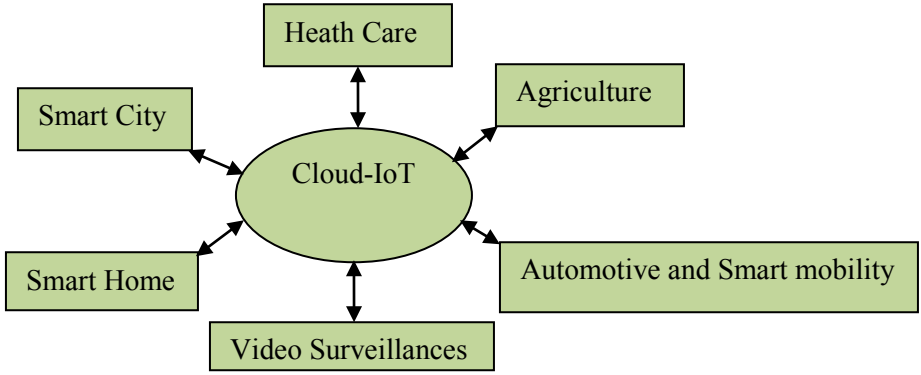

Fig. 5: Applications of integrated cloud-IoT design

Healthcare

Now-a-days, most of the hospitals are maintain the patient record with sensor networks and also monitoring the doctor to track of drug administration. The integrated cloud-IoT design significantly improves the healthcare services and it also advances the quality in medical domain by collaborating the different companies involved. The cloud-IoT design presents innovative applications such as collection of patient data through sensors nodes, transferring data to cloud of medical centers to share and process in Electronic Healthcare Record (EHR). An Ambient Assistant Living (AAL) is one of important applications to live ease for disabled people.

Agriculture

IoT empowers the developments of efficient crops in agriculture in terms of low production cost. The IoT achieves new agriculture infrastructure in various directions such as machinery agriculture, agriculture products and also data base systems. The important benefits of integrated design in agriculture are identifying need of food, tracing food with RFID, Monitoring plants and its surroundings. Monitoring of changes in the soil thereby inputting water, fertilizers, pesticides to the soil. These result to advance in the production of food products and efficient crops to the real world with an effective price.

Automotive and Smart Mobility

IoT is providing an effective solution of massive problems in automobile and transportation services. The integrated cloud-IoT design brings the benefits in terms of managing and reducing road traffic and also enhancing the road safety. The main purpose of cloud-IoT platform presets low cost, on-demand, secure and real-time services to the end-user. To extend the conventional cloud services, vehicular clouds are implemented to enhance the storage capabilities and on-demand computing.

Video Surveillances

The video surveillance is one of most important services for security related domain because it monitors continuous and manages the system by it-self. The integrated design provides the promising solution for complex problems such as video storage. It also proposes the effective solution in term of identifying and managing storage capabilities of video from the camera, load balancing and efficiency of data delivery and fault tolerance. The integrated design is supreme tool for video surveillance.

Smart Home

To empower the automation services in home appliances, the integrated cloud-IoT design is utilized. The cloud provides the best services in terms of huge data with less complexity. The smart home based cloud presents dedicated services in terms of home appliances. An Intelligent Remote control is one of examples of the integrated cloud-IoT design which controls and manages intelligently from anywhere. Several smart home appliances are proposed based huge literature.

Smart City

A middleware for future contained smart cities shall be presented through the IoT which attains the information from sensing devices such as RFID tags or geo tags and providing data consistently. Based on the recent literature, the integrated cloud-IoT design empowered in

terms of connection and integration for sensors and actuators thereby easing to applications to physical world of smart cities. The combined cloud-IoT improves the services and communication to the nearby environment such as Bigbelly, Smart streetlights [11].

Future Directions

The research on integrated cloud-IoT is still live because of lot of open issues and new applications. IoT6, a research project from Europe is dealing IP-V6 and other standards such as COAP, CORE to advance integrated cloud-IoT design. An APT is also standard protocol is used in combined cloud-IoT design to interconnect between advancement of services and smart objects. The complex data mining is one of another important directions integrated design because of complexity of Big data is not solved. Fog computing is new model which extends the services of the cloud computing. There is a huge scope of research in fog computing in particular domains such as smart-grid.

Conclusion

This chapter presented the structure of cloud-IoT design and its importance in various applications. This chapter neatly presented with challenges of IoT and cloud thereby identified the difference between two technologies and also highlighting the importance of the integrated cloud-IoT design. From recent literature, structure and applications of the integrated cloud-IoT is presented. Finally, the future directions of this advanced design are discussed with some open issues in particular applications.

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Internet of Things (IoT) is defined as integrated of things or devices in a network which is embedded various sensors, actuators, software

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and network connectivity to exchange and share the data among them. The things which are sensors and actuators communicate each other to obtain a common goal. The motivation behind IoT is to get knowledge, measure and modify the environmental conditions around people. This plays a major role in the future to obtain the remarkable achievements like e-health, smart agriculture and industry automation etc. IoT provides huge information like Big data which has three characteristics that are volume (data size), velocity (data frequency) and variety (data type). The things in IoT have small storage capability and also computing capacity therefore raising issues in terms of performance, reliability and privacy. Scalability is also one of major drawbacks for IoT because of improper infrastructure [1]. Cloud computing is the technology that provides unlimited capabilities in terms of storage and computing virtually. This is providing services in terms of resource sharing for computing over Internet. The origin of cloud computing was started from the cluster computing and then moved to grid computing there after utility computing. The cloud computing has mainly five characteristics that are Metered service, on-demand self service, broad network access, rapid elasticity and resource pooling. The cloud computing has three main service models that are software-as-a-Service (SaaS), Platform-as-a-Service (PaaS) and Infrastructure-as-a-service (IaaS). Cloud computing has several models of providing services that are private cloud, public cloud, community cloud, hybrid cloud. It also has several issues when connecting to internet thereby requiring an efficient technology to obtain high performance in terms of storage and speed of sharing the data [2]. The characteristics of IoT and Cloud computing is presented in Table.1. A Cloud-IoT is the integrated technology to prevent issues of both IoT and Cloud. Cloud computing extends the real time performance of IoT into distributed and dynamic manner. It enables that the things of IoT are connecting to the cloud and also other devices to share the data securely. Google cloud platform, IoT based Amazon web services, IoT based Microsoft azure and IoT based IBM Watson are leading products in the market with technique Cloud-IoT. Most of the previous works are concentrated on IoT and Cloud computing separately. Recently, a lot of papers are proposing different techniques on cloud-IoT method.

Table 1: Characteristic of IoT and Cloud

IoT	Cloud Computing
It has real time things	It has virtual resources
It has limited storage and computational capabilities	It has virtually unlimited storage and computational capabilities
It has pervasive manner	It has ubiquitous manner
It uses big data source	It has used to manage big data
It uses internet as a point of convergence	It uses internet as service of delivery

The remaining of this chapter as follows: section-2 describes the background work of IoT and cloud computing. Section-3 presents advanced architecture of cloud-IoT and the section-4 propounds applications of integrated architecture. Finally, section-5 concludes the chapter.

Basic Concepts & Background

Internet of Things, the term is first coined by Kevin Ashton with knowledge of "Embedded internet" and "Pervasive computing" in 1999. Thereafter, International Telecommunication Union (ITU) presented formally in 2005. IoT refers that the devices are interconnected in a world-wide network with a unique address and a standard protocol [3]. The advancement of IoT is depended on recent advancements of devices and communicated technologies. The things of IoT not only complex like cellular mobile but also comprise daily life like clothes, food, furniture and so on. By considering many parameters, US National Intelligence Council reported in 2008 that one of the six technologies interests potentially impact on US by 2025 and it is also expected that IoT will cross 24 millions of interconnected devices by 2020 [4]. By observing that the IoT is one of main sources for Big data. Fig.1 presents IoT and its associated technologies. IoT is mainly linked technologies like Big data, Cloud to achieve sophisticated applications virtual to real. Because of integrated network, each component is necessary to the interaction and communication with other IoT [5].

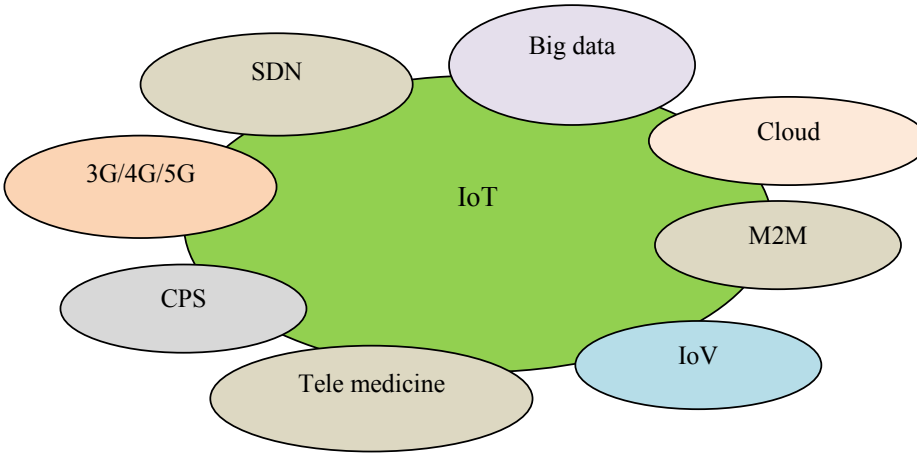

Fig. 1: IoT and its associated technologies

Challenges of IoT

The several challenges rise in IoT when handling high data and sharing huge number of devices [6]. The major issues of IoT are like security, privacy, scalability, interfacing, bandwidth management, energy management, data storage and so on.

1. **Security:** As huge number of devices are interconnected and always must be online to share the information among them. Both the device and its communication media must be secure otherwise entire devices in system are at risk. Smart health system is one of the examples that the IoT need to be secure otherwise patient is in risk.
2. **Privacy:** IoT is the bank of information whose access it immediately. Smart phone is one of the examples of required privacy. Things that are called Smart devices are need to privacy because of sharing information to entire devices in system.
3. **Scalability:** The scaling of things in IoT is another important challenge that affects the performance of the system. The scalability is inversely proposing the performance of IoT that the performance is slows down when number of devices are increases.

4. **Data storage:** The storing of information in IoT is increasing the requirement of energy demands. The major company like Google is using a myriad server farm which occupies large area such as thousands of square feet. This is crucial overhead for data storage of smart devices. The requirement of data storage is proportional to the applications of IoT. To prevent this overhead, the policies must be generated for data which is to be stored and which device can access it and also mention how long it is stored.
5. **Energy Management:** The energy dissipation is increasing with increase in things of IoT. According to estimations in the year of 2012, the data centers need to be required 30 billions of Watts in a year. This is increasing by number of applications in IoT. Though, solar and wind renewable sources are used, it is difficult to reduce energy demands. Hence, energy management of IoT is important research domain in future.
6. **Interfacing:** The interfacing media of IoT is also one of the important parameters that affect the performance of system. Bluetooth, 6LowPAN and Wi-Fi are the example of interfacing media of IoT. The interfacing is complex when number of things is present in the system.

Architecture of IoT

The basic architecture of IoT is shown in fig.2 which consists of four layer structure and it's interconnected each other. The architecture of IoT is mainly constructed with different architecture styles, smart objects, communication and networking, services, applications, cooperative data processing, business models, security and so on [7]. Based perspective of technology, IoT architecture needs to be considered main characteristics among heterogeneous devices such as scalability, extensibility, interoperability, modularity. According environment of things, the architecture needs to interact devices dynamically. Hence, IoT is providing the capability of event-driven efficiently because of heterogeneous and decentralized nature. The importance of each layer in four layered architecture is given table. 2.

Table 2: Importance of each layer

Sensing Layer	The layer is combined with existed real-time hardware (Sensors, RFID) to sense/control real-time world for acquiring information
Networking Layer	This layer supports the basic networking and data sharing devices wired/wirelessly
Service Layer	This layer owns and manages services satisfactorily
Interface Layer	This layer interacts with information to users and other applications

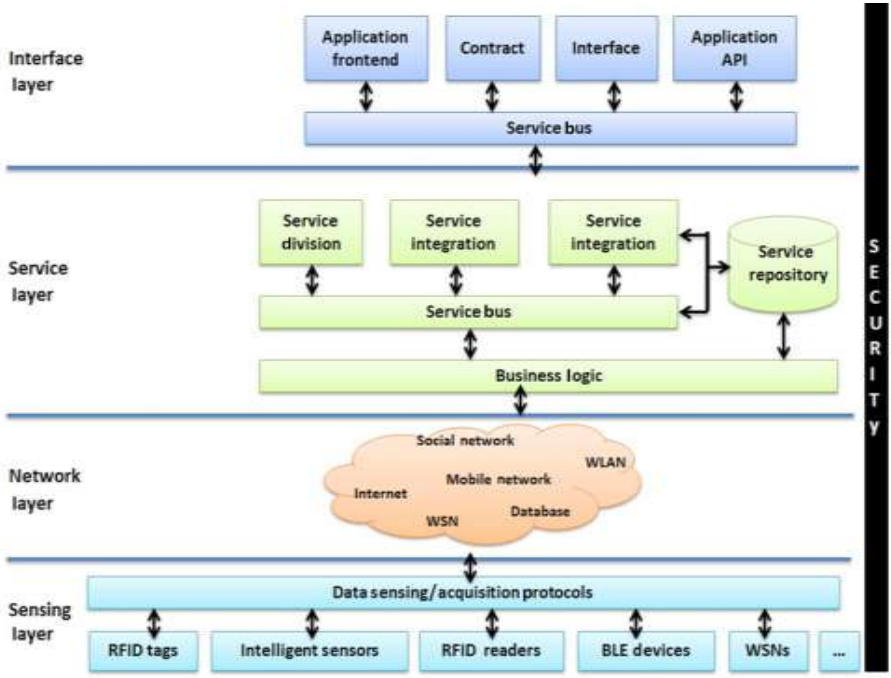

Fig. 2: Structure of IoT

Cloud Computing

There are several definitions are proposed for cloud computing which are accepted by the National Institute of Standard and Technology (NIST). The cloud computing has four different types of models, five basic characteristics and three types services. The deployment models of

cloud computing are classified as public, private, hybrid and community cloud which depends on how the resources are available to consumers through Internet. The public cloud is typically owned by the profitable organization such as Amazon web service where as private cloud is allocated to the single company to give services of particular sector of consumers (Microsoft private cloud). The private cloud provides information higher security and higher level of control. A hybrid cloud is the mixture of both public and private clouds that integrates the required characteristics of both clouds.

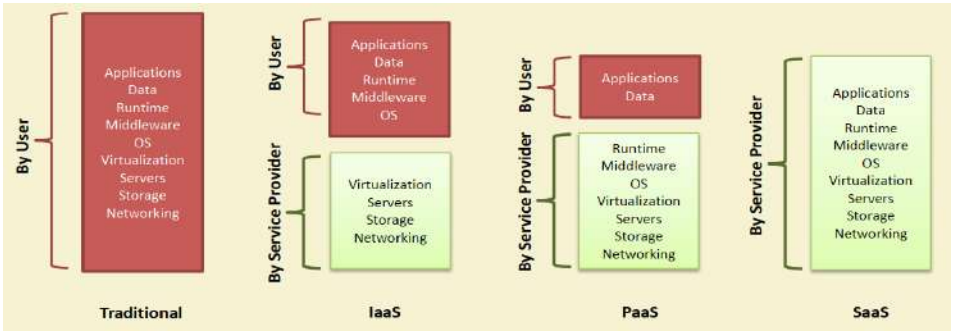

Fig. 3: Comparison of different cloud service models

A community cloud is the cloud which sends same information to group of consumers and also number of companies. Distributed cloud is the cloud which shares the information for collection of scattered set of computing devices in various locations. Public resource computing and volunteer cloud are the two types of distributed cloud. To increase flexibility and fault-tolerance, a multi-cloud which is multiple computing services are presented through single heterogeneous structure. To support interoperability, a inter cloud indicates that clouds of cloud through Internet globally. To enhance the flexibility of consumer, the cloud computing provides three different levels of services namely, SaaS, PaaS and IaaS. Fig. 3 depicts the comparison of services of traditional and cloud models. The SaaS is the service that the software is transferred over internet, example is Google apps. The PaaS provides higher level of service that offers integrated environment to build and test of certain software, example is Microsoft Azure. The IaaS is offering service in terms of infrastructure that is hardware, storage and servers, example is Amazon web services.

Need of Cloud Computing in IoT

Both cloud computing and IoT are developing rapidly with their unique characteristics and services to consumers. The IoT is characterized of large distributed things with low storage and processing capabilities. The things raise the issues in terms of performance in terms of reliability, scalability, security and privacy. The cloud computing featured more devices of a network with unlimited storage. It offers robust and flexible environment that integrates dynamic information from different information sources in the same network. With integration of cloud to IoT, the performance issues of both cloud and IoT are solved partially. Once cloud is integrated to IoT, information is sharing in uniform manner with a standard communication API thereby providing security, accessing information directly from anywhere. Another advent of this integration is IoT resources are deal with unprecedented infrastructure because cloud allows infinite storage with appropriate content. Prediction and data-driven decision making algorithms are presented with low cost, increased revenues and also reduced high risks. An essential requirement of IoT is to provide unique IP access for devices to share information over the dedicated hardware and also the communication among the devices is expensive. The cloud computing presents an affordable and effective solution like processing and tracking any device from anywhere to utilize the customized applications. Hence, the combined cloud-IoT technology solves complex problems thereby providing additional benefits such as ease of use, ease of access. Hence, it is indeed to the next generation in internetworking environment [8].

Challenges of Integrated Design

Though the combined cloud-IoT architecture solves complex problems, it also exhibits huge number of problems. Each application of integrated is showing different challenge thereby huge attention of research community. This integration imposes various challenges in the performance such as heterogeneity, scalability, reliability and big data.

1. **Heterogeneity:** One of the major challenges of integrated design is wide range of heterogeneous system such as devices, platforms, operating system and services used in different

advanced applications. The services of cloud computing are existed with proper interface, customized according to dedicated provider and causing resource integration. The heterogeneity of cloud computing is also non-negligible thereby exacerbating the issues when multi-cloud is utilized. These issues are solved partially with cloud breaking by third parties or cloud providers. If the services are depend on multiple providers, the performance and resilience of application are improved. Because things of IoT are tightly coupled with dedicated application, the service providers are required to conduct survey on the specified hardware and software, computing infrastructure and integrating heterogeneous system.

2. **Scalability:** The combined cloud-IoT design aims to develop massive system with large applications thereby requiring real-time devices to analyze the information. The large scale of devices results number of challenges to become system complex. With number of devices in the system, the scalability critical problem at each level including data sharing, data processing and service of networking. In addition to this, the distribution property of IoT creates tasks hard because the issues of connectivity and latency.
3. **Reliability:** Reliability is one of the major concerns for combined cloud-IoT design because of smart applications. There is a huge scope of occurring errors in integrated design such as intermittent to make the system unreliable. Applications like smart mobility, vehicular ad-hoc network becomes often unreliable because of its mobility in the cluster. In such applications, the resources are deployed in the constrained environment thereby occurring number of challenges such as device failure or device unreachable. The integrated system also exhibits uncertainties related to the resource exhaustion and data center visualization.
4. **Big data:** IoT is one of major sources of big data whereas cloud enables storing it for longer periods and process. Handling of this huge data is complex challenge since the performance of integrated design depends on the data management. On other hand, there is no perfect algorithm for the cloud to the data management. In addition to this, data integrity is one of main concerns because it affects the security and quality of service.

Security and Privacy

The combined cloud-IoT design allows transfer of data from cloud to real-world. The appropriate authorization rules are needed to be framed to access the information from the cloud. This is essential when privacy of users is major concern and also particularly data integrity is needed to be guaranteed. Several issues are arise when complex applications are merged with cloud because lack of information of service provider [9]. The public key of cryptography is not allocated entire layers since constraints of power deployed by IoT. New challenges can able to occur because of vulnerabilities such as hijacking.

Integrated Cloud-IoT Architecture

Based on literature, the IoT architecture consists of three layers that are network, perception and application layer. Fig.4 depicts the structure of integrated design. The sensing layer is used to sense data which is received from near things or surrounding environment [10]. A variety of sensor devices are used to acquire information from different sources such as RFID tags, cameras. A network layer transfers the data from the cloud or internet. Different number of protocols is existed in network layer to transfer data from perception layer to application layer. The primary service of application layer is interfacing of end-user.

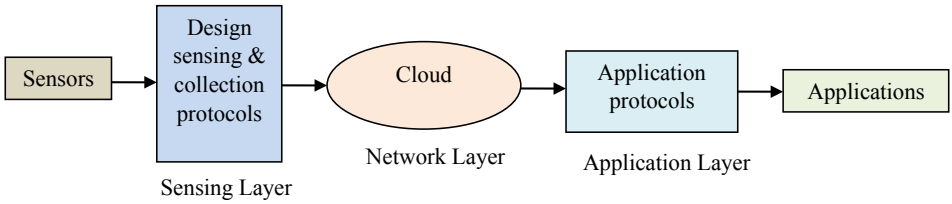

Fig. 4: Structure of integrated cloud-IoT

Applications of Integrated Design

The approach of cloud based IoT introduces large number of applications in terms of services of end-user. The integration of two different technologies shows variety of characteristics to obtain wide set of applications. Fig.5 shows some of major applications which builds on the integrated design.

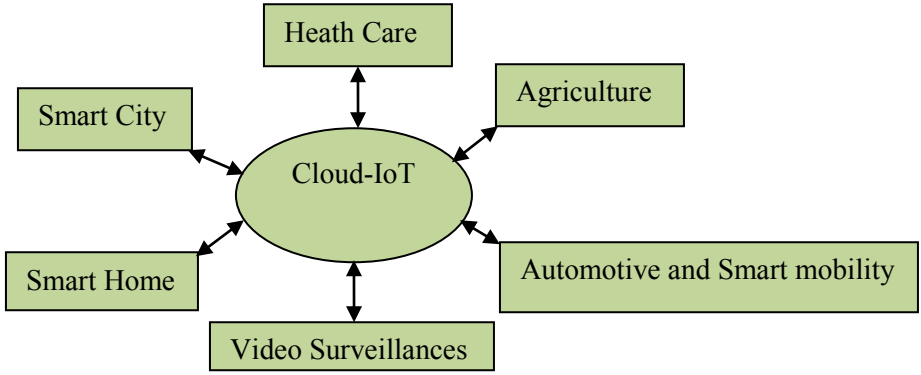

Fig. 5: Applications of integrated cloud-IoT design

Healthcare

Now-a-days, most of the hospitals are maintain the patient record with sensor networks and also monitoring the doctor to track of drug administration. The integrated cloud-IoT design significantly improves the healthcare services and it also advances the quality in medical domain by collaborating the different companies involved. The cloud-IoT design presents innovative applications such as collection of patient data through sensors nodes, transferring data to cloud of medical centers to share and process in Electronic Healthcare Record (EHR). An Ambient Assistant Living (AAL) is one of important applications to live ease for disabled people.

Agriculture

IoT empowers the developments of efficient crops in agriculture in terms of low production cost. The IoT achieves new agriculture infrastructure in various directions such as machinery agriculture, agriculture products and also data base systems. The important benefits of integrated design in agriculture are identifying need of food, tracing food with RFID, Monitoring plants and its surroundings. Monitoring of changes in the soil thereby inputting water, fertilizers, pesticides to the soil. These result to advance in the production of food products and efficient crops to the real world with an effective price.

Automotive and Smart Mobility

IoT is providing an effective solution of massive problems in automobile and transportation services. The integrated cloud-IoT design brings the benefits in terms of managing and reducing road traffic and also enhancing the road safety. The main purpose of cloud-IoT platform presets low cost, on-demand, secure and real-time services to the end-user. To extend the conventional cloud services, vehicular clouds are implemented to enhance the storage capabilities and on-demand computing.

Video Surveillances

The video surveillance is one of most important services for security related domain because it monitors continuous and manages the system by it-self. The integrated design provides the promising solution for complex problems such as video storage. It also proposes the effective solution in term of identifying and managing storage capabilities of video from the camera, load balancing and efficiency of data delivery and fault tolerance. The integrated design is supreme tool for video surveillance.

Smart Home

To empower the automation services in home appliances, the integrated cloud-IoT design is utilized. The cloud provides the best services in terms of huge data with less complexity. The smart home based cloud presents dedicated services in terms of home appliances. An Intelligent Remote control is one of examples of the integrated cloud-IoT design which controls and manages intelligently from anywhere. Several smart home appliances are proposed based huge literature.

Smart City

A middleware for future contained smart cities shall be presented through the IoT which attains the information from sensing devices such as RFID tags or geo tags and providing data consistently. Based on the recent literature, the integrated cloud-IoT design empowered in

terms of connection and integration for sensors and actuators thereby easing to applications to physical world of smart cities. The combined cloud-IoT improves the services and communication to the nearby environment such as Bigbelly, Smart streetlights [11].

Future Directions

The research on integrated cloud-IoT is still live because of lot of open issues and new applications. IoT6, a research project from Europe is dealing IP-V6 and other standards such as COAP, CORE to advance integrated cloud-IoT design. An APT is also standard protocol is used in combined cloud-IoT design to interconnect between advancement of services and smart objects. The complex data mining is one of another important directions integrated design because of complexity of Big data is not solved. Fog computing is new model which extends the services of the cloud computing. There is a huge scope of research in fog computing in particular domains such as smart-grid.

Conclusion

This chapter presented the structure of cloud-IoT design and its importance in various applications. This chapter neatly presented with challenges of IoT and cloud thereby identified the difference between two technologies and also highlighting the importance of the integrated cloud-IoT design. From recent literature, structure and applications of the integrated cloud-IoT is presented. Finally, the future directions of this advanced design are discussed with some open issues in particular applications.

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Improved Vertical Handoff Decision Scheme in Heterogeneous Wireless Network Based on SCS

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Abstract

Seamless continuity is the main objective and challenge in fourth era remote networks (FERNs). To help intelligent constancy in heterogeneous networks, the traditional vertical handover management (VHM) approaches are sufficiently bad. Thus, it is essential to manage those difficulties like a choice of a system and activating of contradictory handover. In heterogeneous remote systems, principle test is a consistent relationship of diverse systems like Wi-Fi, WI-Max, WLAN, and WPAN and so forth. This paper proposed a system called scatter cuckoo searches (SCS) algorithm for vertical handoff, the handover choice stage as well as to mitigate the handling delay and improve the fitness of nodes and quality of a network. We additionally contrasted along and GRA and TOPSIS techniques over SCS in view of the mobile terminal (MT) to get the availability with the best system it estimating by quality of service (QOS) parameters.

Keywords

FERNs VHM TOPISS GRA SCS QOS

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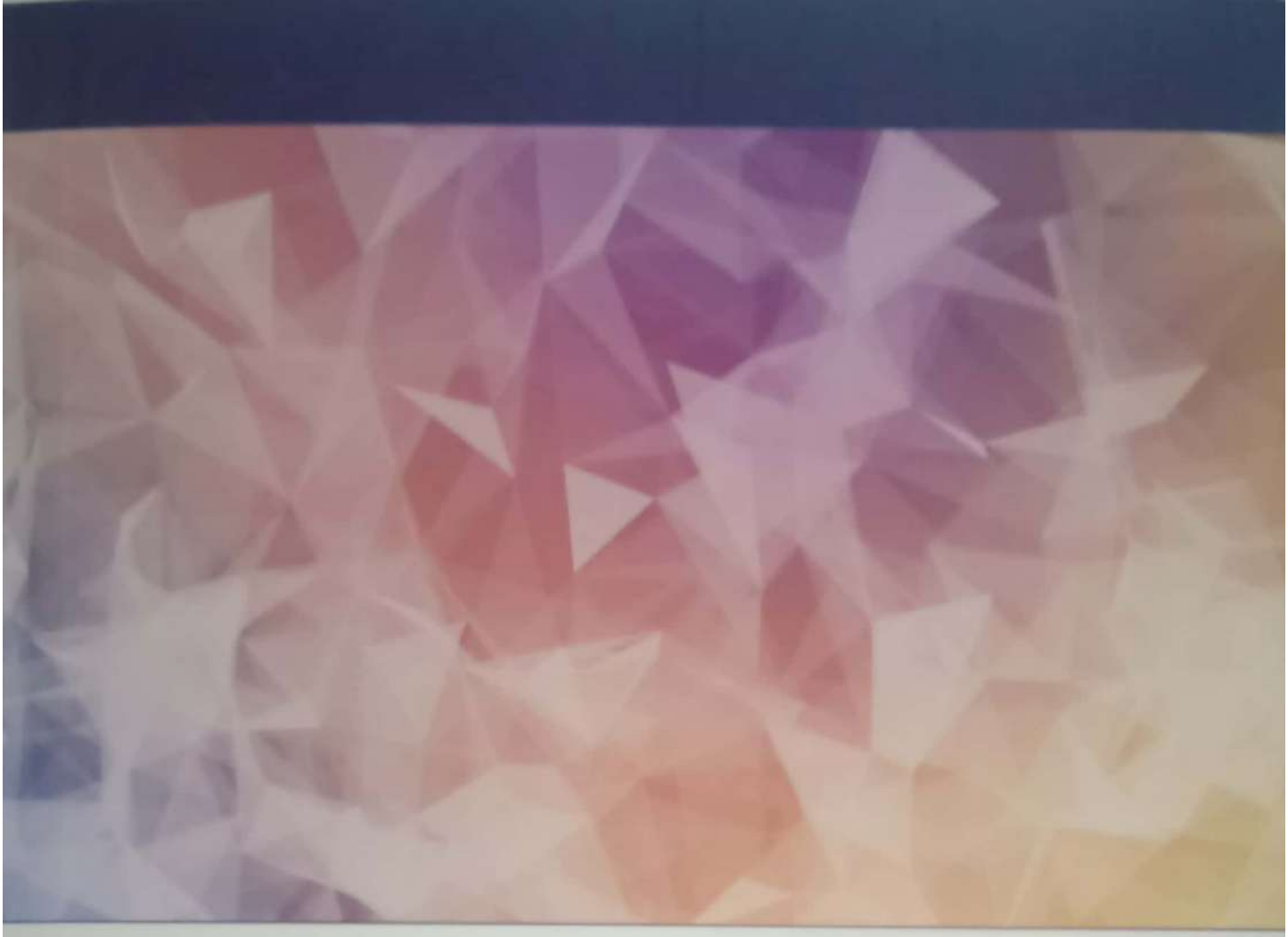

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Vijaya Pal Reddy Panuganti is working as Professor in the Dept. of Computer Science, Matrusri Engineering College Hyderabad India. He received his doctorate degree in Computer Science from JNTU, Hyderabad. He published Two patents and more than 40 research articles in reputed journals. He executed funding projects & many expert talks delivered.

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Vijaya Pal Reddy Panuganti

Content Word Selection Models for Gist Generation

Short Summary Generation

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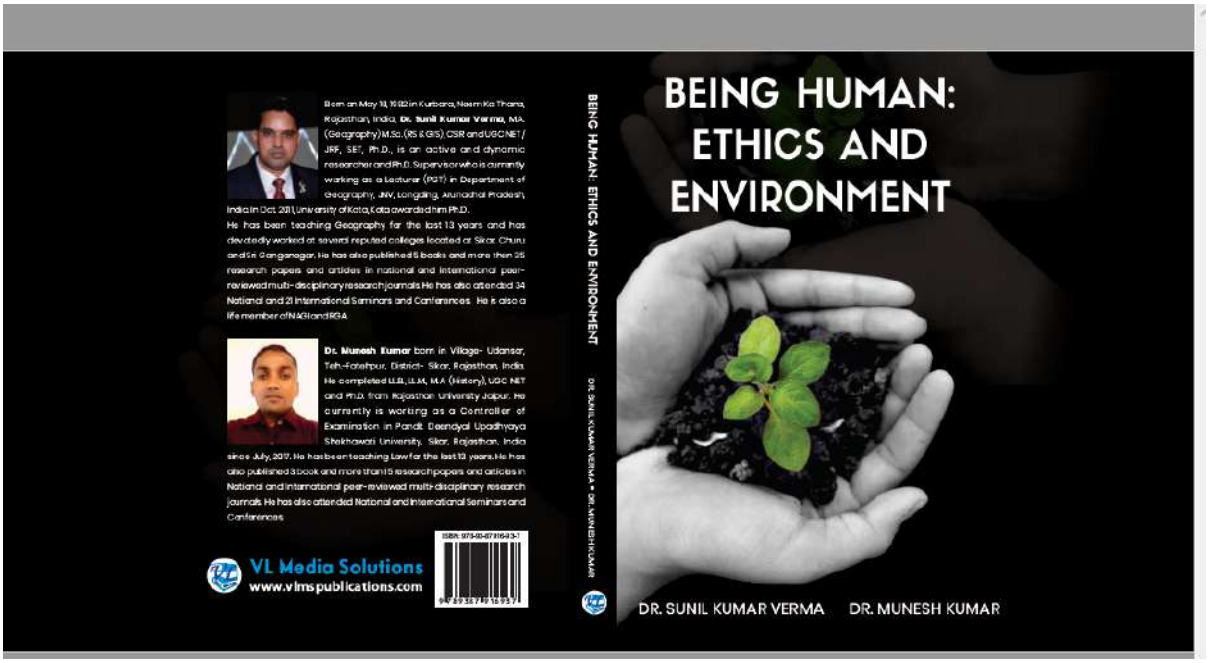
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Preface

It is worth mentioning that due to the increasing and unintended consequences of human economic activity and rapid population growth, unprecedented environmental changes took place in the first 21st century. These changes include depletion of natural resources and widespread pollution such as air, water, soil, and noise pollution. These changes have an unprecedented effect on the planet's climate and life systems. These changes also underline the conditions necessary for the continuation of the economic situation. Thus, human economic activities are considered to be sustainable in the present times. One could say that although the impact of economic growth has been environmental. Instead, zero growth will lead to global warming in the form of environmental degradation and threat.

Environmental ethics is one of the tools of modern environmental conservation and sustainable development. This is also a global problem in the outcome of development. But some people in underdeveloped and developing countries do not know its importance. Given the need for environmental ethics, it is easy for all of us to carry out our duties and responsibilities properly so that sustainable development can take place so that we can hope for a healthy environment for our future generations. Environmental ethics is linked to a sustainable environment and overall development. It teaches us to be healthy and interactive for the global environment and development. This virtue is based primarily on international environmental law under international humanitarian law, international human rights, and public international law.

The World Commission on Environment and Development defines sustainable development as "development that meets the needs of the present without compromising the ability of future generations to meet their own needs". There are some ambiguities in the concept of sustainable development and sustainability. There are two main concepts in the term sustainable development. First, the concept of needs, especially the critical need of the world's poor, which should be given

priority, and the idea of the limitations imposed by the state of technology, and second, the ability of social institutions to "present" and future needs. In addition to these two significant concepts, the four interconnected dimensions of sustainable development can be identified as economic, environmental, social, and cultural, because if long-term development is to be sustainable, there must be a balance between these four dimensions.

It is worth emphasizing that sustainable development requires a balanced pursuit of three things: environmental health, social equality, and economic well-being. It is based not only on the current generation of the population but also on the moral commitment to the welfare of future generations and the increased opportunities. Sustainable development is about ethics, as it asks attendees to consider not only the current situation of the poor but also the potential situation of the future population responsible for our production and consumption patterns.

Sustainability is a human construction in which man uses his environment for many purposes, including the enjoyment of necessities of life, production, and beauty. These objectives aim at enhancing lifestyles, maintaining culture, and preserving environmental quality for future generations, in line with the desire to sustain human life. Different objectives for the use of environmental resources have different expectations regarding what is to be sustained and what claims to make on environmental services.

We believe that sustainability is not a pure form of non-anathropontrism, but certainly it is enlightened from the anthropological and shallow environmental perspectives through which the ecological journey has begun. There is no question of changing the way we look at the nature of humanity to survive. Sustainable development is related to environmental justice because sustainable development can be restored through the process of environmental justice. We must not misuse our natural resources and we must conserve our natural resources for future generations.

We all know that we are in an environmentally dangerous period, like pesticides, ozone depletion, and increasing extinction rates in groundwater. When we think we are separate from the world, we also open up to the possibility of its exploitation and destruction. Thus we are the cause of destroying our environment. Humans must respond to nature to cope with their natural environment. Humans have a responsibility to nature, one of the most recent philosophical discoveries, though never before. Humans have always had an impact on their environment, killing and entertaining farms for food or plowing.

Like humans before us, we know the earth with its evolutionary story of the past, we know its present living creatures, plants, ecology, and we hold the future of the earth in our hands. The accumulation of that power is evident in the dangers of catastrophic extinction in the environmental crises of the late twentieth century. What had been "given" so late became a "bond". Humans are subject to great environmental abuse, such as dictatorships, such as perfect anthropomorphic or morally unrestricted attitudes. We do not yet have enough ethics for this planet and life on earth. To that end, the dissertation seeks to expand the scope of ethics, exploring the values that drive the natural world and the responsibilities of future generations. In this context, we have tried to introduce environmental codes of conduct, which we believe will solve the environmental problems of future generations and lead to global disasters.

The present book entitled "**Being Human: Ethics and Environment**" covers the various aspects of the environment in the present scenario suggesting the way of conservation. I am thankful to all contributors for their cooperation in compiling useful information on various facts of Environmental. Heartfelt thanks go to these contributors who have endeavored to provide up-to-date information on their area of expertise and have given willingly of very valuable time and knowledge. The ideas and notions expressed by the authors with the help of textual contents are innovative, and we have labored hard to popularise their valuable ideas by publishing them in the original shape. we are confident that the information contained in this book will be

useful to those who are interested in "**Being Human: Ethics and Environment**" for the benefits of human life and welfare.

The authors of this book are very grateful to their teachers & friends, Dr. S.S. Khinchi, Dr. M.Z.A. Khan, Dr. Pawan Kumar Sharma, Dr. Ramawatar Verma & Sh. Sushil Saklani who made them rich by offering timely comments and kept them elevated and confident during their research work.

The authors wish this work be so significant and trustworthy for further researchers in the future. Utmost care has been taken, even though printing related errors cannot be ruled out.

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Dr. Munesh Kumar

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A Review on Sustainable development - Facts and Challenges

Dr. Y. Aparna
Dr. B. Anjan Kumar

Abstract

This paper includes a review on broad perspective of goals, ethics, and policies of sustainable development. By addressing few problems on environmental issues we can construct few logical steps to address the Environmental sustainability. The factors and strategies that could help design sustainable cities are focussed. The need for sustainable development is weaved around different facts like climate change, over exploitation of natural resources and scarcity of resources. The paper also shows the linkage of poverty with certain environmental issues.

Introduction

"We do not inherit the Earth from our Ancestors; we borrow it from our Children"

Native American Proverb

Energy security is the major concern for all Countries in present scenario. Conservation of resources is the burning need. Due to overutilization of resources we are creating Junk in our own environment. Affordability, Sustainability and Reliability of global energy are interlinked with each other. The trade-offs between them require a comprehensive approach to energy policy. A powerful tool to address energy security and sustainability concerns lead to policy enhancements The climatic anomalies like heavy rain falls, hurricanes, floods, heat waves and drought conditions are pressing challenges faced by human civilisation in 21st century.

There is wide range of definitions for Sustainable Development, but the most recurrent definition is from the report Our Common Future (also known as the Brundtland Report). The Brundtland report (WCED, 1987) defined Sustainable

Development as "development that meets the needs of the present without comprising the ability of future generations to meet their own needs."

Sustainable Development Goals

They are framed for a better connectivity between People and Planet for profitable, equitable, bearable and viable correlation. In 2015, 195 nations agreed with the United Nation that they can change the world for the better. This will be accomplished by bringing together their respective governments, businesses, media, institutions of higher education, and local NGOs to improve the lives of the people in their country by the year 2030.

There are 17 Goals and each goal has roughly about 160 targets and these targets can vary from region to region. It starts with no poverty and ends with Partnerships for the goals.

Poverty to the highest degree restricts the magnitude and quality of food that people can procure. Poverty remains chiefly a rural problem. It is estimated that 76 percent of the developing world's poor live in rural areas, well above the overall population share living in rural areas, which is only 58 percent. According to Voluntary National Review Report on Implementation of Sustainable Development Goals. Our Country submitted the high level political forum to United Nations showing the progress towards specific goals under various schemes.

The progression of improvement of the human race does not necessitate vague growth in the utilization of energy and materials. We are surviving in incredible technical, economical and geographical transformation. This attempt at redefining progress has come to be known as sustainable development. To achieve Sustainable Development goals preparation and action at local, regional and global scales and framing short to long term goals allow the transition to sustainability. The Millennium Development Goals (MDG's 2000) can be achieved only with the implementation of effective long-term solutions in partnerships.

Science and Sustainable development

According to "Report Of The United Nations Conference On environment And Development" science can afford better understanding through increased research into the underlying

ecological processes and through the application of modern, effective and efficient tools that are now available, such as remote-sensing devices, robotic monitoring instruments and computing and modelling capabilities. Scientists, Research Scholars, Students and academicians provide a source of constant inspiration for upgrading technological aspects related to Sustainability. For example, global warming affects climatic conditions leading to melting of glaciers, rise in level of Sea etc., These changes can be monitored by satellite signals, cyclone warning centres and tide stations. The need to tackle climate change issues is considered as a strategic business challenge. The economic, ecological and cultural parameters must be chosen and linked with one another to promote the goals of sustainability. Similarly, pollution pertaining to air, water and soil can be studied under environmental pollution. The inter linking approach between environmental, social and cultural bodies pave the way for valuable assessment with regard to global sustainability. Numerous professional bodies like UN, UNESCO, The United Nations CSD (Commission on Sustainable Development). World Commission on Environment and Development (WCED), COP (Conference of the Parties), MDG (Millenium Development Goals) are involved in accomplishment of 17 Sustainable Development goals. In environmental matters, where evidences are indecisive, standards in dispute, stakes elevated and decisions imperative, scientists often need to follow methods that might not be appropriate in other scientific accomplishments. An attention-grabbing book "Silent Spring" published by Rachel Carson in 1962 is worth mentioning as this book focus on

documenting the undesirable environmental effects caused by the haphazard use of pesticides particularly DDT.

Sustainable Development and Renewable Energy

Renewable energy technologies include wind, bio fuels, solar, thermal, geothermal, and nuclear and photovoltaics. The global energy demand is about 16, 934 MTOE (Million tonnes of oil equivalent per year).The MNRE (*Ministry of New and Renewable Energy)* is promoting decentralized solutions based on different renewable energies to meet various electricity and thermal requirements. Its motto is "energy forever". The potential of Photovoltaics is part of the potential of all kinds of utilization of

solar radiation energy. Average conservation efficiency of a photovoltaic power system is typically 10-15%.

Geothermal energy sources are derived from convective and conductive hot water systems, which are detected by Physiometric points. The research centres, include GSI (Geological survey of India), ONGC (Oil and Natural Gas corporation) etc. These organisations provide crucial Earth Science information so that resources can be conserved. The changes in energy efficiency, energy savings and replacement of fossil fuels with renewable energy sources lie at the core of sustainable development.

Renewable energy (RE) has a strong synergy with some of the sustainable development goals (SDGs), thus its successful deployment can potentially result in an impact on these SDGs. The MNRE decided to provide custom and excise duty benefits to the solar roof top sector, which in turn will lower the cost of setting up as well generate power.

The causes of energy crisis are over consumption and over population. In tropical countries, 5000 trillion Kwh solar energy is generated per year. Apart from solar power the production of

electricity from moving water include large scale hydropower, small scale hydropower, tidal power plant and wave power plant.

Sustainable cities through renewable Energy

Cities are heeding towards renewable energy sources in order to improve the control of their energy systems. The desirable activities for a smart city include treatment of waste water, recycling of domestic water, hygienic sanitation system and uncontaminated transportation system.

According to Ministry of Housing and Urban Affairs, Government of India, the rationale approach of Smart Cities Mission is to constrain economic growth and progress in quality of life of people by enabling development in their area and harnessing technology that leads to Smart outcomes. This may include turning slums into better planned areas, thereby improving quality and outlook of the whole City. Implementing Smart Solutions will enable cities to use technology, information and data to improve infrastructure and services. This leads to generation of

employment, enhance the quality of life and raise income in urban areas, particularly for economically poor people.

Water conservation and sustainability

Water conservation involves all the policies, strategies and activities to sustainably manage the natural resource of fresh water, to protect the hydrosphere, and to meet the current and future human demand. In African Countries, the major cause of poverty is lack of drinking water. The goal of water conservation can be achieved through tangible efforts on the conservation and utilization of water on sustainable basis with a focus on holistic planning and sustainable development of sources of water. By managing the indoor, outdoor, industrial and agricultural conservation we can manage water usage.

Sustainable water utilization can be achieved by minimizing domestic water consumption, recycling of waste water, improving water infrastructure and by using smart irrigation techniques. The first National Water Policy was adopted in 1987. This Policy was formulated by the Ministry of Water Resources of the Government of India to administer the development and planning of water resources and their optimum consumption.

Conclusion

During COVID-19 the environment healed itself .Let us not over utilize the resources. From the findings of Sustainable Development goals, it seems that every citizen is responsible for health and wealth of our nation. It was observed in U.K that, Principal of a School is made responsible to look after each and every house number allotted to him to check the mental and physical health of student. It is the duty of every citizen to protect mother Earth. Let us learn to live within our needs.

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Design and Analysis of Koch Snowflake Geometry with Enclosing Ring Multiband Patch Antenna Covering S and L Band Applications

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Abstract

This chapter discusses the advancement in the performance of the Koch snowflake fractal antenna's behavior when it is enclosed in a circle. This design using the fractal geometry properties results in an antenna that resonates at multiple frequencies that are 2.141 GHz, 3.352 GHz, 4.260 GHz, 4.622 GHz, 5.161 GHz, 5.462 GHz and 6.910 GHz and the bandwidth at the resonant frequencies are 115.6 MHz, 60.2 MHz, 102.1 MHz, 139.2 MHz, 115.6 MHz, 102 MHz and 140.1 MHz, respectively. On comparing, this modified design of fractal antenna provides better results in S11 parameter than basic Koch snowflake design.

Keywords

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