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3.2.2 Number of books and chapters in edited volumes/books published and papers published in national/ international confere proceedings per teacher during last five years

A.Y: 2016-17

Sl. No.	Name of the teacher	Title of the book/chapters published	Title of the paper	Title of the proceedings of the conference	Year of publication	ISBN/ISSN number of the proceeding	Whether at the time of publication Affiliating Institution Was same Yes/NO	Name of the publisher	Index
1	Dr. Pallavi Khare	-	A Novel Algorithm for Detecting Heart Diseases	ICETESM-2017	2016-17	978-93-86171-32-0.	Yes	Sphoorthy Engineering College	1-14
2	Dr.Y.Aparna	-	Antibacterial and antifungal Study of some derivatives of Oxazolones	Science and Technology for Health	2016-17	-	Yes	Andhra Pradesh Akademi of Sciences, Amaravathi	15-22
3	Aruna kokkula	-	VLSI Architecture for Parallel Multipliers	7th International Conference On Recent Engineering & Technology, Organization Of Science & Innovative Engineering And Technology	2016-17	978-81-904760-9-6	Yes	Organization Of Science & Innovative Engineering And Technology	23-27

4	B.Indira Priyadarshini	-	A Novel Algorithm for Detecting Heart Diseases	Internationsl Conference on Emerginh Trends in Engineering ,Science and Mangement ICETESM-2017	2016-17	ISBN: 978-93-86171-32-0.	Yes	Sphoorthy Engineering College	28-41
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A NOVEL ALGORITHM FOR DETECTING HEART DISEASE

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ABSTRACT

In this paper we present the RRP algorithm with new adaptive method with new solution to resolve respective problem RR interval algorithm in heart signal processing. At first we focus on some previous research, to conclude that, the important ECG processing algorithms discussed on deviation of ST section, width, height and duration of ORS complex of heart signal, efficient diagnosis, noise filtering contain baseline shifts, muscle artefacts and electrode motion. Also RRP algorithm include three parts of signal processing, determination signal features and compare with previously established patient heart signal. In the last stage, using adaptive threshold values for peak detection routines were used for the heart patients with various conditions. The algorithm efficiency is simulated and compared with conventional RR interval algorithm by MATLAB.

Keywords: ECG; Heart; QRS Detection; RRP Algorithm.

I INTRODUCTION

ECG is a graphical representation of the heart impulses. A conventional ECG waves formed under contract with the letters P, Q, R, S, T, have been named. Result of impulses natural speed and direction makes normal sinus rhythm. Otherwise, represent the heart disease. Waves, Q, R, S forms a group together as QRS complexes are discussed. The Complex QRS, ventricular electrical depolarization wave (contraction of the ventricles) show. The Broad QRS duration indicates abnormal or prolonged ventricular polarization.

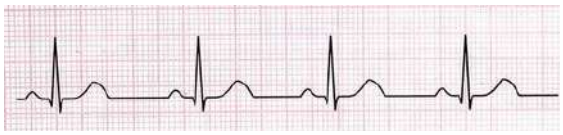
Segment ST, this piece of time between the completion and start depolarization ventricular muscle. This item may be a transient ischemia and muscle damage goes up or down.

T wave represents ventricular depolarization, if it is negative definite MI.

In sinus tachycardia as shown in fig 1, the production rate is faster than 100 beats per minute and In sinus bradycardia the production rate is less than 60 beats per minute, but the signal will be guided by the normal

Normal Sinus Rhythm

Sinus *Tachycardia*



Sinus Bradycardia

Figure 1: A sample graph for Heart Disease

Tachycardia, arrhythmia include irreducible, ventricular tachycardia, ventricular fibrillation ventricular tachycardia irreducible fibrillation, PSVT atrial flutter, fibrillation atrial tachycardia, atrial multifocal, tachycardia, atrial attack.

Sinus bradycardia include Stop arrhythmia, ventricular escape rhythm at Block Level 3, Block mobitz type II.

II LITERATURE REVIEW

In the last decade, a lot of new techniques have been proposed for the detection of QRS complexes, for example, algorithms based on artificial neural networks, genetic algorithms, and wavelet transforms, filter banks and hierarchical methods based on nonlinear transformations.

First Detection Algorithm

As noted in Section A, ECG frequency band is between 15 to 150 Hz. Baseline oscillation frequencies below 1 Hz and above 150 Hz frequency noise is caused by the muscles. The pre-processing algorithm is divided into two parts.

*Filter :*feature extraction stage with linear and nonlinear filters

• *peak detection* : To find the location & duration of the peak signal

The decision algorithm is divided into three phases

• *Ventilation :*threshold values are determined

Based on peak detection, signal levels and signal to noise ratio (Two sets threshold values are used to detect heart signals (a) filter threshold values (b) integrated window threshold values)

• *Learning:* The RR interval Average value and the heart rate limit

bound.

• *QRS detection :*QRS wave detection and differentiation of T –wave measurements.

Fetal heart rate Bit calculation algorithm

Fetal heart rate is one of the few signals which may register as a noninvasive.

In many cases the only available information source is the power

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spectrum of fetal heart rate. The fetal heart rate algorithm is performed in two stages.

• *Filter:* the best estimation frequency for low pass filter is 2 Hz. the output waveforms is some bumps without any sharp point

• *Autocorrelation:* the bit rate is obtained with frequency domain autocorrelation. Heart rate corresponds to distance between the cardiac cycle (n) and the cardiac cycle earlier (n-1).

ECG ASPARS algorithm is a three-stage High Resolution QRS Detection model:

Algorithm can be divided into three stages:

1. *Estimation:* The initial estimation obtains the valid R wave points.

2. *Squares:* Chi-squares non-linear function for computes. The average values for each data points with 20 KHZ sampling rate. The classification rules are based on numerical slope, amplitude and width signal analysis. Peak Level is used to distinguish noise from signal, which is usually half of the maximum peak to peak values.

3. *Peak detection:* data extraction of the R wave with a peak detection window which is placed on the centre of valid points.

III PATTERN RECOGNITION METHODS

The classes of patterns are pre specified ratio, Classifier algorithm called pattern recognition which makes the class attribute pattern. Pattern recognition techniques have generally fall into three categories:

1. *Statistical methods:* patterns and classes are generated with probability distribution.

2. *Structure (analytic):* patterns and classes are characterized by formal structures. In these methods, the basic units are defined as Primitive. All models are expressed in terms of the inter relationships between Primitive Grammar. In most cases, these methods are applied to certain structural pattern.

3. *ANN:* artificial neural networks, each pattern are described in terms of several characteristics. Point's attributes are considered in a multidimensional space. Feature space is divided into several regions corresponding to each class. Pre specified classes in supervised classification by training data determine the boundaries of different classes, there confirm the marked areas. Template feature vector obtained through measurement or observation. in general , Pattern recognition includes the following system components :

• *filter :*Register sensors and pre-processing

• *Patterns:* Feature Extraction which specifies the attributes. Suitable properties have two important properties: First, all models have the collection properties which belong to the same class. Second, the patterns are belonged to other classes do not have those features.

• *Classifier:* classifier which has feature space into regions are labelled and related to each class partitions. The classifier is characterized by the collection set of discrete functions.

• *Monitor:* the Monitor provides information about the training data.

In unsupervised learning data is corresponded to classes without any initial information. In the clustering step, basically, similar to supervised learning, the data is placed in different clusters.

A. Error back propagation algorithm (BPA) used in neural networks.

Artificial neural networks (ANNs) networks are inspired by living organisms that are used in pattern recognition. ANN classification Decision making process in medical data characteristics is suitable. Usually, multilayer neural networks using error back propagation algorithm (BPA) which is the nonlinear classifier, with supervised learning algorithm. The recursive function for learning process always calculates a mean square error cut, to minimize the overall error, initial weights are selected randomly, and then frequently connections weights have been changed to reduce the overall errors. It is desirable that the training data set distributes uniformly in the input neurons. The algorithm consists, the two main routes, with forward and backward path.

1. *Forward path:* An educational model is applied to the network, its effects on intermediate layers through the output layer and spread until eventually obtains the actual network output. In this way, the MLP network parameters (weight matrices and bias vectors), are considered fixed and unchanged.

2. *Backward path:* the opposite direction, the MLP network parameters are adjustable. Error vector is equal to the difference between the desired response and the actual response.

Learning algorithm BPA is based on the approximate calculation which can be reduced by the equations below:

The algorithm convergence speed is slow, Sometimes instability called oscillatory and network parameters is also called divergent, the network has a local minimum points may not be sure that an optimum solution is reached. Convergence of the algorithm is dependent to the initial values of MLP neural network parameters, so that a good choice would be a great help in faster convergence, vice versa.

B. Automatic gain control AGC algorithms with adaptive filtering

Adaptive filtering enables us to have a reference value, internal setting collection, optimize performance in noise wide range. The filtered analog output signal is controlled by changing the amplifier gain with recursive algorithm, In fact, algorithm are presented as gain amplifiers automatic code to set the adaptive digital filter threshold values .

C. QRS Detection Algorithm with FPGA

FPGA consists an array include hundreds of configurable blocks, which can run all kinds of digital logic functions with blocks connection wires. The logical functions performed by each blocks and the electronic switch controls wiring between blocks. The switch configuration is determined in the FPGA configuration memory cells contents. FPGA is used in the cardiac signals analysis and diagnose heart defects by wavelet transform with ALS Adaptive Lifting Scheme implementation, Split into three stages.

1. Split: To break even and odd signal into two signals from ECG signal successive samples.

2. *Filter:* The noise which is reduced with update the step pass filter.

3. *Detection:* Predict step which improve the detection accuracy.

D. Mapping algorithm with delay Phase Portrait

1. *Register:* to receive signals from the sensors and data mapping in two dimension space.

2. *Filter:* low-pass filter with preprocessing and computation Phase Portrait

3. *Peak detection:* if R peak value is bigger than threshold value then QRS decision rules runs, otherwise if the R peak value is bigger than RR intervals mean value then reduces the threshold value and also decision rules runs.

E. Multivariate cardiac signals analysis algorithms

1. *Register* : to receive signals from sensors

2. *filter :*Pre-processing and filtering

3. *Pattern:* Feature Extraction which specifies the attributes.

4. *Classifiers :*which has feature space into regions

5. *Training:* Supervisor will provide information about each categories training data. Accordingly, the feature space regions boundaries will be determined.

6. *Learning:* unsupervised learning is without any initial information about the class corresponds data.

IV WAVELET TRANSFORMS METHODS

Fourier transforms to obtain the filtered signal in the time domain. Unwanted and undesired frequency components from the signal frequency spectrum are removed. Finally the inverse Fourier transform executes. The main idea is that the signal frequency spectrum made up a trigonometric functions combination which is converted by Fourier transforms Frequency and then inverse Fourier transform.

A. MALLAT Algorithm with wavelet transforms dyadic discrete

MALLAT algorithm is more suitable for discrete signals with discrete wavelet transform may be implemented by the number of times. The high and low pass filters make impulse response . with finite length The down sampling action removes redundancy from signal and can increases pass MALLAT algorithm with wavelet transition .filter later stage signal scale delayed can detects the heart defects by octet equivalent filter bank.

B. The algorithm combines Wavelet transform with QRS wave detector

Method implementation Wavelet transform with Analog QRS wave detector with Gabor wavelet filter, constant circuit, Peak detector and comparator. Adjustable threshold value is calculated according to the following formula

C. Power computation algorithm

The heart signal processing is implemented by two moving average filter and low pass filter with enhanced features based on the signal power value, consists the three stages.

1. Filter: pre-processing using pass filters

2. Process: signal processing

3. Detect: Locate and QRS detection

D. Re sampling algorithm

The combination of Fourier transform and re sampling to make extract signal components ability, which consists of four stages.

1. Detect: QRS detection stage
2. Transform: the wavelet transform of ECG signal two-dimensional array.
3. Process: the pure signal is extracted from the two dimensional array.
4. Reconstruction: signal reconstruction phase

V METHODOLOGY

RRP is a new algorithm which is purposed with combination of some before algorithms.

A. RRP algorithm explanation

The RRP algorithm's first step makes a reference signal from patient's heart, this original storage can be save by the physician or patient. Then signal parameters are measured and applied to algorithm's input. The algorithm's result corresponds to patient's heart.

The signal parameters include heart rate and signal amplitude will be calculated up to 15 seconds. (This generally ensures substantial reduction the muscle and electrode motion noise).

B. Two algorithm's assumptions:

1. T*achycardia:*To ensure that we suppose , wherever heart rate is greater than 100 beats per minute (in both normal and alarm status), arrhythmia or tachycardia rhythm is issued
2. *Bradycardia:* To ensure that we suppose, whenever the heart rate is lower than 60 beats per minute in both the state's normal rhythm arrhythmia and bradycardia is issued.

C. Algorithm steps:

*1. Filter low :*remove Baseline Noise

2. *Least Square:*Remove the noise filter (zero phase) and Least Squares (Least Sq.) with appropriate sampling frequency
3. *Resample:*Interpolation calculated using the Resample FFT points
4. *Filterhigh:*Noise muscle electrode movement
5. *RR interval:* Calculate the RR interval calculations based on peak detection threshold values based on a patient's signal.
6. *Sliding window:* Calculate the minimum and maximum frequency values for heart signal sliding window.
7. *Process 1:* calculate the RR interval parameters sinus tachycardia, sinus arrest or heart diagnosed as Function absence of atrial sinus node is known from bradycardia status.
8. *Process 2:* control and distinguish the QRS, P, T wave for Diagnosis arrhythmias from tachycardia.
9. *Process 3 :*Risk rate was normalized to the corresponding alarm will be issued

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VI RESEARCH SIMULATION

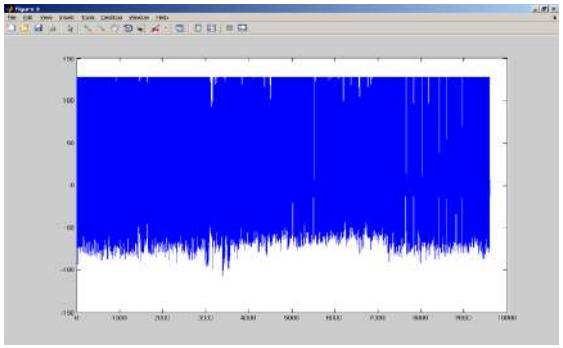


Figure 2: Heart signal with noise diagram

In the next stage, the baseline noise is removed by subtracting the average signal with formula:

Using ECG - mean (ECG) as shown in fig 3

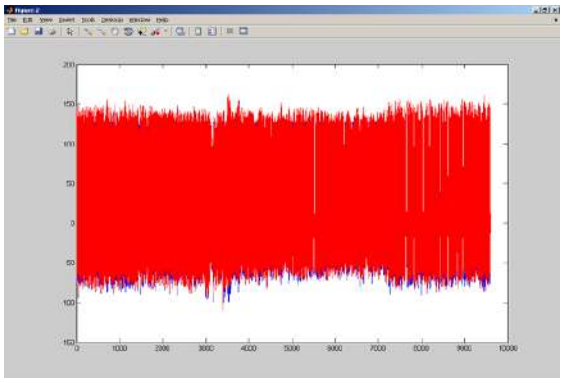


Figure 3: Remove Baseline Noise diagram

In next stage, the zero phase digital filter is applied to ECG signal processing the without Baseline Noise in both the forward and backward directions. The result has many characteristics such as reduce noise and preserves the QRS complex at the same time without making delay .as shown in fig 4 , FILTFILT function in MATLAB simulates it.

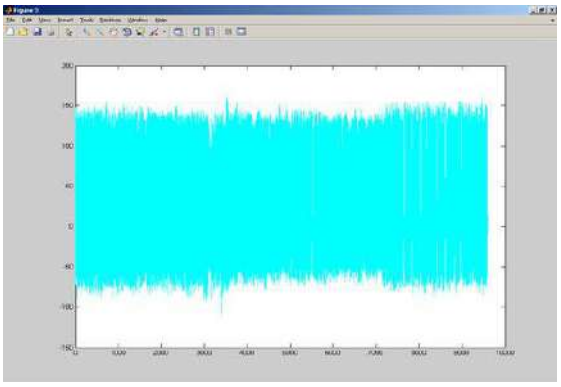


Figure 4: Zero phase noise removal filter and Least Squares diagram

In the next stage, one dimensional interpolation with Fourier transform (FFT based) method applies to calculate the Resample two percentage points. As shown in fig 5 INTERPFT function in MATLAB simulates it.

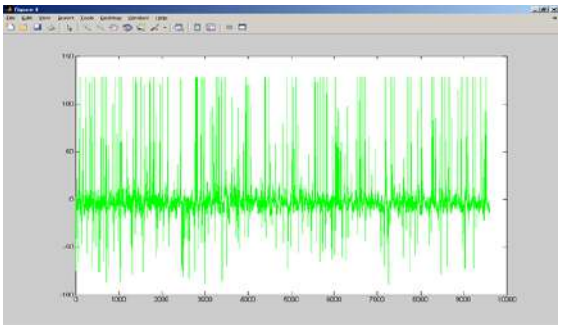


Figure 5: Interpolation FFT Resample method

In the next stage, one dimensional median filter is applied with the sliding window which replace the center value by mean pick points value(That's a nonlinear method). As shown in fig 6, INTERPFT function in MATLAB simulates it.

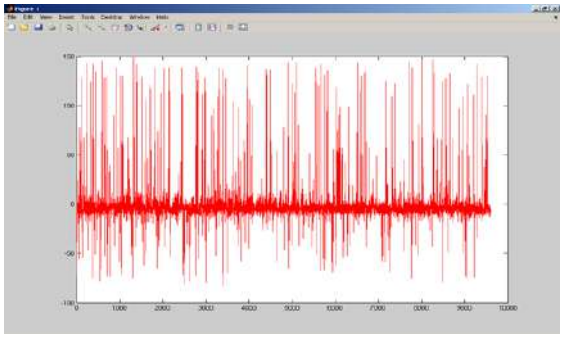


Figure 6: Noise filter with least squares and 2 Hz sample frequency

In the next stage, the conventional thresholds values are applied to peak detection routines. As shown in fig 7, with MATLAB Programming simulates it.

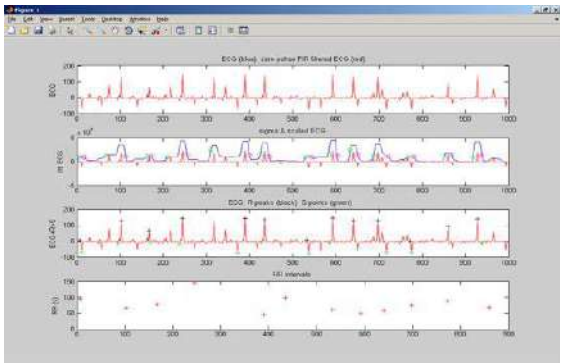
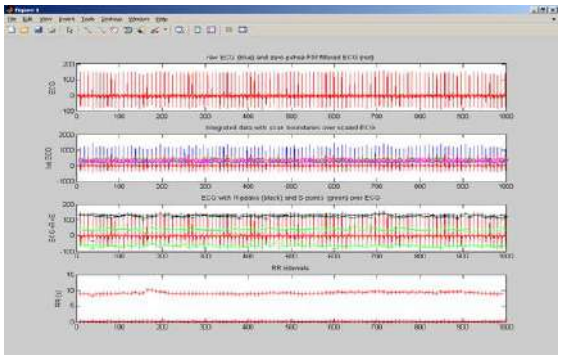


Figure 7: RR interval calculated based on peak detection calculations

In the next stage, the conventional thresholds values are applied to peak detection routines for patient's heart signal. As shown in fig 8, with MATLAB Programming simulates it. Which is useless result for Established heart disease?



VII CONCLUSIONS

In this paper, some important algorithms in the cardiac arrhythmias, time and frequency field and by linear and nonlinear functions was described. At the end, the combination of these algorithms which provides a new algorithm with more flexibility in heart pulse counting and QRS, T, P wave detection. Obviously this method has been as a diagnostic tool to assist physicians in cardiac disease analyzing. However in generally, these tools result never has 100% recognition accuracy. The accuracy of these tools depends on several factors; include the threshold values which are main matter in this new algorithm. Of course, as the simulation results presented demonstrates, the RRP algorithm's accuracy and efficiency is high. As a general conclusion it can be said that the RRP algorithm can be used as a diagnostic tool for heart health trustworthy.

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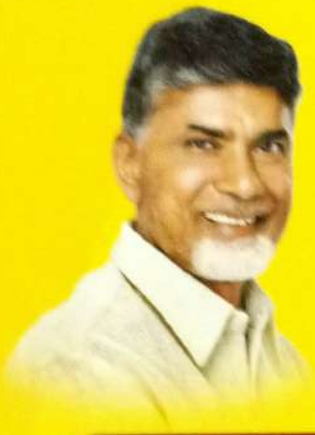

Andhra Pradesh Akademi of Sciences, Amaravathi

APAS

2nd Andhra Pradesh Science Congress

[APSC-2016]

Focal Theme :

SCIENCE & TECHNOLOGY FOR HEALTH

7-9 NOVEMBER 2016

1986

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Science & Technology for Health

Abstracts

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CMPS-OP-037

Antibacterial and antifungal studies of some derivatives of Oxazolones

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Abstract

In view of easy availability and diverse reactions of 2-oxazolin-5-ones there is enormous scope for using them as synthetic intermediates for different heterocyclic compounds. It would be worthwhile to explore the chemistry of these 2-oxazolin-5-ones further and to examine their scope.

Seven (4Z)-4-(arylidene)-2-(2-hydroxyphenyl)oxazol-5(4H)-one derivatives were prepared under milder conditions were prepared by Erlenmeyer method. Physical constants like melting points,structural elucidation by IR,^{1}H-NMR and Mass spectra were carried out.These Erlenmeyer azlactones which are 5 membered heterocyclic compounds containing N and O as heteroatoms.The C-2 and C-4 positions of azlactones are crucial for their various biological activities like antibacterial,analgesic, antifungal,anticancer, anti-inflammatory,neuroleptic, sedative ,antidiabetic.and antiobesity. They also exhibit promising photophysical and photochemical activities and as PH sensors.

All the synthesized oxazolone derivatives were screened for anti-bacterial activities by disc diffusion method against Staphylococcusareus, Bacillusmegaterium (Gram+ve);E.coli and Pseudomonasaeruginosa(Gram-ve)bacterialstrains,and antifungal activity against Candidaalbicans, Rizopus microsporus var. oligosporus.

The activity studies of all the synthesized compounds against bacterial strains in both gram positive and gram negative activity against bacterial strains revealed that all the compounds shows moderate activity against Pseudomonas aeruginosa MTCC No. 1034compared with standard pencillin.Activity against Fungi Rizopusmicrosporus var. oligosporus (MTCC No: 2785) revealed that five compounds out of seven showed good activity at 100ìg/ml.

In view of their further scope in various pharmacological activities, we have prepared few metal complexes with Co,Ni,Cu,Mn,Fe,Pd chlorides and acetates.

CMPS-OP-038

Chemical Examination of Desmodium gangeticum leaf extracts.

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Abstract

The genus Desmodium belongs to Fabaceae family and contains about 350 species which are distributed in tropical and subtropical zones all over the world. Desmodiumgangeticumis one of the medicinally important species among the genus Desmodium. It is used in traditional medicine as bitter tonic, febrifuge, antiemetic and in inflammatory conditions. According to literature survey D. gangeticumpossess antioxidant, anti- nociceptive, anti-inflammatory, antiemetic, cardio- protective, antimicrobial and anti-ulcer effects.

Present work involves the isolation of biologically active compounds from the leaf extracts. The air-dried powder of the leaves was extracted with hexane, ethylacetate and methanol by serial exhaustive extraction method. The extracts were subjected to column chromatography on a silica gel column eluted with solvents of different polarities. Five flavonoids were isolated from the extracts. They are characterized based on IR, ^{1}H NMR, ^{13}C NMR and MS studies as formononetin, pongachromene & 3-methoxy-7-hydroxy kanujin and 7-O-Methyl chrysin & 4', 7-dimethoxy-5-hydroxy flavones.

Antibacterial and Antifungal Studies of some Derivatives of Oxazolones

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Abstract

A series of seven novel oxazolone compounds were synthesized and structures were confirmed by ^{1}HNMR. ^{13}CNMR,IR,mass spectra and elemental analysis studies. Antibacterial and antifungal studies were carried out using disc fusion method. The compounds were tested by taking penicillin as a standard. All the compounds exhibited moderate to good activity against selected bacterial and fungal species.

Keywords: oxazolones, antibacterial, antifungal, disc fusion

1. Introduction

Since decades, development of antibacterial drugs with minimal side effects is a challenging task for medicinal chemists .In this view, synthesis of new drugs with different mode of action are needed to be explored. Heterocyclic compounds are organic compounds that contain a ring structure containing atoms in addition to carbon, such as sulfur, oxygen or nitrogen, as part of the ring. They may be either simple aromatic rings or non-aromatic rings. Some examples are pyridine (C_5H_5N), pyrimidine ($C_4H_4N_2$) and dioxane ($C_4H_8O_2$).Heterocyclic compounds form interface between Chemistry and biology leading to a new scientific insight in drug discovery.The synthesis and the importance of azlactones were studied by many researchers shows various biological, medical and industrial activities. The C-2 and C-4 positions of azlactones are crucial for their various biological activities like antimicrobial[1] antibacterial[2], analgesic[3] , antifungal[4] anticancer[5], anti-inflammatory[6] ,neuroleptic[7], sedative[8] antidiabetic[9] and antiobesity[10]. Azlactones are important intermediates in the preparation of several chemicals including Aminoacids[11], peptides[12], some heterocyclic precursors[13] as well as coupling and photosensitive devices for proteins[14]. They exhibit promising photophysical and photochemical activities [15-16] and as PH sensors[17] .By conventional methods, azlactones are synthesized by aminoacids,from α-haloacids, diazonium salts.Microwave Irradiation and ionic liquids were also used under green synthesis.

1.1. Materials and methods

1.2 Materials

All chemicals and reagents were of analytical grade and purchased from SD Fine-Chem Limited .

1.3 Preparation of *oxazolones*

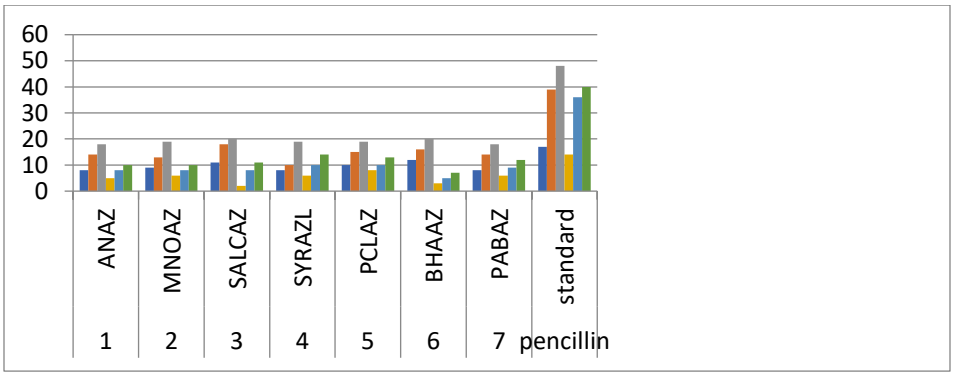
The Erlenmeyer-Plochl azlactone synthesis is a sequence of chemical reactions which convert glycine to various other amino acids via an oxazolone and an azlactone. In this process, the interaction between aldehydes or ketones and acylglycines or aroylglycines in the presence of AC_2O along with CH_3COONa gives the corresponding 4-(alkylidene or arylidene)-2-oxazolin-5-one derivatives Perkin condensation with aromatic aldehydes.

2.Antibacterial studies

The compounds synthesized were screened for their antimicrobial activity by Disc Diffusion Method.In this process the sensitivity of the compounds is calculated by determining the zone of inhibition after placing the paper disc dipped in solution of compounds, on LBS agar medium, which was formerly inoculated with test organism. These results were compared with the zone of inhibition produced after placing disc dipped in the solution of standard antibiotic. The diameter of zone of inhibition is directly proportional to antimicrobial activity of the compound. The

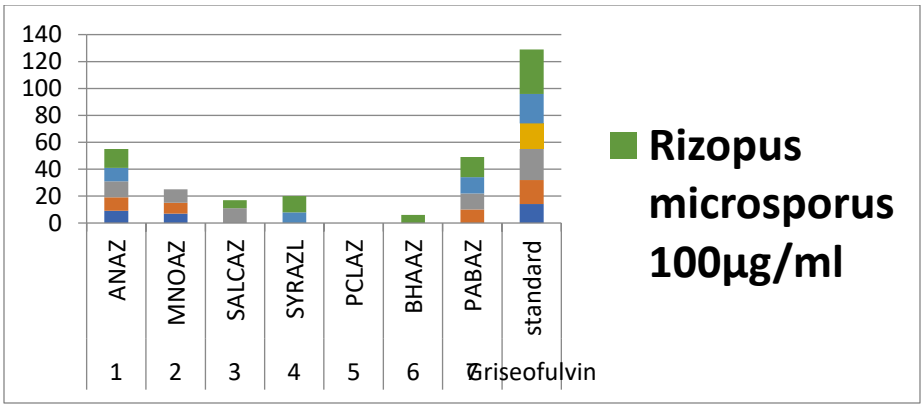
size of zone of inhibition depends on rate of antibiotic diffusion, rate of bacterial growth and incubation condition, concentration of organism. All the synthesized compounds were screened for their antimicrobial activity against two gram positive-Staphylococcus aureus, Bacillus subtilism and two gram negative species- Escherichia Coli,Pseudomonas aeruginosa and antifungal activity against two species Candida albicans, Rizopus microsporus.

	Activity Results of Antibacterial Strains(Gram +ve)						
compd No	code	Activity against Bacillus subtilis (MTCC No.6544)			Activity against Staphylococus areus(MTCC No.3160)		
		25µg/ml	50µg/ml	100µg/ml	25µg/ml	50µg/ml	100µg/ml
1	ANAZ	8	10	16	5	4	10
2	MNOAZ	9	12	12	8	5	10
3	SALCAZ	9	14	17	2	8	11
4	SYRAZL	5	10	19	6	8	7
5	PCLAZ	8	15	19	8	10	13
6	BHAAZ	4	12	15	3	5	7
7	PABAZ	5	8	15	5	9	12
Pencillin	Standard	17	39	48	14	36	40



4.Antifungal studies

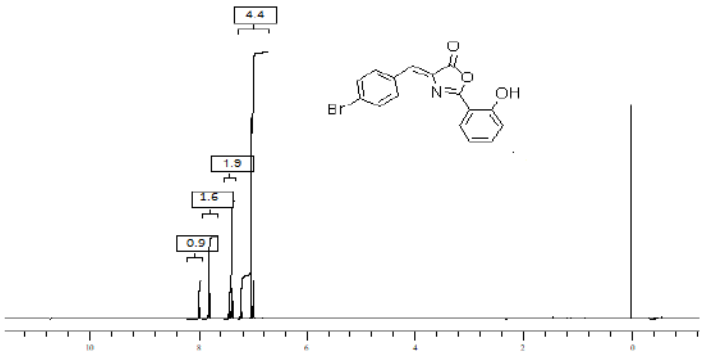
The antifungal assay is performed by using two fungi , *Fusarium ricin*i and *Phytopthoranicotiana*. Potato dextrose agar plates were made and 5mm diameter fungal plugs were placed carefully at the center of the plate around which 5mm wells were made using sterile well borer based on number of samples. The wells were loaded with 100µl of samples each and one well with antifungal chemical as standard. The plates were incubated for 96 hours at 25°C and results were noted.



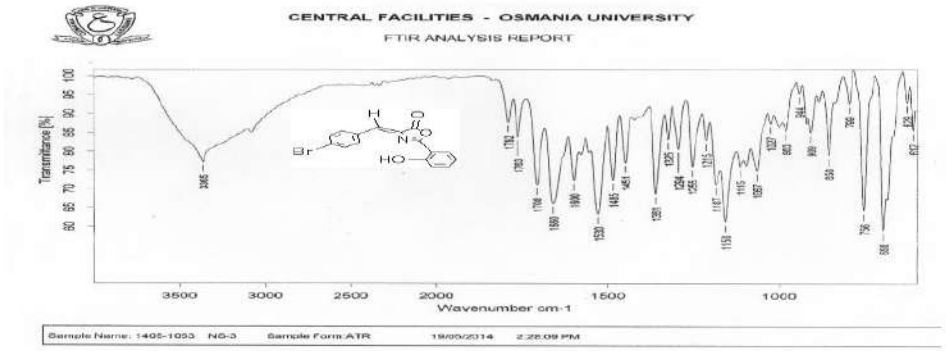
3.Results and discussion

As a representation to support the spectral studies, 4-(4-bromo benzylidene)-2-(2-hydroxyphenyl)oxazol-5(4H)-one was chosen. In the IR spectrum , the characteristic stretching frequency(C=O) was observed at 1786 cm^{-1}, (C=N) at 1653 cm^{-1} and (C-O-C) at 1224 cm^{-1}. The ^{1}H NMR spectrum (400 MHz, $CDCl_3$,) **(** of compound showed multiplet between δ 6.59 to δ 7.2 due to aromatic and δ 8.2 ethylenic proton.In ^{13}C NMR spectrum **(**100 MHZ, $CDCl_3$) showed δ109.3 due to ethylenic carbon, δ 119 - δ 134.2 due to aromatic carbons, δ161.6 due to C=N, δ 166 due to C-OH and δ168.3 due to carbonyl carbon were observed. ESI-MS mass spectrum of compound appeared at m/z 345 .The CHN analysis of showed percentage of C ,N and H as 55.72 ,4.15 and 2.86 respectively which was matching with calculated values.

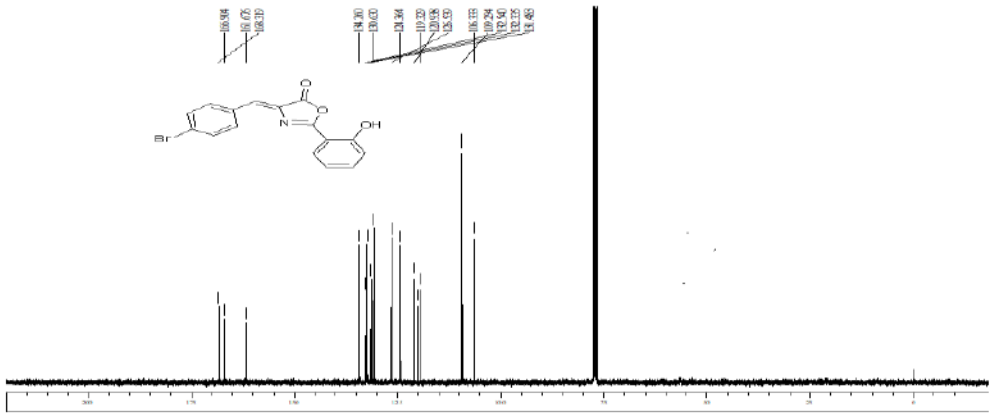
3.1 ^{1}HNMR Spectra



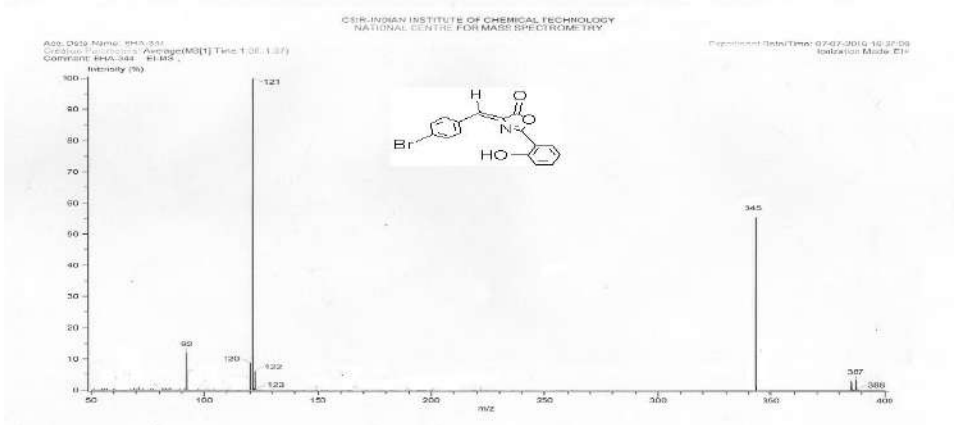
3.2 IR Spectra



3.3 ^{13}CNMR



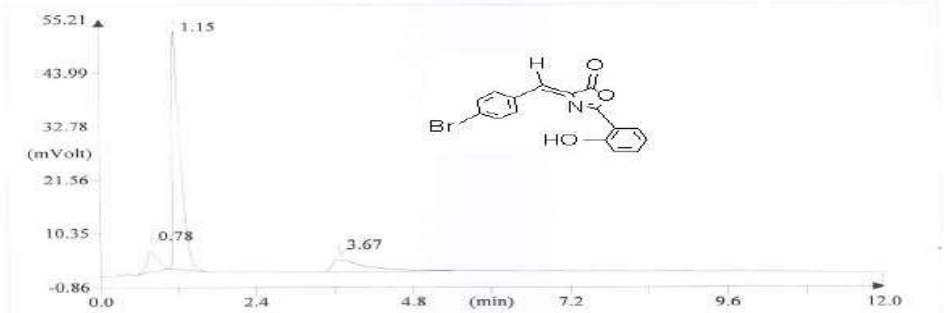
3.4 Mass spectra



3.5CHN analysis

FLASH EA 1112 SERIES CHN REPORT
THERMO FINNIGAN

Method filename:	C:\Program Files\Thermo Finnigan\Eager 300 for EA1112\DATA\Sys_data_es
Sample ID:	BHA (# 42)
Analysis type:	UnkNown
Chromatogram filename:	UNK-10072015-2.dat
Sample weight:	1.169



Element Name	Element %	Ret. Time
Nitrogen	4. 15	0. 78
Carbon	55. 72	1. 15
Hydrogen	2. 86	3. 67

Conclusion

The oxazolone moiety responsible for biological and medical activities.The activity studies of all the synthesized compounds against bacterial strains in both gram positive and gram negative activity against bacterial strains revealed that all the compounds shows moderate activity against Pseudomonas aeruginosa MTCC No. 1034compared with standard pencillin. Activity against Fungi Rizopusmicrosporus var. oligosporus (MTCC No: 2785) revealed that five compounds out of seven showed good activity at 100µg/ml**.**In view of their further scope in various pharmacological activities, we have prepared few oxazolones with substituted amino acids as starting material**.**

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Keywords: Satellite Based Augmentation System (SBAS), Ionospheric Gradients, Ionospheric Pierce Point (IPP), Total Electron Content (TEC).

17. SECURED DATA TRANSMISSION IN WIRELESS SENSOR NETWORKS USING TESDA METHOD

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Wireless Sensor Network (WSN) are need to be more secure while transmittimg data as well as should deployed properly to reduce redundancy and energy consumption. WSNs suffer from many constraints, including low computation capability, small memory, limited energy resources, susceptibility to physical capture and the use of insecure wireless communication channels. These constraints make security in WSNs a challenge. In this paper presented a survey of security issues in WSNs and proposed a new algoritham TESDA which is optimized energy efficient secured data aggregation technic.

As the cluster head is rotated based on residual energy after each round of aggregation.so that network lifetime increases.Based on deviation factor caliculated ,the trust weight is assigned,if more deviation,then the trust value is less.Simulation results observed by using NS-2.From network animator and x-graphs the result are analysed.Among all protocols tesda is an enegy efficient secured data aggregation method.

Keywords—WSN; CH; BS; BECR; CBQR ; CPDA; EESDA;

18. VLSI ARCHITECTURE FOR PARALLEL MULTIPLIERS

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Multimedia applications requires high speed computing architectures to support high resolution graphic systems. Adders and Multipliers are the very important functional blocks in Arithmetic and Logic Unit (ALU) of high speed computing systems. Fast multiplication has always been a vital requirement in most of high performance computing systems. This paper presents the implementations of the high speed Multipliers and their comparative analysis. In this paper, we have proposed VLSI architecture for widely used parallel multipliers such as Booth's multiplier, Wallace multiplier and Dadda Tree multipliers and also presented their design attributes like speed, area. The design parameters of the multipliers can be

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analyzed to design optimum multiply and Accumulate (MAC) units for multimedia Filters, Synthesizers, Wireless communication channels, etc.

Keywords— Arithmetic Logic Unit, Digital Signal Processing (DSP), Multiply and (MAC), serial-parallel multiplier(SPM).

VLSI ARCHITECTURE FOR PARALLEL MULTIPLIERS

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***Abstract* — Multimedia applications requires high speed computing architectures to support high resolution graphic systems. Adders and Multipliers are the very important functional blocks in Arithmetic and Logic Unit (ALU) of high speed computing systems. Fast multiplication has always been a vital requirement in most of high performance computing systems. This paper presents the implementations of the high speed Multipliers and their comparative analysis. In this paper, we have proposed VLSI architecture for widely used parallel multipliers such as Booth's multiplier, Wallace multiplier and Dadda Tree multipliers and also presented their design attributes like speed, area. The design parameters of the multipliers can be analyzed to design optimum multiply and Accumulate (MAC) units for multimedia applications like Filters, Synthesizers, Wireless communication channels, etc.**

Keywords— Arithmetic Logic Unit, Digital Signal Processing (DSP), Multiply and Accumulate Unit (MAC), serial-parallel multiplier(SPM).

I. INTRODUCTION

Multiply and Accumulation (MAC) unit in Digital Signal Processors contains the combination of adder and multiplier. The Multiplication is a performance critical unit in most of the microprocessor, digital signal processor and graphics engines. The architecture and comparison study of various adders and multipliers used in MAC were demonstrated in literature [12] [13]. So high speed multipliers are essential in advanced electronic systems like FIR filters, digital signal processors and microprocessors etc. where speed is main criteria. At present time taken by multiplication operation is important in determination of instruction cycle time period of a DSP chip. Since the demand of high speed computing for signal processing applications is increasing, many digital signal processing (DSP) systems started using high speed multiplication unit to implement algorithms such as convolution, filtering and frequency analysis. There are mainly three kind of multipliers called, Serial multiplier, Parallel Multiplier and Serial-parallel multiplier.

A. Serial Multiplier

In serial multiplication, sequential circuits are being used with feedbacks. The partial products are sequentially produced and then added serially as per the operation. The speed of serial multiplier is less as compared to parallel multiplier because, 1. Serial multiplier adds each bits of the multiplicand sequentially and the process is repeated for each of the multiplier bits, 2. Only one adder can be used to add m × n number of partial products where m and n are number of bits of multiplicand and multiplier respectively.

B. Parallel Multiplier

In parallel multiplier, the parallel multiplication process is break down into two parts, namely partial product generation and partial product accumulation. Generation of partial products is done first by multiplying the multiplicand with each bit of the multiplier and then these partial products are added together parallel to generate the resultant of product P. Number of partial products to be added plays significant role in determining the delay caused by the parallel multiplier. Parallel multipliers are further divided into Array Multiplier and Tree Multiplier. Booth's multiplier is a kind of Array Multiplier and Wallace and Dadda is a kind of Tree multiplier and it also known as column compression multipliers. This paper presents the high speed architecture for

C. Serial-parallel multiplier (SPM)

The Serial-Parallel Multiplier (SPM) operates on each bit of multiplier serially, but it uses parallel adder for partial product accumulation. It brings intermediate trade off between time consuming serial multiplier and area consuming parallel multiplier.

D. MAC Unit

A MAC unit consists of multipliers and accumulators that hold the sum of the previous consecutive products. MAC unit is one of the key blocks for digital signal processing system and plays important role in its delay and area determination. The behaviour of MAC unit is given by the following equation.

$$P = \sum_{i=0}^{N} A_i \times B_i,$$

Where N is length of the sequence equal to sum of length of A and B, P is product, A and B are multiplicand and multipliers respectively. This paper presents the architecture of high speed parallel multipliers, i.e. booth's multipliers, Wallace multiplier and Dadda multipliers, which are widely used for MAC design.

The remaining paper is organized as the literature review in section II, behaviour and architecture of the selected parallel multipliers in section III, implementation of MAC using

multipliers, results and discussion in section IV and finally paper is concluded in section V.

II. Literature Review

Column compression multiplier prolonged to be studied due to their high speed functioning. This multiplier total delay is proportional to the logarithm of the input word length. These multipliers are swifter than array multipliers in which delay grows linearly with operand word length. According to Thomas Ko Callaway [1], the column compression multipliers are more power proficient as compared to array multipliers. Wallace [2] introduced a method for fast multiplication centred on summing the partial product bits on parallel by using a tree of carry save adders which was recognized as the Wallace tree. Dadda [3] later advanced Wallace's method by significant a compressor placement strategy that required fewer compressor in the partial product reduction stage at the fee of larger carry-propagate adder. S. Veeramachaneni proposed novel architectures and the designs of low power and high speed compressors for addition in the partial product addition stage or accumulation stage. The compressors 3:2, 4:2 and 5:2 are the essential components in many applications where addition is required most importantly in multiplication [4]. Booth multiplier algorithm works by analyzing the initial partial product P last two bits and the corresponding operation of (01) add , (10) subtract , (11,00) arithmetic right shift operation is done on the partial product P and this stage prolongs for n-bit stages. Booth multiplier along with additional modules like logic functions, subtraction module, addition module division module squaring module are combined to design calculator [6]. S. Malik, S. Dhall have designed a MAC unit that consisted of 8- bit Booth's Multiplier, 16-bit Ripple carry Adder and 17- bit accumulator where the accumulator is made of parallel in parallel out shift register. The basic operation of MAC is the product of and is always given to the 17 bit- accumulator and then again added with the next product of and [7]. In the year 1950's, multiplier speed was notably improved with the introduction of Booth multiplier. Booth's method and the modified Booth's method do not require a rectification of the product when either or both of the operands is negative for two's complement numbers [8]. The MAC unit [9] is composed of 8- bit Wallace tree Multiplier, 17- bit register, 17 bit accumulator. Wherein [9] the accumulator is 17–bit carry look ahead adder used to increase the speed. The MAC has the ability to multiply and add with the previous product for 8 times. It also consists of block enabling technique in which the block which is not being used for the operation will be kept off.

III. Behaviour and Architecture of Parallel Multipliers

A. Booth Multiplier

Booth's algorithm is one of the important algorithms to perform signed multiplication on binary numbers. It consist of repeatedly adding one of two already determined values A and S to a initial product A, then performing a arithmetic right shift on A, S and Q. Where A is initial product of size equal to the sum of size of Multiplier Q and Multiplicand S. Let's consider x and y be the multiplicand and multiplier with size and respectively. The flow chart of fast Booth's multiplier algorithm to obtain the product of x and y is shown below in figure 1.

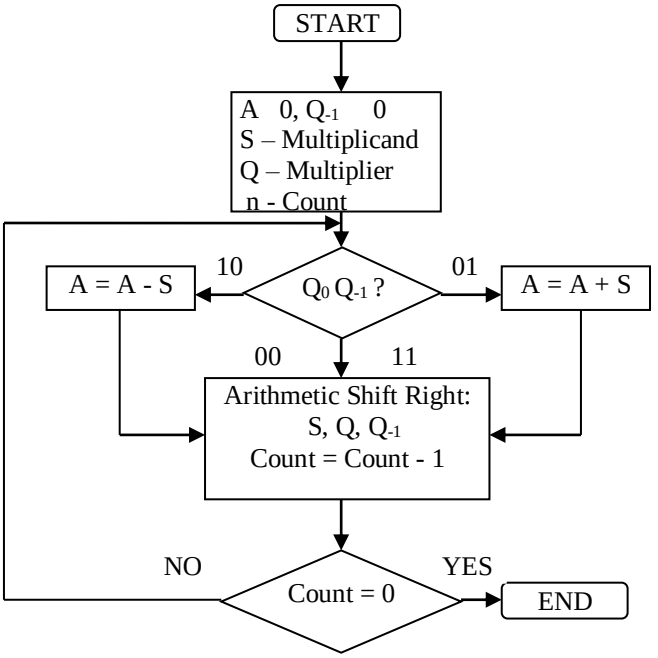

Figure 1. Flow chart of Booth's Multiplier

B. Wallace tree multiplier

In 1964 C. S. Wallace introduced a method for multiplication centred on summing the partial product bits in parallel using a tree of carry save adders which became well-known as the Wallace tree. The flow chart of Wallace-tree multiplier is shown in figure 2.

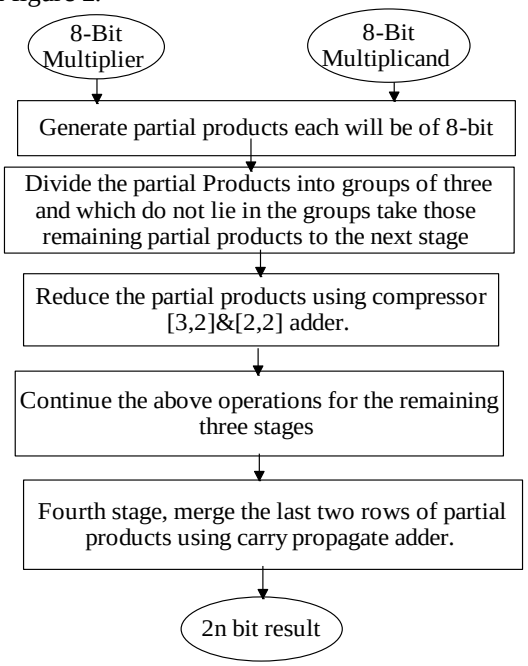

Figure 2.Flow chart of Wallace Multiplier.

Implementation of digital multiplier is reliant to the scheme used for addition of partial product array bits. As delay is proportional to the size of the multiplicand, the multiplier blocks will need more time to perform the task. Therefore partial products are condensed using a technique called carry save addition which allows successive additions in one global step. In the carry-save adder, carry transmission is avoided by treating the intermediary carries as outputs instead of advancing them to the next higher bit position.

C. Dadda multiplier

The Dadda multiplier follows refined Wallace's method. The flow chart of Dadda Multiplier is sown in figure 3.

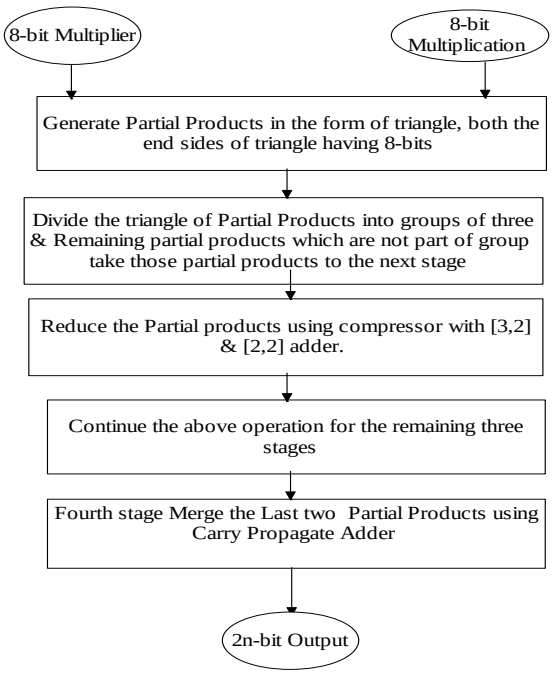

Figure 3.Flow chart of Dadda Multiplier

IV RESULTS/DISCUSSION

The above implemented multipliers are simulated using Xilinx and synthesized using Xilinx 13.2, virtex-5,XC5VLX110T-FF1136.The synthesis results for all three multiplier are obtained and their attributes are analyzed. The attributes, i.e. area and speed, of the parallel multipliers are summarized in table 1. The table 1 demonstrates the detailed comparative analysis of the implemented multipliers in terms of delay, area. From table 1, Booth's Multiplier delay is 3.29ns, Wallace Multiplier delay is 14.665 ns and the delay for Dada Multiplier is 12.834ns.

Table 1. Summary of Parallel Multipliers

Multiplier algorithm	Area (Number of Bit Slices)	Delay (ns)
Booth	95	3.29
Wallace	107	14.665
Dadda	111	12.834

V CONCLUSION / FUTURE WORK

The behavior of parallel Multipliers Booth, Wallace and Dadda Multiplier is described using verilog HDL, and then simulations results and synthesis reports are obtained. The synthesis report for the Multiplier shows that booth's multiplier has the least delay and can be used for low cost application devices. Further study and comparative analysis can be done on higher range Multiplier like 16-bit, 34-bit and 64 bit. In future, the analysis can be carried out on single precision and double Precision floating point multiplier.

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A NOVEL ALGORITHM FOR DETECTING HEART DISEASE

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ABSTRACT

In this paper we present the RRP algorithm with new adaptive method with new solution to resolve respective problem RR interval algorithm in heart signal processing. At first we focus on some previous research, to conclude that, the important ECG processing algorithms discussed on deviation of ST section, width, height and duration of ORS complex of heart signal, efficient diagnosis, noise filtering contain baseline shifts, muscle artefacts and electrode motion. Also RRP algorithm include three parts of signal processing, determination signal features and compare with previously established patient heart signal. In the last stage, using adaptive threshold values for peak detection routines were used for the heart patients with various conditions. The algorithm efficiency is simulated and compared with conventional RR interval algorithm by MATLAB.

Keywords: ECG; Heart; QRS Detection; RRP Algorithm.

I INTRODUCTION

ECG is a graphical representation of the heart impulses. A conventional ECG waves formed under contract with the letters P, Q, R, S, T, have been named. Result of impulses natural speed and direction makes normal sinus rhythm. Otherwise, represent the heart disease. Waves, Q, R, S forms a group together as QRS complexes are discussed. The Complex QRS, ventricular electrical depolarization wave (contraction of the ventricles) show. The Broad QRS duration indicates abnormal or prolonged ventricular polarization.

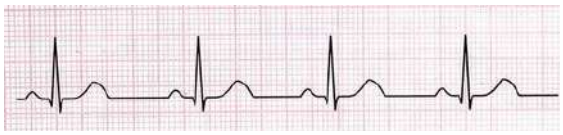
Segment ST, this piece of time between the completion and start depolarization ventricular muscle. This item may be a transient ischemia and muscle damage goes up or down.

T wave represents ventricular depolarization, if it is negative definite MI.

In sinus tachycardia as shown in fig 1, the production rate is faster than 100 beats per minute and In sinus bradycardia the production rate is less than 60 beats per minute, but the signal will be guided by the normal

Normal Sinus Rhythm

Sinus *Tachycardia*



Sinus Bradycardia

Figure 1: A sample graph for Heart Disease

Tachycardia, arrhythmia include irreducible, ventricular tachycardia, ventricular fibrillation ventricular tachycardia irreducible fibrillation, PSVT atrial flutter, fibrillation atrial tachycardia, atrial multifocal, tachycardia, atrial attack.

Sinus bradycardia include Stop arrhythmia, ventricular escape rhythm at Block Level 3, Block mobitz type II.

II LITERATURE REVIEW

In the last decade, a lot of new techniques have been proposed for the detection of QRS complexes, for example, algorithms based on artificial neural networks, genetic algorithms, and wavelet transforms, filter banks and hierarchical methods based on nonlinear transformations.

First Detection Algorithm

As noted in Section A, ECG frequency band is between 15 to 150 Hz. Baseline oscillation frequencies below 1 Hz and above 150 Hz frequency noise is caused by the muscles. The pre-processing algorithm is divided into two parts.

*Filter :*feature extraction stage with linear and nonlinear filters

• *peak detection* : To find the location & duration of the peak signal

The decision algorithm is divided into three phases

• *Ventilation :*threshold values are determined

Based on peak detection, signal levels and signal to noise ratio (Two sets threshold values are used to detect heart signals (a) filter threshold values (b) integrated window threshold values)

• *Learning:* The RR interval Average value and the heart rate limit

bound.

• *QRS detection :*QRS wave detection and differentiation of T –wave measurements.

Fetal heart rate Bit calculation algorithm

Fetal heart rate is one of the few signals which may register as a noninvasive.

In many cases the only available information source is the power

spectrum of fetal heart rate. The fetal heart rate algorithm is performed in two stages.

• *Filter:* the best estimation frequency for low pass filter is 2 Hz. the output waveforms is some bumps without any sharp point

• *Autocorrelation:* the bit rate is obtained with frequency domain autocorrelation. Heart rate corresponds to distance between the cardiac cycle (n) and the cardiac cycle earlier (n-1).

ECG ASPARS algorithm is a three-stage High Resolution QRS Detection model:

Algorithm can be divided into three stages:

1. *Estimation:* The initial estimation obtains the valid R wave points.

2. *Squares:* Chi-squares non-linear function for computes. The average values for each data points with 20 KHZ sampling rate. The classification rules are based on numerical slope, amplitude and width signal analysis. Peak Level is used to distinguish noise from signal, which is usually half of the maximum peak to peak values.

3. *Peak detection:* data extraction of the R wave with a peak detection window which is placed on the centre of valid points.

III PATTERN RECOGNITION METHODS

The classes of patterns are pre specified ratio, Classifier algorithm called pattern recognition which makes the class attribute pattern. Pattern recognition techniques have generally fall into three categories:

1. *Statistical methods:* patterns and classes are generated with probability distribution.

2. *Structure (analytic):* patterns and classes are characterized by formal structures. In these methods, the basic units are defined as Primitive. All models are expressed in terms of the inter relationships between Primitive Grammar. In most cases, these methods are applied to certain structural pattern.

3. *ANN:* artificial neural networks, each pattern are described in terms of several characteristics. Point's attributes are considered in a multidimensional space. Feature space is divided into several regions corresponding to each class. Pre specified classes in supervised classification by training data determine the boundaries of different classes, there confirm the marked areas. Template feature vector obtained through measurement or observation. in general , Pattern recognition includes the following system components :

• *filter :*Register sensors and pre-processing

• *Patterns:* Feature Extraction which specifies the attributes. Suitable properties have two important properties: First, all models have the collection properties which belong to the same class. Second, the patterns are belonged to other classes do not have those features.

• *Classifier:* classifier which has feature space into regions are labelled and related to each class partitions. The classifier is characterized by the collection set of discrete functions.

• *Monitor:* the Monitor provides information about the training data.

In unsupervised learning data is corresponded to classes without any initial information. In the clustering step, basically, similar to supervised learning, the data is placed in different clusters.

A. Error back propagation algorithm (BPA) used in neural networks.

Artificial neural networks (ANNs) networks are inspired by living organisms that are used in pattern recognition. ANN classification Decision making process in medical data characteristics is suitable. Usually, multilayer neural networks using error back propagation algorithm (BPA) which is the nonlinear classifier, with supervised learning algorithm. The recursive function for learning process always calculates a mean square error cut, to minimize the overall error, initial weights are selected randomly, and then frequently connections weights have been changed to reduce the overall errors. It is desirable that the training data set distributes uniformly in the input neurons. The algorithm consists, the two main routes, with forward and backward path.

1. *Forward path:* An educational model is applied to the network, its effects on intermediate layers through the output layer and spread until eventually obtains the actual network output. In this way, the MLP network parameters (weight matrices and bias vectors), are considered fixed and unchanged.

2. *Backward path:* the opposite direction, the MLP network parameters are adjustable. Error vector is equal to the difference between the desired response and the actual response.

Learning algorithm BPA is based on the approximate calculation which can be reduced by the equations below:

The algorithm convergence speed is slow, Sometimes instability called oscillatory and network parameters is also called divergent, the network has a local minimum points may not be sure that an optimum solution is reached. Convergence of the algorithm is dependent to the initial values of MLP neural network parameters, so that a good choice would be a great help in faster convergence, vice versa.

B. Automatic gain control AGC algorithms with adaptive filtering

Adaptive filtering enables us to have a reference value, internal setting collection, optimize performance in noise wide range. The filtered analog output signal is controlled by changing the amplifier gain with recursive algorithm, In fact, algorithm are presented as gain amplifiers automatic code to set the adaptive digital filter threshold values .

C. QRS Detection Algorithm with FPGA

FPGA consists an array include hundreds of configurable blocks, which can run all kinds of digital logic functions with blocks connection wires. The logical functions performed by each blocks and the electronic switch controls wiring between blocks. The switch configuration is determined in the FPGA configuration memory cells contents. FPGA is used in the cardiac signals analysis and diagnose heart defects by wavelet transform with ALS Adaptive Lifting Scheme implementation, Split into three stages.

1. Split: To break even and odd signal into two signals from ECG signal successive samples.

2. *Filter:* The noise which is reduced with update the step pass filter.

3. *Detection:* Predict step which improve the detection accuracy.

D. Mapping algorithm with delay Phase Portrait

1. *Register:* to receive signals from the sensors and data mapping in two dimension space.

2. *Filter:* low-pass filter with preprocessing and computation Phase Portrait

3. *Peak detection:* if R peak value is bigger than threshold value then QRS decision rules runs, otherwise if the R peak value is bigger than RR intervals mean value then reduces the threshold value and also decision rules runs.

E. Multivariate cardiac signals analysis algorithms

1. *Register* : to receive signals from sensors

2. *filter :*Pre-processing and filtering

3. *Pattern:* Feature Extraction which specifies the attributes.

4. *Classifiers :*which has feature space into regions

5. *Training:* Supervisor will provide information about each categories training data. Accordingly, the feature space regions boundaries will be determined.

6. *Learning:* unsupervised learning is without any initial information about the class corresponds data.

IV WAVELET TRANSFORMS METHODS

Fourier transforms to obtain the filtered signal in the time domain. Unwanted and undesired frequency components from the signal frequency spectrum are removed. Finally the inverse Fourier transform executes. The main idea is that the signal frequency spectrum made up a trigonometric functions combination which is converted by Fourier transforms Frequency and then inverse Fourier transform.

A. MALLAT Algorithm with wavelet transforms dyadic discrete

MALLAT algorithm is more suitable for discrete signals with discrete wavelet transform may be implemented by the number of times. The high and low pass filters make impulse response . with finite length The down sampling action removes redundancy from signal and can increases pass MALLAT algorithm with wavelet transition .filter later stage signal scale delayed can detects the heart defects by octet equivalent filter bank.

B. The algorithm combines Wavelet transform with QRS wave detector

Method implementation Wavelet transform with Analog QRS wave detector with Gabor wavelet filter, constant circuit, Peak detector and comparator. Adjustable threshold value is calculated according to the following formula

C. Power computation algorithm

The heart signal processing is implemented by two moving average filter and low pass filter with enhanced features based on the signal power value, consists the three stages.

1. Filter: pre-processing using pass filters

2. Process: signal processing

3. Detect: Locate and QRS detection

D. Re sampling algorithm

The combination of Fourier transform and re sampling to make extract signal components ability, which consists of four stages.

1. Detect: QRS detection stage
2. Transform: the wavelet transform of ECG signal two-dimensional array.
3. Process: the pure signal is extracted from the two dimensional array.
4. Reconstruction: signal reconstruction phase

V METHODOLOGY

RRP is a new algorithm which is purposed with combination of some before algorithms.

A. RRP algorithm explanation

The RRP algorithm's first step makes a reference signal from patient's heart, this original storage can be save by the physician or patient. Then signal parameters are measured and applied to algorithm's input. The algorithm's result corresponds to patient's heart.

The signal parameters include heart rate and signal amplitude will be calculated up to 15 seconds. (This generally ensures substantial reduction the muscle and electrode motion noise).

B. Two algorithm's assumptions:

1. T*achycardia:*To ensure that we suppose , wherever heart rate is greater than 100 beats per minute (in both normal and alarm status), arrhythmia or tachycardia rhythm is issued
2. *Bradycardia:* To ensure that we suppose, whenever the heart rate is lower than 60 beats per minute in both the state's normal rhythm arrhythmia and bradycardia is issued.

C. Algorithm steps:

*1. Filter low :*remove Baseline Noise

2. *Least Square:*Remove the noise filter (zero phase) and Least Squares (Least Sq.) with appropriate sampling frequency
3. *Resample:*Interpolation calculated using the Resample FFT points
4. *Filterhigh:*Noise muscle electrode movement
5. *RR interval:* Calculate the RR interval calculations based on peak detection threshold values based on a patient's signal.
6. *Sliding window:* Calculate the minimum and maximum frequency values for heart signal sliding window.
7. *Process 1:* calculate the RR interval parameters sinus tachycardia, sinus arrest or heart diagnosed as Function absence of atrial sinus node is known from bradycardia status.
8. *Process 2:* control and distinguish the QRS, P, T wave for Diagnosis arrhythmias from tachycardia.
9. *Process 3 :*Risk rate was normalized to the corresponding alarm will be issued

VI RESEARCH SIMULATION

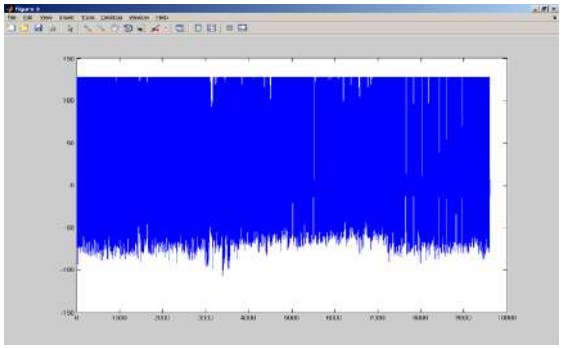


Figure 2: Heart signal with noise diagram

In the next stage, the baseline noise is removed by subtracting the average signal with formula:

Using ECG - mean (ECG) as shown in fig 3

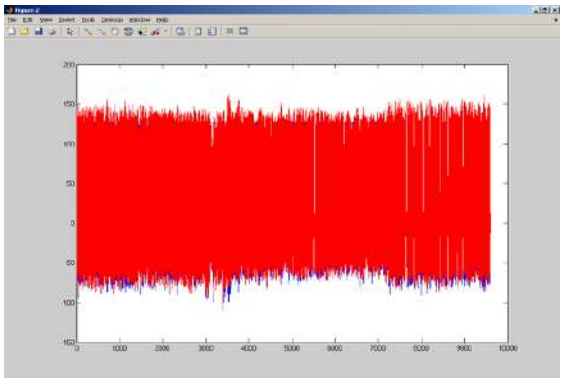


Figure 3: Remove Baseline Noise diagram

In next stage, the zero phase digital filter is applied to ECG signal processing the without Baseline Noise in both the forward and backward directions. The result has many characteristics such as reduce noise and preserves the QRS complex at the same time without making delay .as shown in fig 4 , FILTFILT function in MATLAB simulates it.

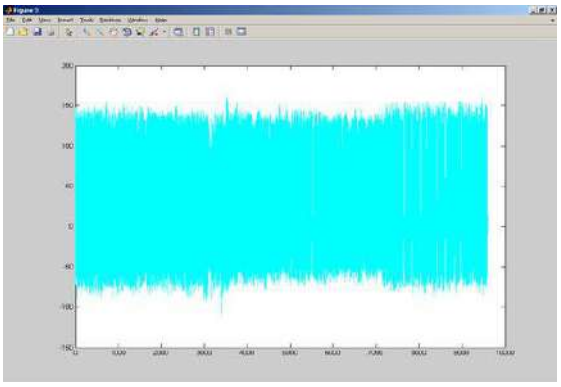


Figure 4: Zero phase noise removal filter and Least Squares diagram

In the next stage, one dimensional interpolation with Fourier transform (FFT based) method applies to calculate the Resample two percentage points. As shown in fig 5 INTERPFT function in MATLAB simulates it.

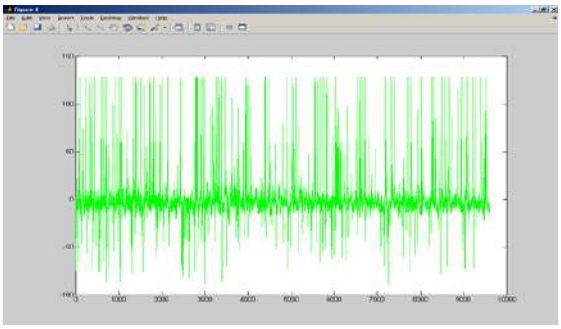


Figure 5: Interpolation FFT Resample method

In the next stage, one dimensional median filter is applied with the sliding window which replace the center value by mean pick points value(That's a nonlinear method). As shown in fig 6, INTERPFT function in MATLAB simulates it.

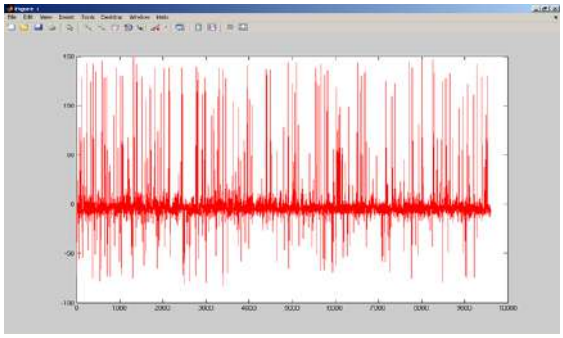


Figure 6: Noise filter with least squares and 2 Hz sample frequency

In the next stage, the conventional thresholds values are applied to peak detection routines. As shown in fig 7, with MATLAB Programming simulates it.

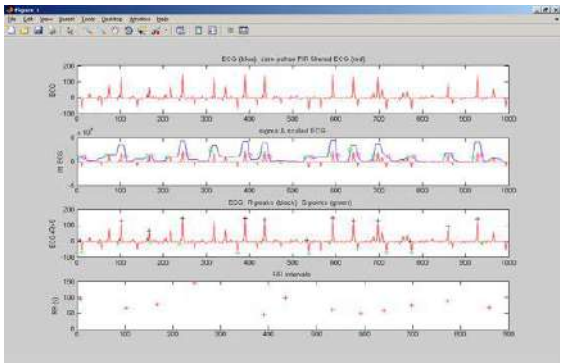
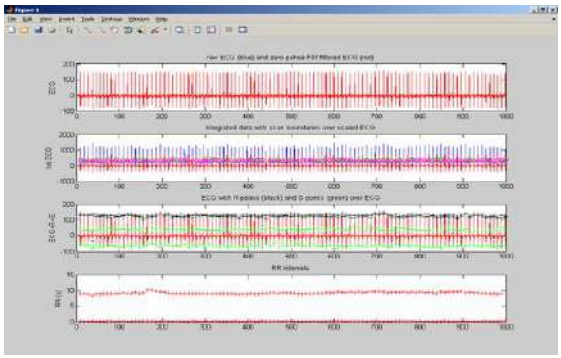


Figure 7: RR interval calculated based on peak detection calculations

In the next stage, the conventional thresholds values are applied to peak detection routines for patient's heart signal. As shown in fig 8, with MATLAB Programming simulates it. Which is useless result for Established heart disease?



VII CONCLUSIONS

In this paper, some important algorithms in the cardiac arrhythmias, time and frequency field and by linear and nonlinear functions was described. At the end, the combination of these algorithms which provides a new algorithm with more flexibility in heart pulse counting and QRS, T, P wave detection. Obviously this method has been as a diagnostic tool to assist physicians in cardiac disease analyzing. However in generally, these tools result never has 100% recognition accuracy. The accuracy of these tools depends on several factors; include the threshold values which are main matter in this new algorithm. Of course, as the simulation results presented demonstrates, the RRP algorithm's accuracy and efficiency is high. As a general conclusion it can be said that the RRP algorithm can be used as a diagnostic tool for heart health trustworthy.

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17. SECURED DATA TRANSMISSION IN WIRELESS SENSOR NETWORKS USING TESDA METHOD

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Wireless Sensor Network (WSN) are need to be more secure while transmittimg data as well as should deployed properly to reduce redundancy and energy consumption. WSNs suffer from many constraints, including low computation capability, small memory, limited energy resources, susceptibility to physical capture and the use of insecure wireless communication channels. These constraints make security in WSNs a challenge. In this paper presented a survey of security issues in WSNs and proposed a new algoritham TESDA which is optimized energy efficient secured data aggregation technic.

As the cluster head is rotated based on residual energy after each round of aggregation.so that network lifetime increases.Based on deviation factor caliculated ,the trust weight is assigned,if more deviation,then the trust value is less.Simulation results observed by using NS-2.From network animator and x-graphs the result are analysed.Among all protocols tesda is an enegy efficient secured data aggregation method.

Keywords—WSN; CH; BS; BECR; CBQR ; CPDA; EESDA;

18. VLSI ARCHITECTURE FOR PARALLEL MULTIPLIERS

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Multimedia applications requires high speed computing architectures to support high resolution graphic systems. Adders and Multipliers are the very important functional blocks in Arithmetic and Logic Unit (ALU) of high speed computing systems. Fast multiplication has always been a vital requirement in most of high performance computing systems. This paper presents the implementations of the high speed Multipliers and their comparative analysis. In this paper, we have proposed VLSI architecture for widely used parallel multipliers such as Booth's multiplier, Wallace multiplier and Dadda Tree multipliers and also presented their design attributes like speed, area. The design parameters of the multipliers can be

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analyzed to design optimum multiply and Accumulate (MAC) units for multimedia Filters, Synthesizers, Wireless communication channels, etc.

Keywords— Arithmetic Logic Unit, Digital Signal Processing (DSP), Multiply and (MAC), serial-parallel multiplier(SPM).

VLSI ARCHITECTURE FOR PARALLEL MULTIPLIERS

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***Abstract* — Multimedia applications requires high speed computing architectures to support high resolution graphic systems. Adders and Multipliers are the very important functional blocks in Arithmetic and Logic Unit (ALU) of high speed computing systems. Fast multiplication has always been a vital requirement in most of high performance computing systems. This paper presents the implementations of the high speed Multipliers and their comparative analysis. In this paper, we have proposed VLSI architecture for widely used parallel multipliers such as Booth's multiplier, Wallace multiplier and Dadda Tree multipliers and also presented their design attributes like speed, area. The design parameters of the multipliers can be analyzed to design optimum multiply and Accumulate (MAC) units for multimedia applications like Filters, Synthesizers, Wireless communication channels, etc.**

Keywords— Arithmetic Logic Unit, Digital Signal Processing (DSP), Multiply and Accumulate Unit (MAC), serial-parallel multiplier(SPM).

I. INTRODUCTION

Multiply and Accumulation (MAC) unit in Digital Signal Processors contains the combination of adder and multiplier. The Multiplication is a performance critical unit in most of the microprocessor, digital signal processor and graphics engines. The architecture and comparison study of various adders and multipliers used in MAC were demonstrated in literature [12] [13]. So high speed multipliers are essential in advanced electronic systems like FIR filters, digital signal processors and microprocessors etc. where speed is main criteria. At present time taken by multiplication operation is important in determination of instruction cycle time period of a DSP chip. Since the demand of high speed computing for signal processing applications is increasing, many digital signal processing (DSP) systems started using high speed multiplication unit to implement algorithms such as convolution, filtering and frequency analysis. There are mainly three kind of multipliers called, Serial multiplier, Parallel Multiplier and Serial-parallel multiplier.

A. Serial Multiplier

In serial multiplication, sequential circuits are being used with feedbacks. The partial products are sequentially produced and then added serially as per the operation. The speed of serial multiplier is less as compared to parallel multiplier because, 1. Serial multiplier adds each bits of the multiplicand sequentially and the process is repeated for each of the multiplier bits, 2. Only one adder can be used to add m × n number of partial products where m and n are number of bits of multiplicand and multiplier respectively.

B. Parallel Multiplier

In parallel multiplier, the parallel multiplication process is break down into two parts, namely partial product generation and partial product accumulation. Generation of partial products is done first by multiplying the multiplicand with each bit of the multiplier and then these partial products are added together parallel to generate the resultant of product P. Number of partial products to be added plays significant role in determining the delay caused by the parallel multiplier. Parallel multipliers are further divided into Array Multiplier and Tree Multiplier. Booth's multiplier is a kind of Array Multiplier and Wallace and Dadda is a kind of Tree multiplier and it also known as column compression multipliers. This paper presents the high speed architecture for

C. Serial-parallel multiplier (SPM)

The Serial-Parallel Multiplier (SPM) operates on each bit of multiplier serially, but it uses parallel adder for partial product accumulation. It brings intermediate trade off between time consuming serial multiplier and area consuming parallel multiplier.

D. MAC Unit

A MAC unit consists of multipliers and accumulators that hold the sum of the previous consecutive products. MAC unit is one of the key blocks for digital signal processing system and plays important role in its delay and area determination. The behaviour of MAC unit is given by the following equation.

$$P = \sum_{i=0}^{N} A_i \times B_i,$$

Where N is length of the sequence equal to sum of length of A and B, P is product, A and B are multiplicand and multipliers respectively. This paper presents the architecture of high speed parallel multipliers, i.e. booth's multipliers, Wallace multiplier and Dadda multipliers, which are widely used for MAC design.

The remaining paper is organized as the literature review in section II, behaviour and architecture of the selected parallel multipliers in section III, implementation of MAC using

multipliers, results and discussion in section IV and finally paper is concluded in section V.

II. Literature Review

Column compression multiplier prolonged to be studied due to their high speed functioning. This multiplier total delay is proportional to the logarithm of the input word length. These multipliers are swifter than array multipliers in which delay grows linearly with operand word length. According to Thomas Ko Callaway [1], the column compression multipliers are more power proficient as compared to array multipliers. Wallace [2] introduced a method for fast multiplication centred on summing the partial product bits on parallel by using a tree of carry save adders which was recognized as the Wallace tree. Dadda [3] later advanced Wallace's method by significant a compressor placement strategy that required fewer compressor in the partial product reduction stage at the fee of larger carry-propagate adder. S. Veeramachaneni proposed novel architectures and the designs of low power and high speed compressors for addition in the partial product addition stage or accumulation stage. The compressors 3:2, 4:2 and 5:2 are the essential components in many applications where addition is required most importantly in multiplication [4]. Booth multiplier algorithm works by analyzing the initial partial product P last two bits and the corresponding operation of (01) add , (10) subtract , (11,00) arithmetic right shift operation is done on the partial product P and this stage prolongs for n-bit stages. Booth multiplier along with additional modules like logic functions, subtraction module, addition module division module squaring module are combined to design calculator [6]. S. Malik, S. Dhall have designed a MAC unit that consisted of 8- bit Booth's Multiplier, 16-bit Ripple carry Adder and 17- bit accumulator where the accumulator is made of parallel in parallel out shift register. The basic operation of MAC is the product of and is always given to the 17 bit- accumulator and then again added with the next product of and [7]. In the year 1950's, multiplier speed was notably improved with the introduction of Booth multiplier. Booth's method and the modified Booth's method do not require a rectification of the product when either or both of the operands is negative for two's complement numbers [8]. The MAC unit [9] is composed of 8- bit Wallace tree Multiplier, 17- bit register, 17 bit accumulator. Wherein [9] the accumulator is 17–bit carry look ahead adder used to increase the speed. The MAC has the ability to multiply and add with the previous product for 8 times. It also consists of block enabling technique in which the block which is not being used for the operation will be kept off.

III. Behaviour and Architecture of Parallel Multipliers

A. Booth Multiplier

Booth's algorithm is one of the important algorithms to perform signed multiplication on binary numbers. It consist of repeatedly adding one of two already determined values A and S to a initial product A, then performing a arithmetic right shift on A, S and Q. Where A is initial product of size equal to the sum of size of Multiplier Q and Multiplicand S. Let's consider x and y be the multiplicand and multiplier with size and respectively. The flow chart of fast Booth's multiplier algorithm to obtain the product of x and y is shown below in figure 1.

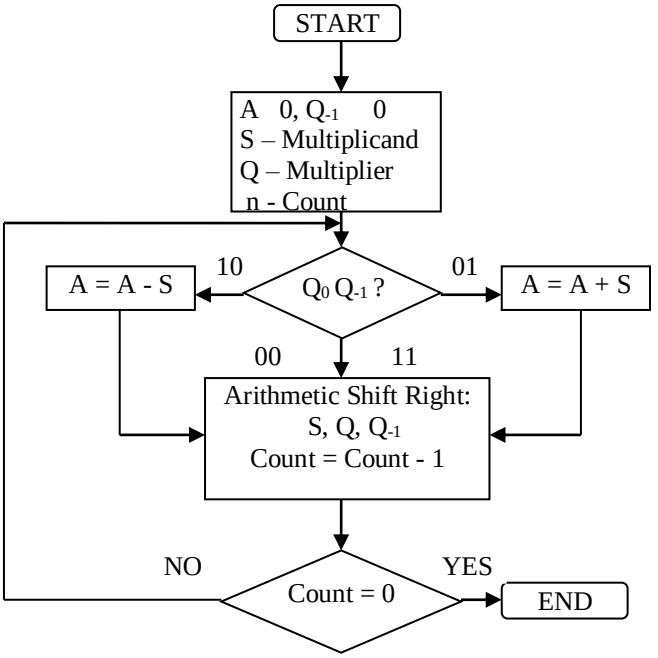

Figure 1. Flow chart of Booth's Multiplier

B. Wallace tree multiplier

In 1964 C. S. Wallace introduced a method for multiplication centred on summing the partial product bits in parallel using a tree of carry save adders which became well-known as the Wallace tree. The flow chart of Wallace-tree multiplier is shown in figure 2.

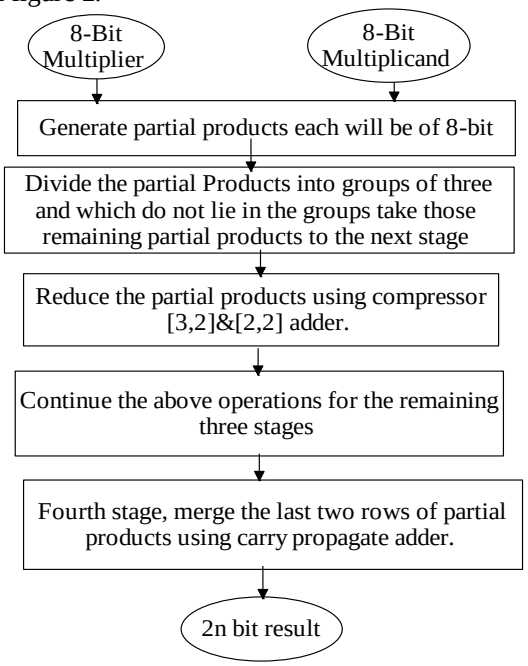

Figure 2.Flow chart of Wallace Multiplier.

Implementation of digital multiplier is reliant to the scheme used for addition of partial product array bits. As delay is proportional to the size of the multiplicand, the multiplier blocks will need more time to perform the task. Therefore partial products are condensed using a technique called carry save addition which allows successive additions in one global step. In the carry-save adder, carry transmission is avoided by treating the intermediary carries as outputs instead of advancing them to the next higher bit position.

C. Dadda multiplier

The Dadda multiplier follows refined Wallace's method. The flow chart of Dadda Multiplier is sown in figure 3.

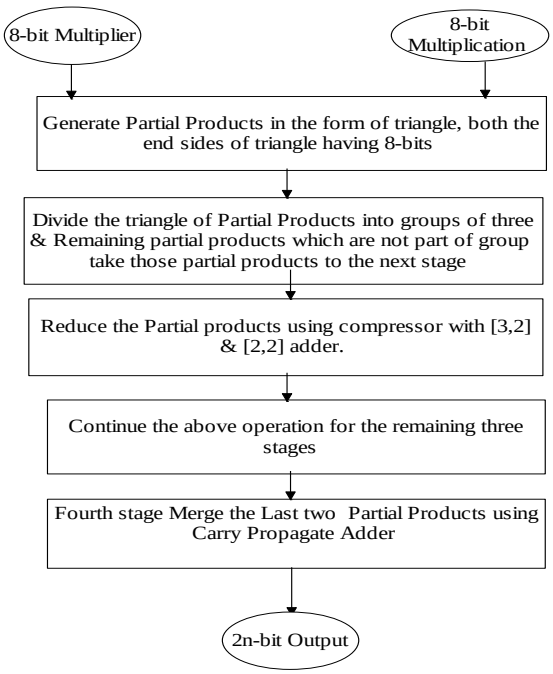

Figure 3.Flow chart of Dadda Multiplier

IV RESULTS/DISCUSSION

The above implemented multipliers are simulated using Xilinx and synthesized using Xilinx 13.2, virtex-5,XC5VLX110T-FF1136.The synthesis results for all three multiplier are obtained and their attributes are analyzed. The attributes, i.e. area and speed, of the parallel multipliers are summarized in table 1. The table 1 demonstrates the detailed comparative analysis of the implemented multipliers in terms of delay, area. From table 1, Booth's Multiplier delay is 3.29ns, Wallace Multiplier delay is 14.665 ns and the delay for Dada Multiplier is 12.834ns.

Table 1. Summary of Parallel Multipliers

Multiplier algorithm	Area (Number of Bit Slices)	Delay (ns)
Booth	95	3.29
Wallace	107	14.665
Dadda	111	12.834

V CONCLUSION / FUTURE WORK

The behavior of parallel Multipliers Booth, Wallace and Dadda Multiplier is described using verilog HDL, and then simulations results and synthesis reports are obtained. The synthesis report for the Multiplier shows that booth's multiplier has the least delay and can be used for low cost application devices. Further study and comparative analysis can be done on higher range Multiplier like 16-bit, 34-bit and 64 bit. In future, the analysis can be carried out on single precision and double Precision floating point multiplier.

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Abstract

Embedded Systems complexity is enhancing many folds in most of the product domains. Changing requirements and uncertainty during early stages of development are of greatest concern for the developing community, as they enhance system development complexities. Verification encompasses all aspects of system development process. This paper proposes an incremental paradigm that incorporates early integration and reduces uncertainty during initial phases of development under changing conditions of requirements. The method can be represented by a cascaded V-model. The verification methodology implementation issues are presented.

Keywords

Embedded systems Changing requirements Uncertainty in development Verification method Early integration Division of design-verification-cycle Cascaded V-model Implementation of verification method

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Abstract

In various domains like VLSI design, Embedded Systems, Signal processing, Image processing etc. combinational and logical circuit are the basic building blocks whereas addition is the fundamental step involved in any of it. Increasing the efficiency of these fundamental blocks is one of the major concerns in the application development. Moreover, power and delay are the major concern in the VLSI design so as to increase the efficiency of the circuit. In the combinational system performance and speed of the circuit is directly related with delay. In this paper hybrid adder circuit is designed using both Complementary Metal Oxide Semiconductor (CMOS) logic and transmission gates which performs addition at a low power and reduced delay. Further the speed of operation of the circuit is improved by introducing Gate Level Body Biasing (GLBB) in the design. The design was first implemented for full adder and then extended for 8 bit ripple carry adder. The circuit was implemented using Cadence Virtuoso tools in 180 nm technology. For 1.8 V supply at 180 nm technology, the average delay of the circuit is (114.5 ps), having moderate power consumption (27.52 mW) is found to have extremely low values than that resulted from the use of very weak CMOS inverters coupled with strong transmission gates. With additional GLBB circuit incorporated with the design proved useful in boosting the circuit. In comparison with the existing full adder the proposed Full adder found to offer significant improvement in terms of speed at the cost of power.

Keywords

Delay Hybrid full adder High speed adder Transmission gates Body biasing

Notes

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